Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC

Yan Zhu, Chi-Hang Chan, Si-Seng Wong, U Seng-Pan, and Rui Paulo Martins

***Abstract*— This brief reports a 120 MS/s 12-bit successive approximation register analog-to-digital converter (ADC). The conversion nonlinearity in a bridge digital-to-analog converter is analyzed, and its corresponding histogram-based ratio mismatch (HBRM) calibration is presented in detail. Verified by behavioral simulations as well as measured results, the solution improves both the dynamic performance and the static performance of the ADC. The measurement results demonstrate that the HBRM calibration effectively improves the signal-to-noise distortion ratio from 56.9 to 63.7 dB at dc input, with a sampling frequency of 120 MS/s.**

***Index Terms*— Bridge DAC, linearity calibration, SAR ADC.**

I. Introduction

Successive approximation register (SAR) analog-to-digital converters (ADCs) [1]–[7] achieve high-power efficiency due to its simple architecture and dynamic operation. The conversion linearity of an SAR ADC relies basically on the capacitive digital-to-analog converter (DAC), where the binary-weighted [1], [2], [4], [7] and bridge structures [3], [5], [6] are commonly used. The bridge-DAC has less total unit capacitors compared with the binary-weighted DAC under the same total capacitance according to the kT/C noise requirement. For example, a 12-bit DAC with binary-weighted structure requires a total of 4096 units, while the bridge-DAC obtains a minimum of 127 units, implementing 6 bit in the most significant bit (MSB) array and the least significant bit (LSB) array, respectively. Therefore, the bridge-DAC exhibits less interconnection and overhead area loss. However, it suffers serious conversion nonlinearity due to the mismatch of the nonunit attenuation capacitor as well as the top-plate parasitics at the inner node of the bridge-DAC [5], [8]. The existing background linearity calibration [1], [7] uses pseudorandom noise injection to estimate the radix error in a binary-weighed DAC and correct it in the digital domain. It involves no feedback to the analog circuitry that simplifies the circuit implementation and achieves higher calibration accuracy. However, the calibration requires additional signal injections and imposes a long converging time.

The SAR ADC with histogram-based ratio mismatch (HBRM) calibration was recently presented in [6]. The solution corrects the bridge-DAC's nonlinearity in digital domain, which also involves no feedback to the analog circuitry and costs less calibration time and effort. Based on the proposed solution [6], this brief analyzes the conversion nonlinearity in the bridge-DAC structure as well as the calibration accuracy relevant to the static and dynamic performances of the conversion, which was verified in behavioral simulations and measured results. To prove the effectiveness of the linearity calibration, an SAR ADC operating at 120 MS/s was designed in 90-nm CMOS, which is implemented with a bridge-DAC and metal–oxide–metal (MOM) capacitors.

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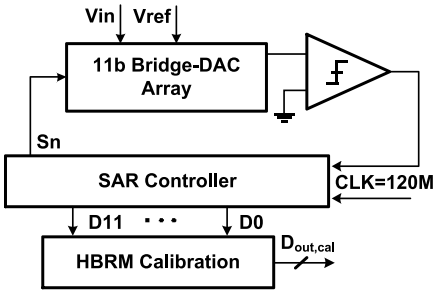


Fig. 1. SAR ADC architecture.

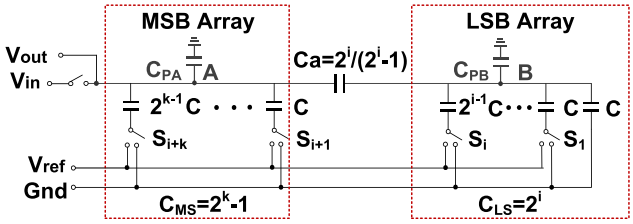


Fig. 2. n-bit bridge-structure DAC that contains a k-bit MSB and an i-bit LSB array ($k + i = n$).

II. ADC Architecture

The 12-bit ADC architecture is shown in Fig. 1, which consists of a bridge-structure capacitive DAC array, a comparator, an SAR controller, and the HBRM calibration engine. The DAC array is used to sample the input signal and subtract the reference voltages with a binary-searched approximation. The comparator is a two-stage dynamic latch [9]. The SAR controller, including the bit register and the switch drivers, performs $V_{\rm cm}$-based switching [3] for lower switching energy and better conversion linearity [8]. Since the bridge-DAC [3] is built in this design, its conversion nonlinearity is calibrated in the digital domain [6]. When the conversion is completed, the digital code enters the HBRM calibration engine to estimate and correct the conversion nonlinearities. The calibration is implemented off-chip, and its details are introduced in Section III.

III. Linearity Analysis in the Bridge DAC

An n-bit bridge-DAC array is shown in Fig. 2, which contains a k-bit MSB array and an i-bit LSB array. The attenuation capacitor C_a,

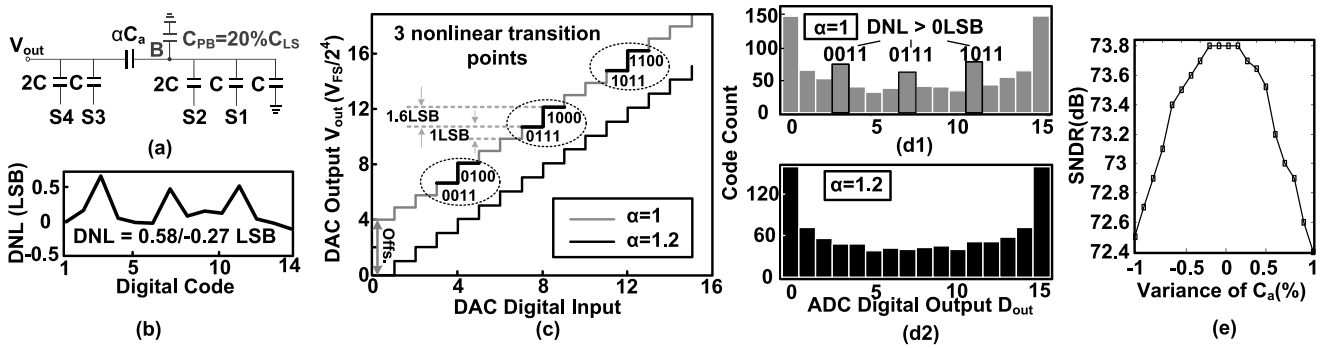


Fig. 3. (a) 4-bit (2 bit + 2 bit) bridge-DAC. (b) Corresponding DNL of the SAR ADC. (c) Transfer characteristic of the 4-bit-bridge DAC with respect to $\alpha = 1$ and $\alpha = 1.2$. For the clarification, offset is added to the case of $\alpha = 1$. (d1) Corresponding output code histogram of 4-bit SAR ADCs with a sine wave input, $\alpha = 1$. (d2) $\alpha = 1.2$. (e) SNDR versus variance of C_a in a 12-bit SAR built with (6 bit + 6 bit) bridge-DAC.

implemented in series with the MSB and the LSB arrays, is a nonunit capacitor with the value of $2^i/(2^i - 1)C$. The output equivalent capacitance of the bridge-DAC is only $2^k C$. Therefore, to satisfy the same kT/C noise, the bridge-DAC can be built with much larger unit capacitors than the binary-weighted approach. However, the bridge-DAC structure is very sensitive to the mismatch of the attenuation capacitor C_a and the top-plate parasitic capacitance $C_{\rm PB}$ at node B in Fig. 2. The analog output $V_{\rm out}$ (X) of a bridge-DAC, including the parasitics $C_{\rm PA}$ and $C_{\rm PB}$, can be calculated as [8]

$$V_{\rm out}(X) = \frac{(C_{\rm LS}+C_{\rm PB}+C_a)\sum_{j=1}^{k} 2^{j-1}{\rm CS}_{j+i}+C_a\sum_{j=1}^{i} 2^{j-1}{\rm CS}_j}{C_a(C_{\rm LS}+C_{\rm MS}+C_{\rm PA}+C_{\rm PB})+(C_{\rm LS}+C_{\rm PB})(C_{\rm MS}+C_{\rm PA})}\cdot V_{\rm ref} \quad (1)$$

where $C_{\rm LS}$ and $C_{\rm MS}$ are the sum of the capacitance in the LSB and the MSB arrays, respectively. The DAC digital input $X = [S_n \ldots S_1]$ with S_j equal to 1 or 0 represents the DAC connecting $V_{\rm ref}$ or *Gnd* for bit n. The $C_{\rm PA}$ and $C_{\rm PB}$ in the denominator cause an overall gain error, while the parasitic capacitor $C_{\rm PB}$ in the numerator correlated with the bit decision of the MSB array causes a ratio mismatch between the MSB array and the LSB array. The effect presented at the output of the ADC is systematic differential-nonlinearity (DNL) errors [8]. A 4-bit example is shown in Fig. 3(a), while the bridge-DAC is built with a 2-bit MSB array and a 2-bit LSB array, where 20% top-plate parasitic capacitance of $C_{\rm LS}$ is included and the DAC is otherwise ideal. Ideally, the ratio between the LSB of the MSB array and the one from the LSB array $V_{\rm out}(0100)$:$V_{\rm out}(0001)$ is 4:1. As there is $C_{\rm PB}$, the ratio increases to 4.6:1. This ratio mismatch causes the systematic DNL of ≈0.6LSB [in Fig. 3(b)] corresponding to the three transition points shown in Fig. 3(c). Each point contains the carry from bits S2 to S3 of DAC's input (e.g., the first transition point 0011 to 0100). The code histogram of the ADC with a sine wave signal input is shown in Fig. 3(d1). There are positive DNL at the digital output codes, where the nonlinearities occur in the DAC. The positive DNL cannot be corrected in the digital domain, and the reason will be explained in Section IV.

The nonlinearities due to the ratio mismatch of the MSB array and the LSB array can be compensated by enlarging the ratio α of C_a. As the total capacitance at the internal node is increased by 20%, C_a should be increased by 1.2 times accordingly, which can be derived as

$$\frac{\alpha C_a}{\alpha C_a + C_{\rm LS} + C_{\rm PB}} = \frac{C_a}{C_a + C_{\rm LS}} \Rightarrow \alpha = 1 + \frac{C_{\rm PB}}{C_{\rm LS}}. \quad (2)$$

The transfer curve of the DAC and the code histogram of the ADC with an α of 1.2 are plotted, respectively, in Fig. 3(c) and (d2), which

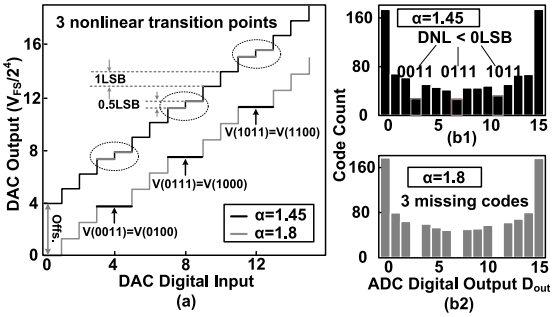


Fig. 4. (a) Transfer characteristic of a 4-bit-bridge DAC. For clarification, offset is added to the case of $\alpha = 1.45$. (b1) Corresponding output code histogram of the 4-bit SAR ADCs with a sine wave input, $\alpha = 1.45$. (b2) $\alpha = 1.8$.

demonstrates the effectiveness of the compensation. However, in practice, the compensation accuracy is difficult to guarantee, as there exist across-chip-variations of $C_{\rm PB}$ as well as the mismatch of the nonunit capacitor C_a. Especially for a high resolution target, the conversion sensitivity to the variance of C_a in a 12-bit SAR ADC is shown in Fig. 3(e), where a (6 bit + 6 bit) bridge-DAC is built and the ADC is otherwise ideal. To guarantee the drop of signal-to-noise distortion ratio (SNDR) of <1 dB, it is required that the variation of C_a is less than ±0.9%.

If the ratio α of C_a increases beyond the compensation value 1.2, the nonlinearities in the DAC appear in the opposite direction. As shown in Fig. 4(a), the nonlinear transition points are decreased by enlarging the ratio α to 1.45. Accordingly, that results in correspondingly negative DNL of −0.5LSB at the output of the ADC, as shown in Fig. 4(b1). Since the DNL is within ±0.5LSB, it is acceptable. However, if the ratio α is further increasing, it will cause DNL less than −0.5LSB or missing codes. In Fig. 4(a), if α is increased to 1.8, the output voltage of the DAC at codes 0011, 0111, and 1011 is equivalent to their corresponding right adjacent codes 0100, 1000 and 1100, which causes missing codes at the output of the ADC. The code histogram of the ADC with an α of 1.8 is shown in Fig. 4(b2). As expected, the three digital codes are missing due to the nonlinearities in the DAC.

IV. Proposed HBRM Calibration

The proposed HBRM calibration corrects the conversion nonlinearities in the digital domain, which does not rely on the compensation accuracy between C_a and $C_{\rm PB}$. The attenuation capacitor C_a is initially designed to be much larger than the compensation value.

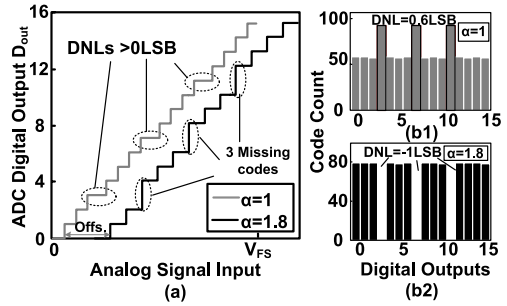


Fig. 5. (a) Transfer characteristics of 4-bit SAR ADC. (b1) Corresponding output code histogram of 4-bit SAR ADC with a ramp input, $\alpha = 1$. (b2) $\alpha = 1.8$.

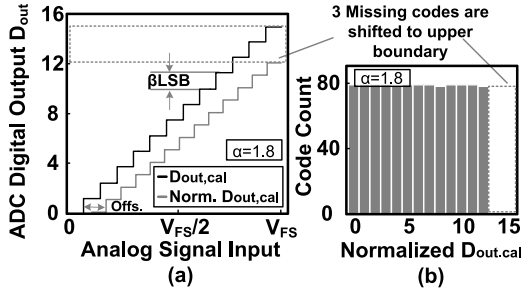


Fig. 6. (a) Calibrated transfer characteristics of 4-bit SAR ADC. (b) Corresponding output code histogram of 4-bit SAR ADC.

Therefore, even when there is variation of C_{PB}, the nonlinearities at the ADC output are systematically negative DNL $<$ 0LSB or missing codes. This is the key requirement to perform the calibration, because the positive DNL cannot be fixed in the digital domain. In Fig. 5(a), the output characteristics of the 4-bit ADC with respect to α of 1 and 1.8 are plotted. When $\alpha = 1$, there exists positive DNL. These codes accumulate a larger number of the hits than the others, as shown in Fig. 5(b1). A larger number of analog inputs are represented by the same digital code, then, impossible to be differentiated in the digital domain. Independently of the way the data is processed, the positive DNLs always exist, as the number of hits cannot be reduced. However, for the case that contains the missing codes in Fig. 5(b2), the number of hits for each code is approximated (more uniformly distributed). Thus, its nonlinearities can be corrected accordingly through the multiplication of all the bits in the LSB array by a gain factor β

$$D_{\mathrm{out,cal}}[B_n \ldots B_1] = \sum_{j=1}^{k} 2^{j+i-1} B_{j+i} + \beta \sum_{j=1}^{i} 2^{j-1} B_j \qquad (3)$$

where B_j equal to 1 or 0 represents the digital output. Once β is applied to the digital output as in (3), the D_{out} at the left adjacent of the missing code will overflow. Therefore, the digital outputs reacquire continuity, as the missed steps are compensated by enlarging the step size to β LSB. Ideally, the bits full-scale in the LSB array is 2^iLSB, which matches with the calibrated full-scale. Accordingly, β can be derived as

$$\beta = \frac{2^i \mathrm{LSB}}{S_m \mathrm{LSB}} \qquad (4)$$

where S_m is the measured step sum. In Fig. 5(a), there exists one missing code in each interval of four codes. Thus, the gain factor β is 4/3, which is applied to the LSB bits B_2 and B_1 in the 4-bit digital output. The calibrated output $D_{\mathrm{out,cal}}$ is shown in Fig. 6(a),

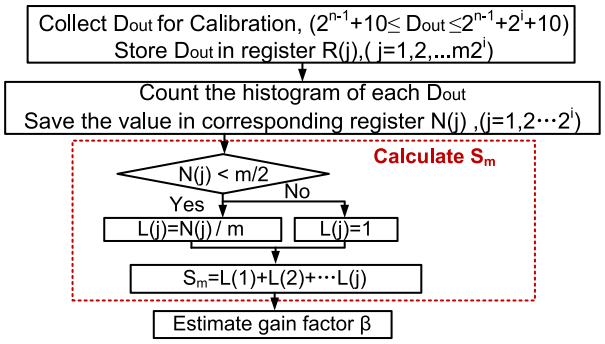


Fig. 7. Flowchart of the HBRM calibration.

where the missed steps are compensated by enlarging the step size to β LSB. By normalizing the calibrated outputs $D_{\mathrm{out,cal}}$ to 1LSB as

$$\mathrm{Norm}(D_{\mathrm{out,cal}}) = \mathrm{fix}\left[\left(\sum_{j=1}^{k} 2^{j+i-1} B_{j+i} + \beta \sum_{j=1}^{i} 2^{j-1} B_j\right)/\beta\right] \qquad (5)$$

the missing codes are shifted to the upper boundary of the output, as shown in Fig. 6(b). The truncation is made at the calibrated output, where the floating number is ignored directly to obtain the final 12-bit digital output.

The flowchart of the HBRM calibration algorithm is shown in Fig. 7. According to (4), the gain factor β is determined by the division of 2^i (ideal step sum in LSB array) and S_m in an n-bit SAR built with $(k + i)$ bit bridge-DAC that utilizes the conventional switching. The S_m is estimated by the codes histogram statistics. Since the nonlinearity has a periodical interval of 2^i, to simplify the statistical analysis, the code range evolves only in 2^i consecutive outputs. As with a sine-wave input, the digital outputs are more uniformly distributed in the midcode region than those at the two sides, the statistical range is set from $D_{\mathrm{out}}(2^{n-1} + 10)$ to $D_{\mathrm{out}}(2^{n-1} + 2^i + 10)$. On the other hand, the calibration accuracy is potentially affected by the capacitor mismatches that are usually worse at the MSB, MSB/2, and 3MSB/2 transitions. In addition, the data range for gain estimation should exclude these transition points. As the calibration collects a total number of $m2^i$ codes within the range, the average count is m. The calibration collects data from D_{out} and stores it in the register $R(j)$. Once the register is full ($j = m2^i$), a histogram of the collected data is made and saved in a register $N(1)$ to $N(2^i)$. Usually, the DNL within 0.5LSB is acceptable, as the conversion may be affected by the other nonidealities, such as capacitor mismatches, reference errors, and noise from comparator and kT/C. Therefore, the threshold for erroneous output is defined as half of the average value $(m/2)$. As mentioned before, the digital outputs contain only the negative DNLs. If $N(j) \geq m/2$ (DNL ≥ -0.5LSB), which indicates less conversion nonlinearity, the code will be counted as 1LSB to S_m. If $0 \leq N(j) < m/2$ (DNL less than -0.5LSB), the code contains the error that is added as a fraction of LSB, where the fraction is defined as $N(j)/m$. The comparison repeats 2^i times. Once the value of S_m is decided according to (4), the gain factor β can be estimated and applied to the i LSBs in the subsequent digital outputs to perform the correction. As β is only applied to the LSBs instead of to the full n bits, the implementation of the digital multiplier can be much more relaxed. On the other hand, the MOM capacitance is insensitive to temperature variations. Once the parasitic nonlinearity is fixed, it is not necessary to track the error in the background. Considering that the calibration accuracy

C_{PB}/C_{LS}	β	SNDR(dB) w/o & w/ Cal.	SFDR(dB) w/o & w/ Cal.
5%	1.39	47.8/69.4	59.7/82.1
10%	1.33	48.9/69.8	61.4/82.5
15%	1.28	50.2/70.4	63.1/83.5
20%	1.23	51.6/70.9	64.8/83.1
25%	1.19	53.2/71.1	67.1/83.2
30%	1.14	55.3/72	68.8/83.7
35%	1.1	57.6/72.5	71.3/84.1
40%	1.07	61.1/73.1	74.8/85.4
45%	1.03	66.5/73.2	79.4/86.7
50%	1	73.6/73.6	87/87

(a)

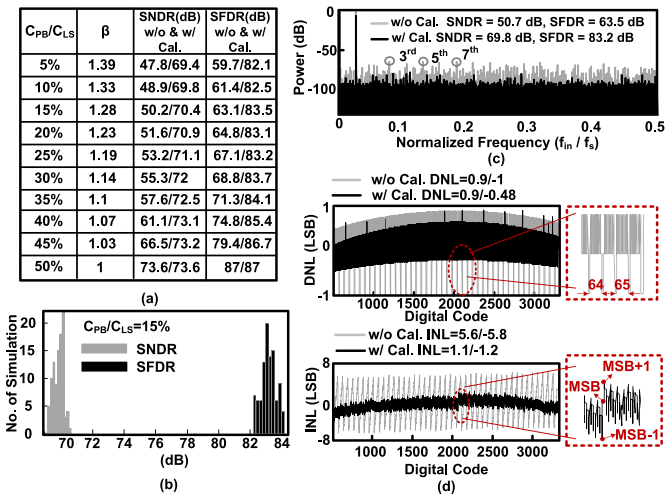


Fig. 8. (a) Variation of C_{PB} versus the dynamic performance in a 12-bit SAR ADC without and with calibration. (b) SNDR and SFDR spread of 100 MC simulations at $C_{PB}/C_{LS} = 15\%$. (c) Corresponding FFT of the digital output. (d) DNL and INL of the digital output.

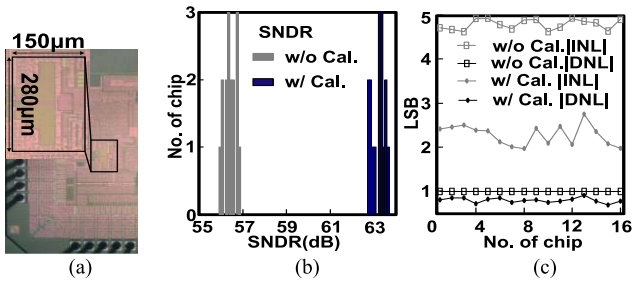


Fig. 9. (a) Chip photograph of SAR ADC. (b) Measured SNDR of total 16 chips. (c) Measured DNL and INL of total 16 chips.

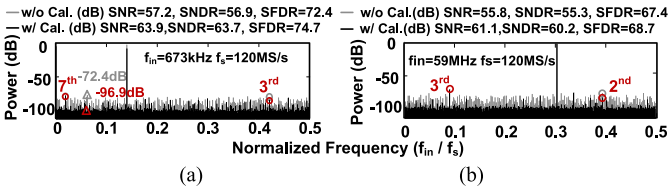


Fig. 10. Measured FFT of the digital output (decimated by 25) at (a) dc input and (b) Nyquist input.

is potentially affected by the noise, the calibration can be repeated several times to obtain an average value of β. The iteration should be set as $\geq$5.

To verify the HBRM calibration method, behavioral simulations were performed, which modeled the conversion nonlinearities in a 12-bit SAR built with (6 bit + 6 bit) bridge-DAC. The values of the unit capacitors are Gaussian random variables with a standard deviation of σ ($\Delta C/C = 0.1\%$). The attenuation capacitor is set as 48/31C ($\alpha = 1.5$), and the top-plate parasitic capacitance varies from 5% to 50%. Fig. 8(a) lists dynamic performance of 100 times Monte Carlo (MC) simulation with the average results before and after calibration. As the ratio α is set as 1.5, it can cover at most 50% parasitic variation. As also shown in Fig. 8(a), a corresponding gain factor β can be estimated by the calibration scheme to compensate the nonlinearities caused by the parasitics. Regarding the case of $C_{PB}/C_{LS} = 15\%$, the spread of SNDR spurious-free dynamic range (SFDR) of 100 times MC simulation after calibration are shown in Fig. 8(b), the variations are within 2 dB. The corresponding output spectrum before and after calibration is plotted in Fig. 8(c). The ratio mismatch gives rise to odd harmonics and spurs that limit the SNDR and to 50.7 and 63.5 dB, respectively. After calibration, the spurs are removed and the odd harmonics are suppressed to lower than -83 dB, and thus improving the SNDR by 19.1 dB. The static performance is shown in Fig. 8(d); before calibration, the DNL contains a bunch of missing codes. The nonlinearities happen periodically with an interval near 64 codes, which is expected, as the LSB array in DAC contains 6 bit. The nonlinearities also lead to a corresponding saw tooth pattern in integral nonlinearity (INL), which is larger than 5LSB. After calibration, the missing codes in DNL are all corrected and the |INL| is suppressed to $\leq$1.2LSB. According to the switching nature, the MSB is determined directly by comparing the difference of two differential input signals that is DAC mismatch uncorrelated. Therefore, the INL is minimized in the middle and turns worse at the steps below and above it [8].

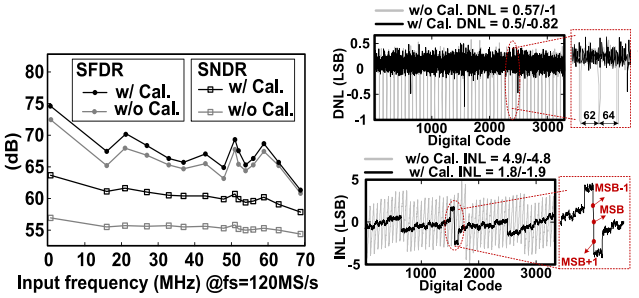
A. DAC Array

An 11-bit (6 bit + 5 bit) bridge-DAC is implemented, where 1 bit is reduced using the V_{cm}-based switching technique [3]. In this design, the output equivalent capacitance of the DAC is 64C, and the unit capacitance is 20 fF, and thus resulting in a total sampling capacitance of 1.28 pF (single ended). The proposed HBRM calibration is verified in two 12-bit SAR ADCs. To evaluate the calibration effectiveness to the capacitor mismatch and across-chip variations, the value of C_a in two designs is different, while the ADC otherwise is the same. The ideal value of C_a should be 20.6 fF. The first design covers the parasitic range of 20% by implementing a C_a of 25 fF ($\alpha_2 \approx 1.2$), and the measured results were reported in [6], therefore, it is not illustrated here. Only the measured results of the second design are reported and analyzed, where $C_a = 27$ fF is implemented to guarantee a larger correction range up to 30% of the parasitic capacitance C_{PB} ($\alpha_1 = 27/20.6 \approx 1.3$).

V. Measurement Results

The 12-bit SAR ADC was fabricated in a 1P9M 90-nm CMOS process with MOM capacitors. Fig. 9(a) shows the die photograph of the design with C_a of 27 fF; the active area is 0.042 mm^2. The analog power consumption is 0.8 mW and the digital power including the SAR logic and clock generator is 2.4 mW. The total power consumption is 3.2 mW at 120 MS/s from 1.2 V supply. The digital outputs are postprocessed according to the HBRM calibration algorithm. The calibration is controlled by MATLAB running on a PC, but the controller could be integrated in VHDL. The digital gate count of the calibration algorithm is ~5k and the estimated place and routed area is 0.14 mm^2 with the operating power of 2.3 mW at 120 MHz. The calibration is based on 1280 data outputs; thus, the required calibration time is $\approx$11 μs. Fig. 9(b) and (c) shows the measured dynamic and static performance of the total available 16 chips at dc input and 120 MS/s sampling rate. The achieved average SNDR before and after calibration is 56.4 and 63.4 dB, respectively. The average DNL and INL after calibration are 0.81LSB and 2.3LSB, respectively.

Fig. 10 shows the measured fast Fourier transform (FFT) at 673 KHz and at Nyquist frequency (59 MHz) with a conversion rate of 120 MS/s. Before calibration, the ratio mismatch causes a bunch of spurs spreading among the whole spectrum and the rise to the third harmonic, which matches the effect exhibited in the behavioral of Fig. 8(c). This limits the SNR and the SFDR to 57.2 and 72.4 dB, respectively. Once the calibration is active, the spurs are removed. The spur limiting the SFDR before calibration is



(a) (b)

Fig. 11. Measured performances of the SAR ADC without and with calibration. (a) Measured dynamic performance. (b) Measured static performance.

TABLE I
SUMMARY OF PERFORMANCE AND COMPARISONS

	[1]	[7]	1st SAR [6] (Ca=25fF)	2nd SAR (Ca=27fF)
Architecture	SAR	SAR	SAR	SAR
Technology (nm)	130	90	90	90
Resolution (bit)	12	12	12	12
Sampling Rate (MS/s)	45	50	120	120
Supply Voltage (V)	1.2	1.2	1.2	1.2
Input Swing (V_{p-p})	2.4	2.4	2	2
SNDR (dB)	68.3	66.5	64.3	63.7
Area (mm^2)	0.059	0.046	0.042	0.042
Power (mW)	2.8	3.3	3.2	3.2
FOM=Power/$2^{ENOB@Nyq.}*f_s$ (fJ/conv-step)	36	45	28	32
Calibration	Off-chip	Off-chip	Off-chip	Off-chip

suppressed to lower than −96.9 dB. In addition, the third harmonic is below −81 dB. Consequently, both SNR and SNDR are improved by near 6.7 dB. The seventh harmonic on the left-hand side dominating the SFDR is potentially caused by the capacitor mismatches rather than the ratio mismatch of the bridge-DAC. As the input frequency increases to Nyquist, the sampling distortions originate the third harmonic that dominates the SFDR before and after calibration. Even though the SFDR is slightly improved by 1.3 dB, the SNDR can be increased by 4.9 dB. Fig. 11(a) shows the measured dynamic performance. The measured static performances with and without the HBRM calibration are shown in Fig. 11(b). Based on the measurement, the DNL before calibration has the systematic comb-alike pattern due to a large number of missing codesthat are periodic and have an interval of near 64 codes. Since 6 bits are determined in the LSB array, the nonlinearities are expected and match correctly with the behavioral model in Fig. 8(d). In addition, the INL contains the systematic sawtooth pattern that reflects the intrinsic conversion nonlinearity relevant to the capacitor mismatches due to the use of the split DAC. The effect is similar to what is shown in Fig. 8(d). When the calibration is active, the missing codes in DNL are all removed and the INL is improved to within 2LSB, correspondingly. According to the switching nature of the V_{cm}-based approach, the INL is minimized in the middle that is −0.12LSB, and becomes higher at the steps below and above the MSB transitions, while for the DNL, it should be maximized at the MSB and MSB + 1 transitions [8]. Since the DNL measurement at near MSB, MSB/2, and 3 MSB/2 transition points is larger, the DAC settling errors get worse over there. When the bigger capacitors are charged or discharged, this causes larger reference ripples. Table I summarizes and compares the overall measured performance of the two designs with the state-of-the-art linearity calibrated high-resolution and medium-speed SAR ADCs.

VI. CONCLUSION

This brief proposed a linearity calibrated high-speed SAR ADC. The conversion nonlinearity in a capacitive bridge DAC is analyzed and an HBRM calibration is presented in detail. The calibration suppresses the spurs due to ratio mismatches in DAC that improves the SNR of the ADC. The static performances are also significantly improved and the missing codes in DNL are removed. Moreover, the calibration is performed in the digital domain, which achieves high accuracy and large calibration range. The solution does not depend on the matching between the attenuation and unit capacitors which relaxes the implementation effort. The solution was verified in two designs to demonstrate the calibration sensitivity and effectiveness to across-chip variations and capacitor mismatches.

REFERENCES

[1] W. Liu, P. Huang, and Y. Chiu, "A 12 b 22.5/45 MS/s 3.0 mW 0.059 mm^2 CMOS SAR ADC achieving over 90 dB SFDR," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 380–381.

[2] P. Harpe, E. Cantatore, and A. van Roermund, "An oversampled 12/14 b SAR ADC with noise reduction and linearity enhancements achieving up to 79.1 dB SNDR," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 194–195.

[3] Y. Zhu *et al.*, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[4] C.-C. Liu *et al.*, "A 10 b 100 MS/s 1.13 mW SAR ADC with binary-scaled error compensation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 386–387.

[5] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto, "A 10 b 50 MS/s 820 μW SAR ADC with on-chip digital calibration," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 384–385.

[6] Y. Zhu, C.-H. Chan, U Seng-Pan, and R. P. Martins, "A 10.4-ENOB 120 MS/s SAR ADC with DAC linearity calibration in 90 nm CMOS," in *Proc. IEEE A-SSCC*, Nov. 2013, pp. 69–72.

[7] W. Liu, P. Huang, and Y. Chiu, "A 12-bit 50-MS/s 3.3-mW SAR ADC with background digital calibration," in *IEEE CICC Dig. Tech. Papers*, Sep. 2012, pp. 1–4.

[8] Y. Zhu *et al.*, "Split-SAR ADCs: Improved linearity with power and speed optimization," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 372–383, Feb. 2014.

[9] C.-H. Chan, Y. Zhu, U.-F. Chio, S.-W. Sin, U Seng-Pan, and R. P. Martins, "A reconfigurable low-noise dynamic comparator with offset calibration in 90 nm CMOS," in *Proc. IEEE A-SSCC*, Nov. 2011, pp. 233–236.