A 6 b 5 GS/s 4 Interleaved 3 b/Cycle SAR ADC

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***Abstract*—This paper presents a 4× time-interleaved 6-bit 5 GS/s 3 b/cycle SAR analog-to-digital converter (ADC). Hardware overhead induced by a 3 b/cycle architecture is eased by an interpolation technique where around 1/3 of the hardware is saved. In addition, complicated switching controls are simplified with a proposed fractional DAC array switching scheme, thus reducing the design complexity and the hardware burden. A boundary detection code overriding (BDCO) is introduced to reduce error probability at the large error magnitude, by utilizing the extended time when the comparator is at reset and the DAC at settling. The floorplan of the front-end is optimized for important interleaving clock distributions, and a master-clock-control bootstrapped-switch technique is adopted to suppress the timing-skew effect among the channels. The unit capacitor has been designed to suit for the DAC structure which allows top-plate sharing in both directions, plus, the offset is calibrated on-chip with a clocking variable biasing transistor pair at the latch. Measurement results show that the prototype can achieve 5 GS/s with a total power consumption of 5.5 mW at 1 V supply in 65 nm CMOS technology. Besides, it exhibits a 30.76 dB SNDR and 43.12 dB SFDR at Nyquist, which yields a Walden FoM of 39 fJ/conversion-step.**

***Index Terms*—Analog-to-digital conversion, interleaving, interpolation, multibit/cycle SAR, offset calibration.**

I. Introduction

BOTH WIRELINE and wireless communication systems keep increasing the demand on bandwidth for higher data transfer rate. Applications like in 60 GHz-band receivers and serial links induce challenges for designing easily driven, power efficient and compact analog-to-digital converter (ADC) interfaces. A possible range of ADC specifications is 6–8 bits and up to several GS/s. Due to the benefits granted by technology scaling, both operation frequency and energy efficiency are improved in highly digital ADC architectures, which allow very energy-efficient designs as ∼40 fJ/conversion-step Walden FoM with 2.2 GS/s [1].

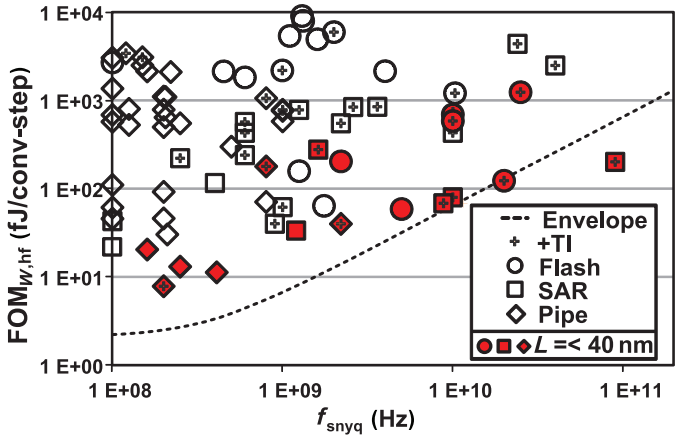

Fig. 1. ADC performance survey.

Especially for circuits consuming mainly dynamic power, both intrinsic parasitic and supply voltage are shrinking, which implies a drastic improvement on their power consumption. By inspecting the recent state-of-the-art ADC survey [2] as illustrated in Fig. 1, it can be observed that all energy-efficient designs in these ranges of specifications are implemented in advanced technology nodes at or below 40 nm. On the other hand, advanced nodes are costly while an architectural optimization can be more general for different scenarios under various technologies. From the survey, it can be noticed that most of the power efficient designs with these specifications are composed of flash or SAR ADC combining with time interleaving. The SAR ADC is a well-known energy-efficient architecture while the speed of SAR ADCs can be further improved with the comparator interleaving [3], loop-unrolled asynchronous loop [4], or the multibit per cycle [5]. The flash ADC is known as the fastest ADC architecture but power hungry. By adopting interpolation [6] or calibration [7], outstanding energy efficiency can also be accomplished under advanced technology nodes. In a standalone flash or SAR architecture, speed and energy efficiency are still limited due to their inherent characteristics; therefore, they are often combined with time interleaving to achieve a breakthrough. More details of the architectural analysis can be found in Sections II-B and II-C. Time interleaving can be a very effective way to increase the sampling rate of the ADC, but it induces extra design complexity and conversion nonidealities especially with large numbers of interleaving channels. Even though various calibration techniques for timing, gain, and offset error have been introduced [8]–[10], the power required for the digital gain and timing corrections is prohibitive at 6 b resolution.

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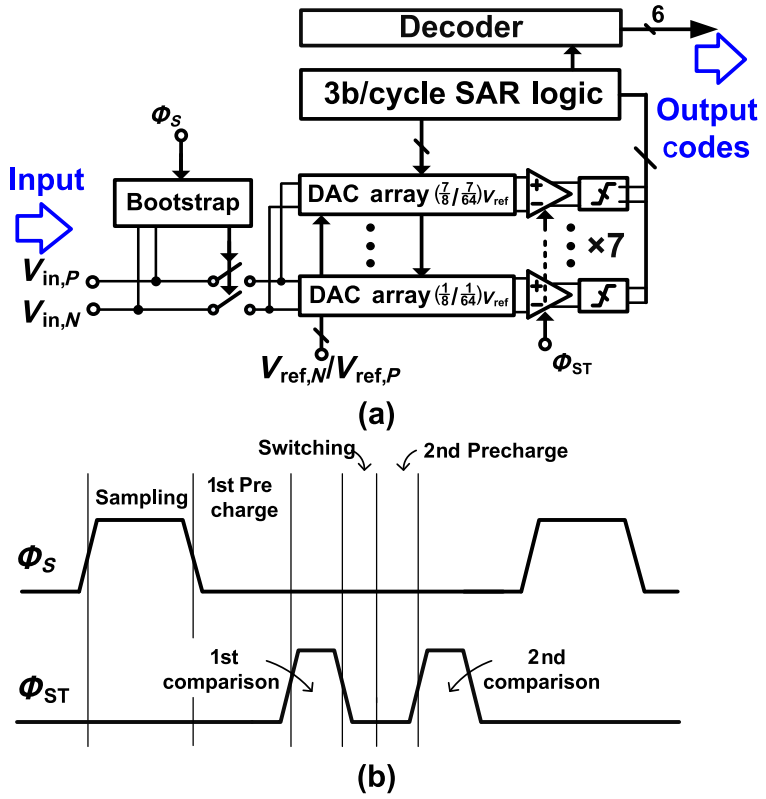

Fig. 2. ADC (a) architecture and (b) timing diagram with time allocation.

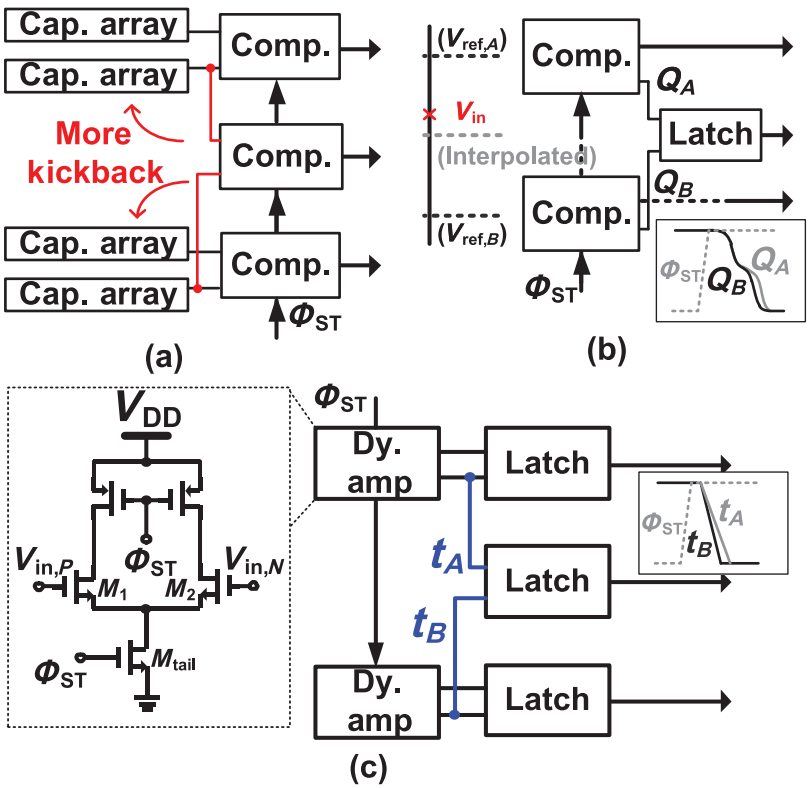

Fig. 3. Interpolation methods at outputs of (a) capacitor array, (b) latch, and (c) dynamic preamp.

This work proposed a combination of a 3 b/cycle SAR architecture with time interleaving [11] which targets a 6 bit 6 GS/s specification. Rather than applying complicated timing-skew calibration, the timing error is suppressed by a proper layout floorplan and circuit techniques with optimizing the number of channels. The hardware overhead and circuit complexity are eased with the presented techniques, which include dynamic preamplifier interpolation, DAC structure and

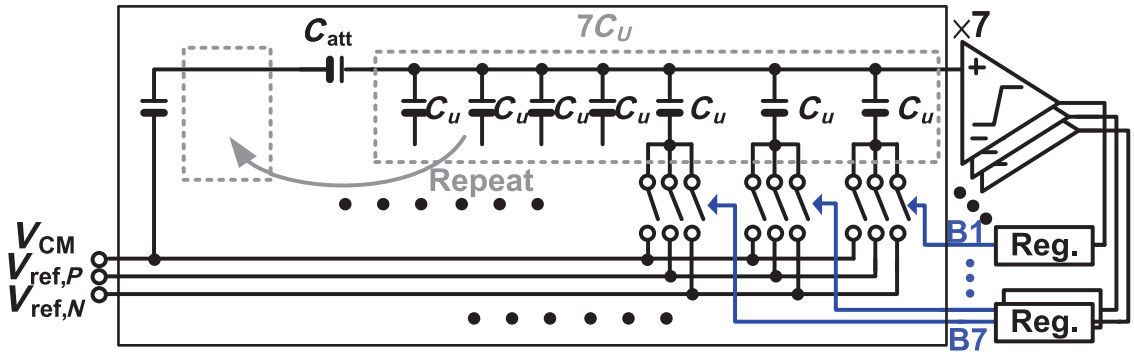

Fig. 4. Circuit detail of conventional 3 b/cycle segmentation VCM-based switching in a 6 b split DAC structure.

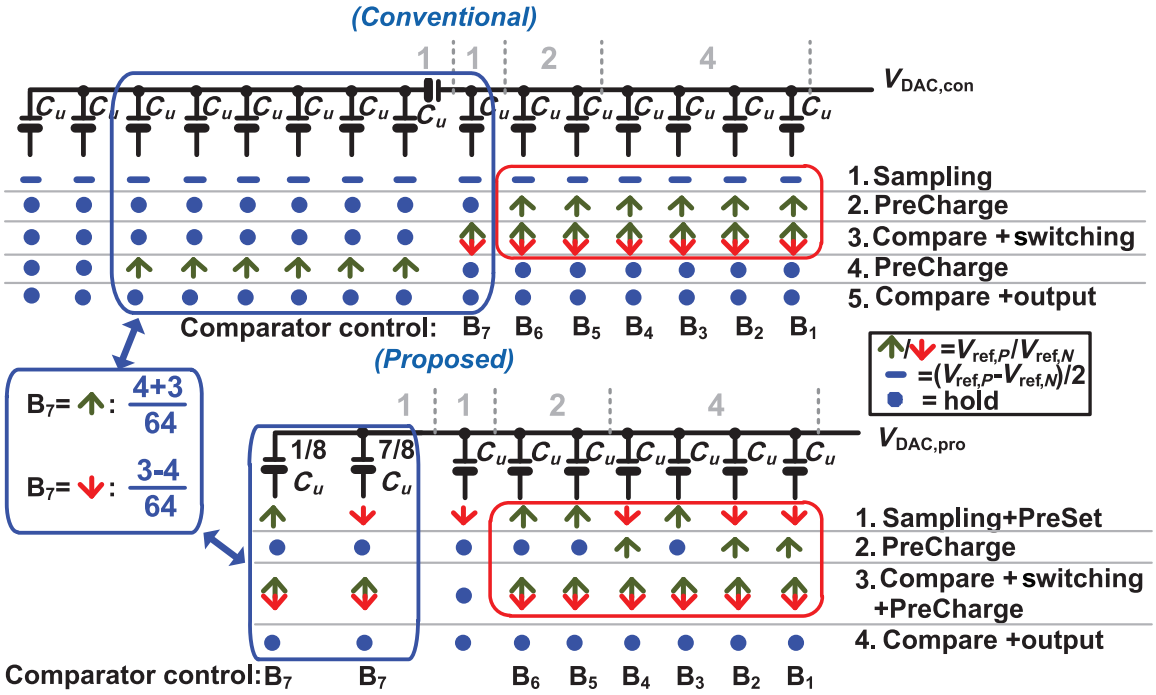

Fig. 5. Comparison between the proposed and the conventional switching operation.

switching simplification, boundary detection code overriding (BDCO), and master-clock-control bootstrapped-switch. As observed during the measurements, the prototype can achieve 5 GS/s at 1 V supply and up to 6 GS/s at 1.2 V supply with SNDR above 30 dB at Nyquist. The power consumption is as low as 5.5 mW with a Walden FoM of 39 fJ/conversion-step. The organization of this paper is as follows. The ADC structure and a generalized architectural analysis are introduced in Section II. Section III discusses various hardware and complexity reduction circuit techniques. Section IV describes the BDCO scheme. Circuit structures, such as offset calibration and DAC implementation, are detailed in Section V. Measured results are reported in Section VI and finally the conclusion is drawn in Section VII.

II. 3 B/Cycle SAR ADC Architecture

Fig. 2(a) illustrates the block diagram of the conventional 3 b/cycle SAR ADC architecture. It consists of 7 DAC arrays, dynamic preamplifiers and latches, a 3 b/cycle SA logic, a sampling front-end with bootstrapped-switches and an encoder. Fig. 2(b) shows its timing diagram. During the sampling phase Φ_s, the differential input signals ($V_{\text{in},P}$ and $V_{\text{in},N}$) are sampled on the DAC capacitors arrays. Then, 7 DACs precharge to their corresponding first cycle's reference voltages ($1/8{-}7/8V_{\text{ref}}$), where the sampled signal is subtracted by corresponding references in the DACs and the results are passed to the comparators. The comparators give their decisions at $\Phi_{\text{ST}} = 1$ to control DACs to switch a successive-approximated residue via the SAR logic. Next, the precharging operation repeats but for the second cycle's reference voltages ($1/64{-}7/64V_{\text{ref}}$) which is followed by the second comparisons. Each comparison resolves 3 bits resolution and all comparators' outputs are consequently decoded through the decoder to obtain a binary output. It is worth noting that the hardware complexity is growing exponentially with the number of resolving bits per cycle in a multibit SAR ADC, similar to the flash. Furthermore, the routing parasitic, due to the large amount of hardware in the 3 b/cycle, also degrade the energy efficiency. Even though a 3 b/cycle structure may not seem to be power efficient due to

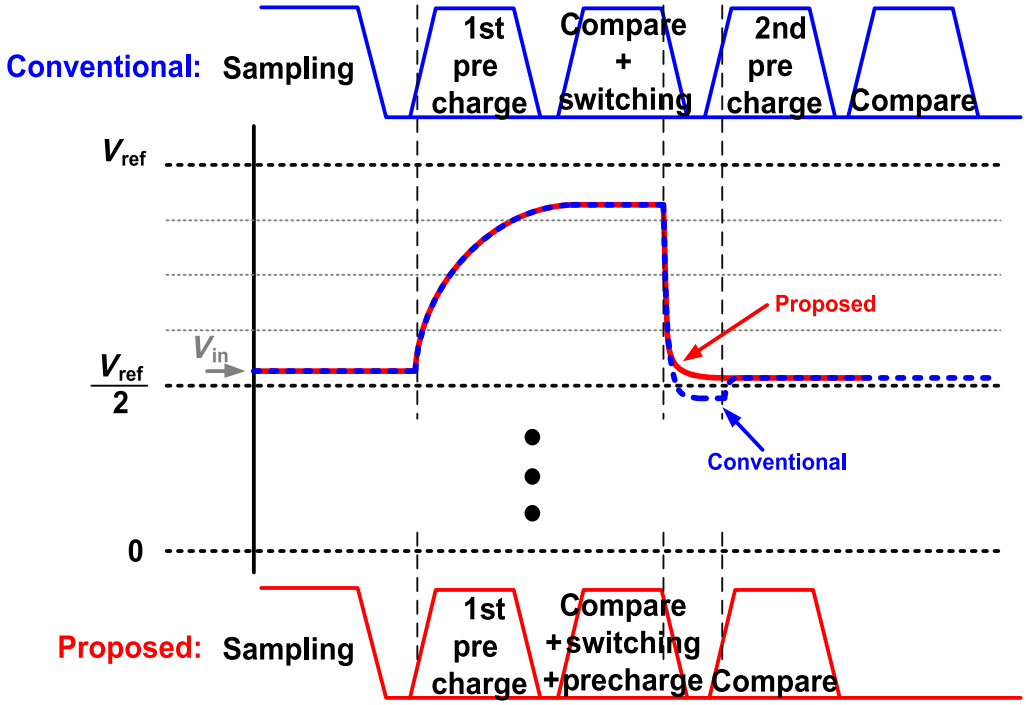

Fig. 6. Signals behavior and timing diagram of the proposed and the conventional switching operation.

the hardware overhead, it relaxes the scaling of comparators and logics toward higher speed which can lead to actually better energy efficiency than the 1 b/cycle SAR ADC. On the other hand, hardware reduction techniques are necessary in order to maintain the benefits of the 3 b/cycle SAR architecture. The interleaving technique is also adopted in this design to further increase the sampling rate of the ADC.

III. Hardware and Operation Optimization

As there are large hardware burdens and complicated control circuitries in the 3 b/cycle SAR architecture, simplification in both operation and implementation is necessary for a good energy efficiency.

A. Interpolation at the Dynamic Amplifier's Output

Interpolation can effectively reduce the amount of hardware in the multibit SAR ADC, which can be achieved at the DACs' outputs [12] or the latches' outputs [13]. Nevertheless, the DAC interpolation leads to double kickback noise [Fig. 3(a)] from the comparators to each DAC and eventually limits the total capacitance in the DAC arrays. Alternatively, latch interpolation does not give rise to more kickback, but the interpolated latches become slow when the input is close to their interpolated thresholds as shown in Fig. 3(b). From [14], it can be found that the regeneration time of the latch depends on the input difference in a natural log scale. Since the interpolating latch only starts after the preceding latches have finished, the delay is inevitably increased. Here, the interpolation is obtained at the outputs of the dynamic preamplifiers, which does not induce more kickback and also has less speed penalty than the latch interpolation method. Fig. 3(c) shows the interpolation setup

TABLE I
Comparison Between Conventional and Proposed Switching

	Conv.	Pro.
Number of control bits	13	8
Number of control switches	33	16
Number of voltage Lv.	3	2
Number of unit cap	16	8
Number of phases	5	4

and the circuit schematic of the adopted dynamic preamplifier topology. It consists of a reset pair of PMOS, a input pair of NMOS ($M_{1,2}$), and a clocking tail transistor (M_{tail}). Its delay when $\Phi_{\text{ST}} = 1$ can be expressed as (based on the square law model with a velocity saturation assumption)

$$\text{Delay}_{\text{pre}} \propto R_{\text{eq},M1} C_L,$$
$$\text{where } R_{\text{eq},M1} \propto \frac{1}{(V_{\text{in}} - V_{s1} - V_{\text{Tn}} - V_{D,\text{SATn}}/2)} \quad (1)$$

where $R_{\text{eq},M1}$ is the equivalent resistance of M_1 when M_{tail} is enabled, and V_{s1} and $V_{D,\text{SATn}}$ are the source voltage and the saturation voltage of M_1, respectively. V_{Tn} is the threshold voltage of the NMOS transistor. It can be realized from (1) that the delay of the dynamic preamplifier is (approximately) inversely proportional to the input; therefore, the input difference does not have significant impact on the interpolation speed.

Due to the interpolation, the DACs and the dynamic preamplifiers are reduced from 7 to 4 with only two extra dummy latches (for balancing the load at the preamplifiers' outputs). It is worth noting that the logics and the controls of the DACs

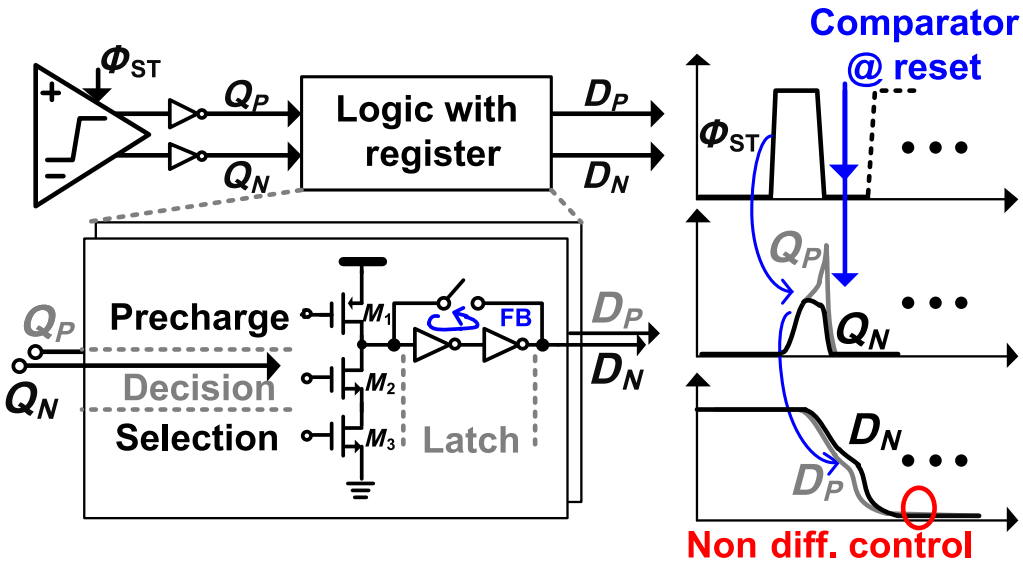

Fig. 7. Signals' behaviors of the logic circuit when the comparator's input difference is small and circuit details.

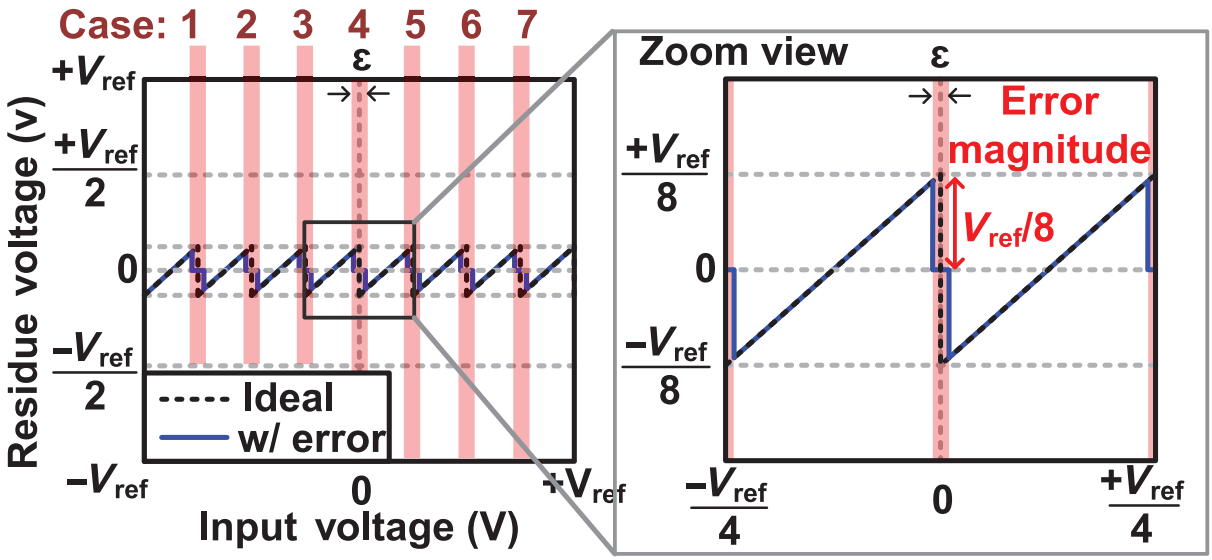

Fig. 8. Ideal and error (dot line) residue transfer curves of 6 bit 3 b/cycle SAR with nondifferential controls of the DACs in the red regions.

(for different precharging values) are also saved as well as achieving input capacitance reduction. Eventually, the power consumption, circuit complexity, and core area are significantly reduced and enable an energy-efficient 3 b/cycle SAR architecture. It is also worth noting that the interpolating technique causes a drifted common mode at the interpolated latches. In the proposed scheme, it leads to a faster slope at the input of the interpolated latches which increases the speed of the latch and induces more noise. However, as the noise from the latch can be suppressed by the dynamic preamplifier, it does not induce a large noise overhead for a 6 bit design. On the other hand, since this drifted slope is not sensed during calibration, a residual offset voltage is remained from the latch. In the simulation, it can be found the input-referred 3σ residual offset is as small as ± 1 mV due to the gain of the dynamic amplifier.

B. Reduced Reference Segmentation VCM-Based Switching and DAC Arrays

Fig. 4 shows the circuit details of the conventional VCM-based [15] segmentation switching for multibit SAR ADC [16] in a split DAC structure. All the capacitors are arranged in a single unit; therefore, the outputs of the comparators can directly control the DACs (B1–B7) without extra decoding logic and delay. On the other hand, it requires different control switches and logics for the precharging, switching, and sampling operation. It also needs three voltage levels ($V_{\text{ref},P}$, $V_{\text{ref},N}$, and V_{CM}) among different operation phases. Those switches, voltage levels, and routing of the control signals create a complex matrix which causes undesired coupling and lowers the SA loop speed with more power consumption, especially for the 3 b/cycle SAR architecture. Two simplifications are made in the DAC

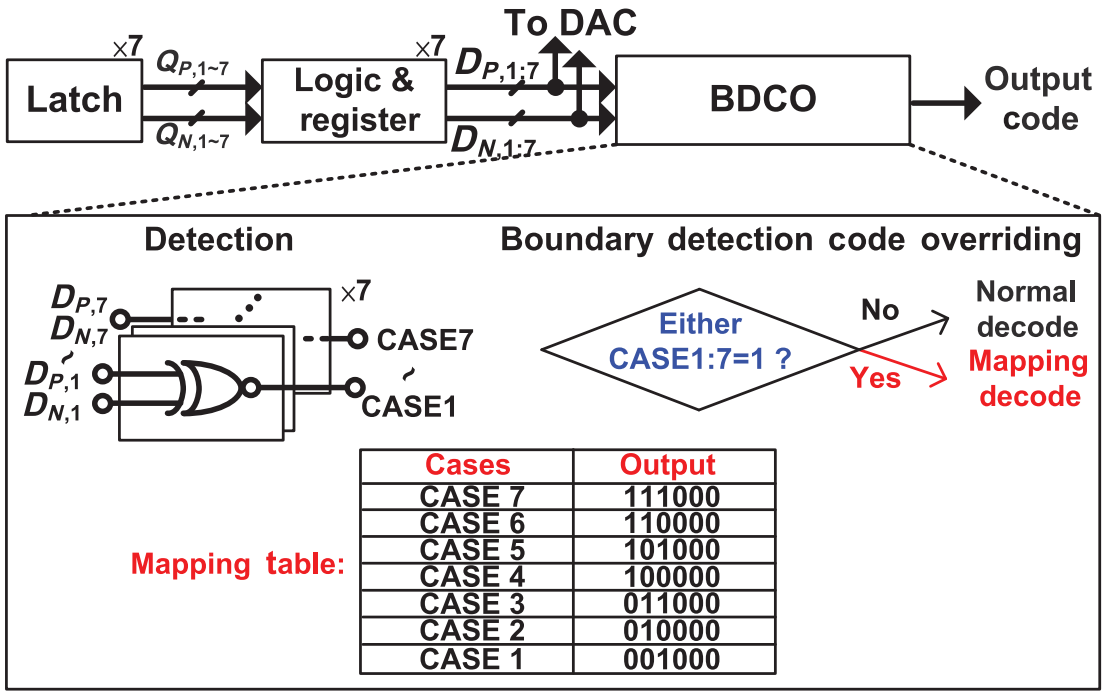

Fig. 9. BDCO scheme with circuit details, logic flow, and mapping table.

and switching logic in order to save hardware and operation phases. First, rather than using a full binary DAC or a split DAC structure, this design adopts fractional capacitors in the LSB array. Even though the fractional capacitors experience certain variations due to their small value, they only degrade by a small amount of the SNDR due to the small contribution from the last LSBs. Based on this design, the matching (σ_C/C) has to vary by about 6% in order to cause around a 3 dB drop in the SNDR for 6 bit, which is quite large when considering that the matching of the MOM capacitor is usual around 1% in the adopted process. Second, rather than reset the bottom-plates at $(V_{\text{ref},P} - V_{\text{ref},N})/2$ during sampling, they preset to $V_{\text{ref},P} - V_{\text{ref},N}$ accordingly. The comparison between the conventional and proposed switching operation is explained next in detail.

Fig. 5 shows an example of the DAC switching with a $7/8 \times V_{\text{ref}}$ reference voltage. For the first six capacitors (with comparators' controls B1–B6) during sampling phase (Step 1), all the bottom-plates of the DAC are reset to $(V_{\text{ref},P} - V_{\text{ref},N})/2$ conventionally; while three of them are preset to $V_{\text{ref},P}$ and others to $V_{\text{ref},N}$ in the proposed switching. Since the top-plate sampling technique is adopted in this design, the preset values do not affect the sampling operation, but such preset sequence allows maintaining the same functionality as the conventional switching which can be shown later. In the first precharging phase (Step 2, where the input shift with the corresponding reference voltage), only the capacitor preset to $V_{\text{ref},N}$ is switched to $V_{\text{ref},P}$ while the others remain unchanged in the proposed scheme; therefore, it matches to the operation of the conventional structure with six capacitors switching from $(V_{\text{ref},P} - V_{\text{ref},N})/2$ to $V_{\text{ref},P}$ and removes the need of $(V_{\text{ref},P} - V_{\text{ref},N})/2$ voltage. Next (Step 3), the comparators give their decisions and control the DAC to generate a residual voltage. Since the output controls of the comparators are in thermometer, the preset sequence (in Step 1) also guarantees the same result between the conventional and the proposed method. For instance, if the outputs of B1–B6 are 110000, the conventional switching gives a residual voltage of: $V_{\text{in}} + (2 \times 1/2 \times (V_{\text{ref},P} - V_{\text{ref},N}) - 4 \times 1/2 \times (V_{\text{ref},P} - V_{\text{ref},N})) = V_{\text{in}} - (V_{\text{ref},P} - V_{\text{ref},N})$ regarding the switching operation from Steps 1) to 3); and the residual voltage of the proposed scheme is: $V_{\text{in}} + (2 \times (V_{\text{ref},P} - V_{\text{ref},N}) - 3 \times (V_{\text{ref},P} - V_{\text{ref},N})) = V_{\text{in}} - (V_{\text{ref},P} - V_{\text{ref},N})$. Thus, both methods converge to an identical residue. Afterward, the controls of the bottom-plates hold until the next sample.

For the remaining capacitors (with comparator's control B7 and/or the split LSB capacitors), similarly a certain sequence is preset during sampling in the proposed switching and the conventional one just reset to $(V_{\text{ref},P} - V_{\text{ref},N})/2$ (Step 1). During first comparison and second precharging operation in the proposed scheme (Step 3), the 7/8 fractional capacitor switches from the preset value $(V_{\text{ref},N})$ to $V_{\text{ref},P}$, and the 1/8 fractional capacitor remains unchanged if $\text{B7} = 1$. While if $\text{B7} = 0$, then the 1/8 capacitor switches from $V_{\text{ref},P}$ to $V_{\text{ref},N}$, and the 7/8 capacitor keeps constant. It is worth emphasizing that the preset sequence with the fractional value of the capacitors not only guarantees an identical functionality as the conventional operation but also saves an extra phase. In this example with a $7/8 \times V_{\text{ref}}$ reference voltage, the DAC moves by $+7/64$ for $\text{B7} = 1$ with precharging, and moves by $-1/64$ for $\text{B7} = 0$ with precharging in the conventional scheme (Steps 3–4). Therefore, the fractional values of 1/8 and 7/8, and the preset sequence are arranged accordingly in the proposed switching to match the conventional operation.

The signals' behavior and the time diagram of the conventional and proposed switching are given in Fig. 6. In this

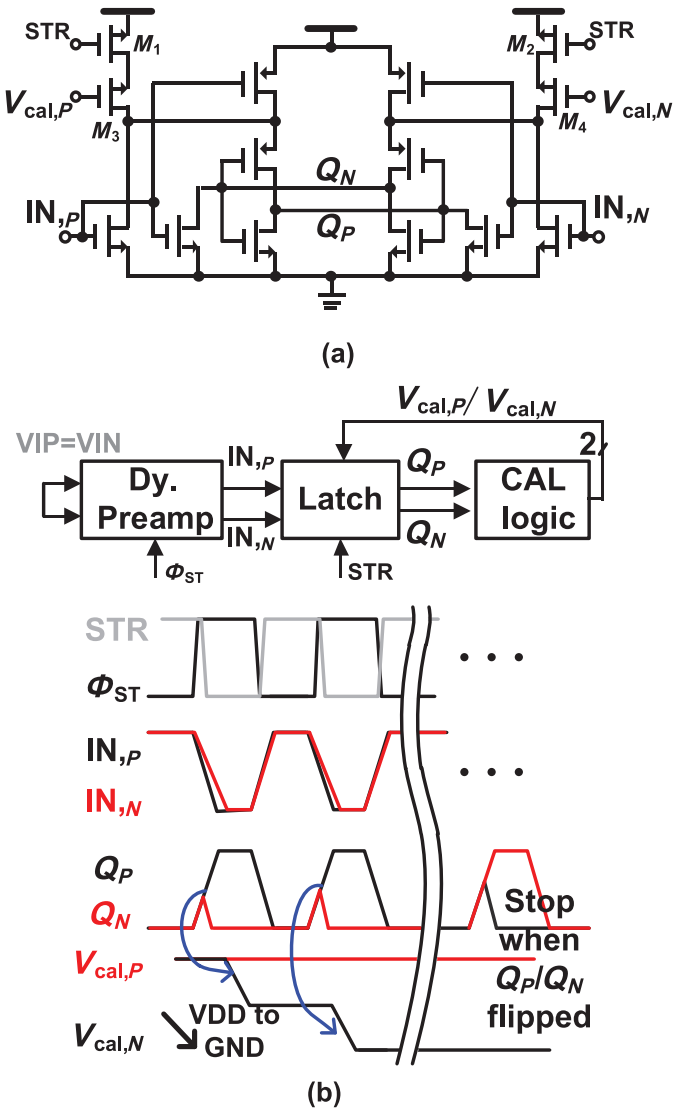

Fig. 10. Offset calibration technique with (a) circuit schematic of adopted latch and (b) calibration process and signals' behaviors.

example, the top-plate voltage of the DAC with a $7/8 \times V_{\text{ref}}$ reference voltage is illustrated with a certain input (V_{in}). After the sampling and first precharge operation, both methods have an identical timing and the same top-plate voltage. Next, the comparators give their decision which set B1–B7 to "0" in this example. The proposed switching scheme directly converts to the final output which combines the residual switching and precharging operation, while the conventional one requires two steps to accomplish the same result.

It is worth noting that the benefits of the VCM-based switching are better linearity, constant common-mode voltage for the comparator and less switching energy when comparing with the set-and-down and conventional scheme. However, as targeting to only 6 bit resolution in this design with a small value of the DAC, the power consumption of the DACs switching consumes only less than 2.5% of the total which becomes a minor concern. While a simple and fast operation as well as a constant common-mode voltage is the main goal, a simplified VCM-based switching method for multibit is proposed. The number of control bits, control switches, voltage levels, unit capacitors and operation phases in the proposed implementation are compared with the conventional structure, as listed in Table I. It can be observed that the number of control bits and control switches are significantly reduced by the proposed method (more than half). The V_{CM} voltage level is removed in order that all the control switches experience large overdrive voltages for high speed. The number of unit capacitors is cut by half and one phase of operation is saved.

IV. Boundary Detection Code Overriding

For low-power and high-speed purposes, a dynamic logic family is often adopted in the high-speed SAR logic implementation [17], [18]. Besides, the precharging, selection, switching and latch function can be combined together with one dynamic logic gate in this design. Nevertheless, dynamic logic is not robust to a condition when the input difference of the comparator is small and its outputs are interpreting at the metastable state.

A. Error Characteristic

The adopted logic circuit and its signal behaviors with small input difference at the comparator are depicted in Fig. 7. The dynamic logic consists of three transistors; one for pull up and two for pull down. The precharging controls go through PMOS (M_1); the decision from the comparator employ to M_2, and M_3 is for selection purpose and to identify the working cycle. A latch [by extra feedback loop (FB)] is enabled after the decision of the comparator is propagated.

This circuit block provides both logistic and latch functions to control the differential DAC performing the SAR switching. Assuming that the comparator input is small, its outputs do not have enough time to regenerate a valid difference which produces nondifferential controls to the differential DAC (D_p, D_n). Consequently, the residue of the DAC becomes zero in this condition and the error amplitude can be illustrated in Fig. 8. The dot line represents the ideal residual transfer curve and the blue line contains error. The red regions represent the case when the input of the comparator is small and nondifferential controls to the DAC are propagated. Since there are seven comparisons in the first cycle, seven cases are indicated. With a zoom-in view of case 4, it can be seen that the error magnitude caused by nondifferential controls can be as large as $V_{\text{ref}}/8$ which is 8 LSB in this design. The error region ε can be estimated with the following equation [14]:

$$|\varepsilon| \leq 2 \times \frac{V_{\text{valid}}}{A_{\text{tot}} \exp\left(T_{\text{comp}}/\tau_{\text{reg}}\right)} \tag{2}$$

where V_{valid} is the valid-logic-level, A_{tot} is the total gain from the latch (before regeneration) and logic propagation, T_{comp} is the available time for the regeneration, and τ_{reg} is the regeneration time constant. It can be highlighted that by either increasing T_{comp} or by lowering τ_{reg}, the ε can be effectively reduced. In the high-speed SAR ADC design, T_{comp} is often short while lowering τ_{reg} leads to degradation of the energy efficiency as explained in Section II. Other solution for suppressing

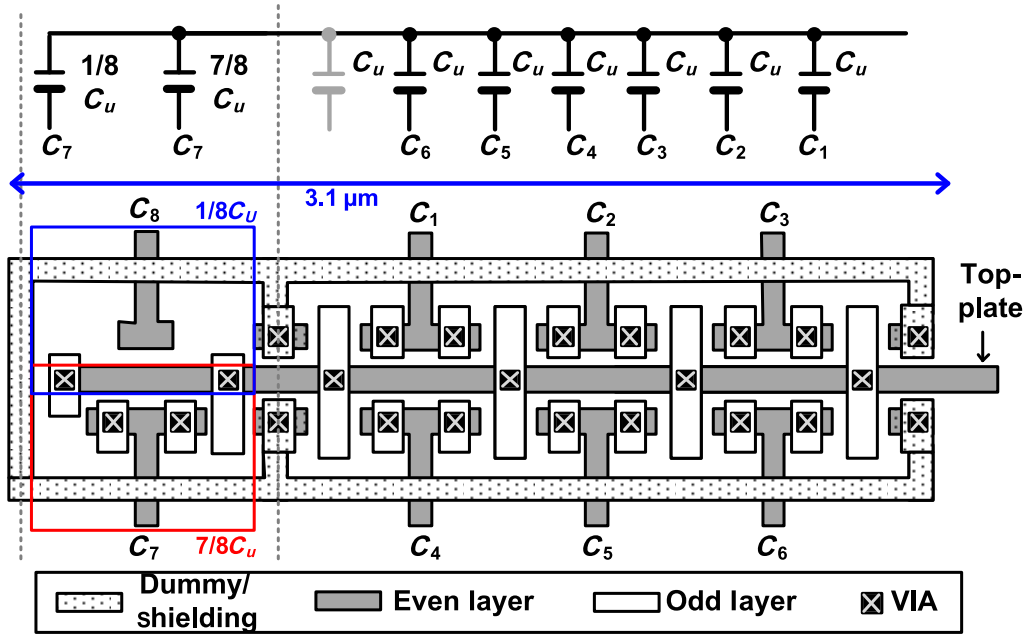

Fig. 11. DAC layout structure ($7/8V_{\text{ref}}$ example).

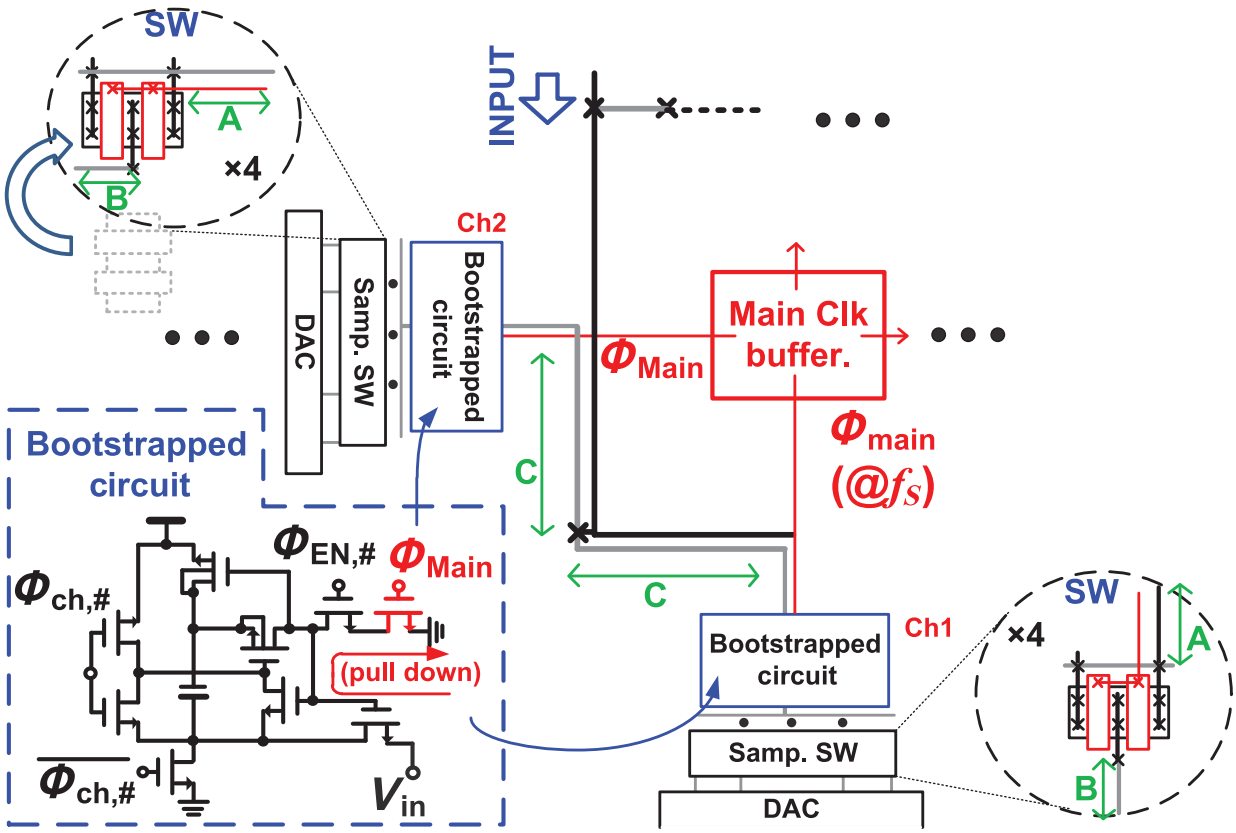

Fig. 12. Floorplan of the interleaved sampling front-end with details of the bootstrapped circuit.

ε is by adding extra latches at the comparator's outputs, which introduces an exponential gain [14] to reduce ε. Nevertheless, large power overhead and extra SA loop delay are added, especially in a 3 b/cycle SAR architecture requiring seven extra latches. Instead, a correction scheme is proposed at the output of the ADC in this design.

B. Correction Scheme

Fig. 9 shows the block diagram, circuit details, and logic flow of the proposed BDCO scheme. The BDCO circuits detect whether the controls for the differential DAC are different or not with simply XOR gates. If either cases (CASE 1–7) are

detected, the output of the ADC will be directly replaced by the code in the mapping table in Fig. 10 accordingly. During this condition, the residue and the second cycle comparison results are not important anymore and not being used for the rest of the quantization. If CASE 1–7 are not activated, the ADC will process the normal operation with regular decoding. It is worth noting that the BDCO does not eliminate all the occurrence of 8 LSB errors, since the decision point is now shifted to the detection of the CASE 1–7 in the BDCO. If it is in metastability, the 8 LSB's error will still appear. However, as the case signals have more time (when the comparator at reset and DAC at settling) as well as extra logic gain (e.g., XOR gate and keeper/latch in FB of Fig. 7), the error probability (P_E) with 8 LSB's error magnitude is considerably suppressed. During the measurement, it can be found that the P_E has been improved at least by four orders of magnitude (10^{-2} to 10^{-6}) when comparing with the simulation (no noise at postlayout) without the proposed BDCO scheme.

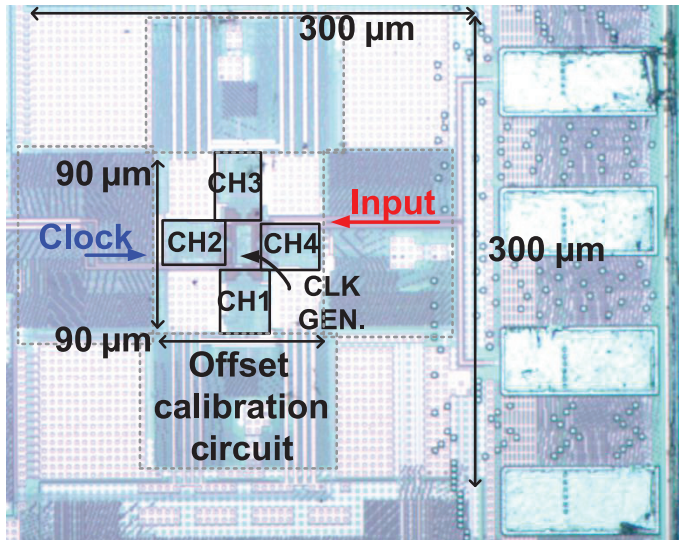

Fig. 13. Chip microphotograph.

V. Circuit, Layout, and Interleaving Front-end

A prototype ADC was fabricated in 65 nm CMOS to evaluate the effectiveness of the proposed architecture. This section describes the on-chip offset calibration for the dynamic preamplifiers and latches, the DAC layout structure, and the interleaving sampling front-end.

A. Dynamic Biasing Offset Calibration

As interpolation is applied at the dynamic preamps' outputs, offset compensation, such as extra differential pair [19], at the preamplifier level result in a residual offset at the interpolated latches. Even though the interpolation can relax the offset requirement at the latches [6], their offsets still need to be handled in this design due to small sizing for low-power purposes. Conventionally, offsets in the latch can be calibrated with variable capacitance at its outputs with digital or analog control [20], [21]. However, this not only slows down the comparators but also increases their power consumption because of the significant amount of extra loads. Alternatively in this design, a pair of clocked variable-biasing transistors is introduced at the internal nodes of the latch for offset compensation. According to the simulation, the proposed scheme lead to 15% speed improvement comparing with the variable capacitance technique for the same offset calibration range (± 20 mV) in this design. As shown in Fig. 10(a), the added transistors ($M_1 - M_4$) are clocked before the latch being enabled by the dynamic preamplifier. The variable-biasing transistors ($M_3 - M_4$) control the current flow at the internal nodes in order to suppress the offset. The calibration step can be described by Fig. 10(b) as follows: first, the inputs of the preamplifier are shorted together, the calibration logic then senses the offset polarity through the calibrating latch and feeds back an investigating voltage ($V_{\text{cal},P}/V_{\text{cal},N}$) to compensate the offset. Second, the output of the latch flips after the offset is calibrated and $V_{\text{cal},P}/V_{\text{cal},N}$ holds its current value similar as [21]. These steps repeat seven times to calibrate all the offsets from each dynamic preamplifiers and latches at foreground. Since the calibration is performed in foreground, the offset voltage can drift due to the supply or temperature variation (after calibrated). With a $+10\%$ or -10% supply voltage variation after calibration, the simulated 3σ postcalibration offset voltage increases from ± 1 mV to -15 mV to 10 mV and to -5 mV to 7 mV range, respectively. After calibration at 27 °C, if the temperature changes to -40 °C or $+125$ °C, the offset voltage drifts to -2.8 to 4 mV at -40 °C; and to -5.23 to 6.1 mV at $+125$ °C. Both large supply voltage or temperature variation lead to a residual offset voltage exceeding $1/2$ LSB of the ADC; therefore, recalibration is required in order to keep the performance.

B. Unit Capacitance and DAC Structure

For the low-to-moderate resolution SAR ADC design, the matching of the DAC and the KT/C noise are usually not the constraints. Thus, a small unit capacitance can be chosen to enhance the SA FB as well as lowering the power from switching and buffer circuits. In this design, the unit capacitance (C_u) is only 400 aF which is mainly limited by the input variable capacitance at the dynamic preamplifier's inputs. As the top-plate sampling is adopted in this design, this variable gate capacitance induces a signal-dependent gain error. The variable (gate) capacitance from a 1 V_{pp} input swing and $0.27/0.06$ µm (width/length) transistor is close to 0.3 fF which limits the total capacitance of each DAC array (single side) to at least 6.4 fF for less than 1/4 LSB error.

The unit capacitor structure is designed to be able to be shared in both vertical and horizontal directions so that a very compact DAC layout can be accomplished as shown in Fig. 11. The fractional capacitor (1/8 and $7/8C_u$) is implemented with a similar coupling structure as the unit capacitor but with less desired coupling capacitance. Different from the fractional capacitors, the layout matching of the first 6 MSB unit capacitors is important. Therefore, a common-centroid approach is adopted with dummies surrounding to insure their accuracy.

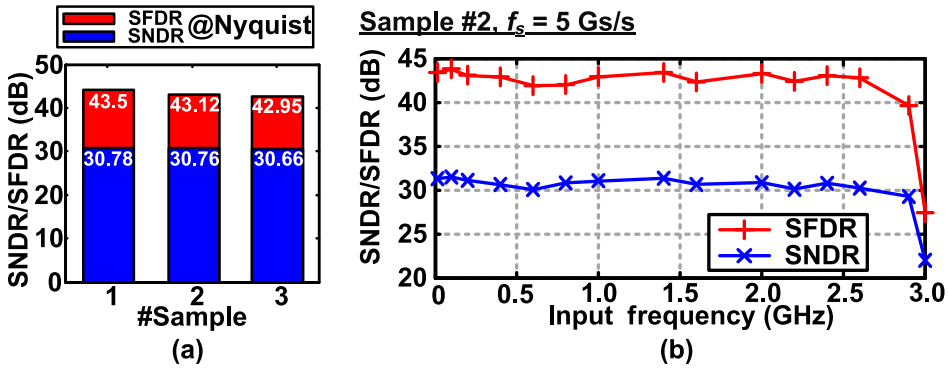

Fig. 14. Measured results of SNDR and SFDR (a) from three different samples at near Nyquist input and (b) sweeping across input frequency at $f_S = 5$ GS/s with sample number 2.

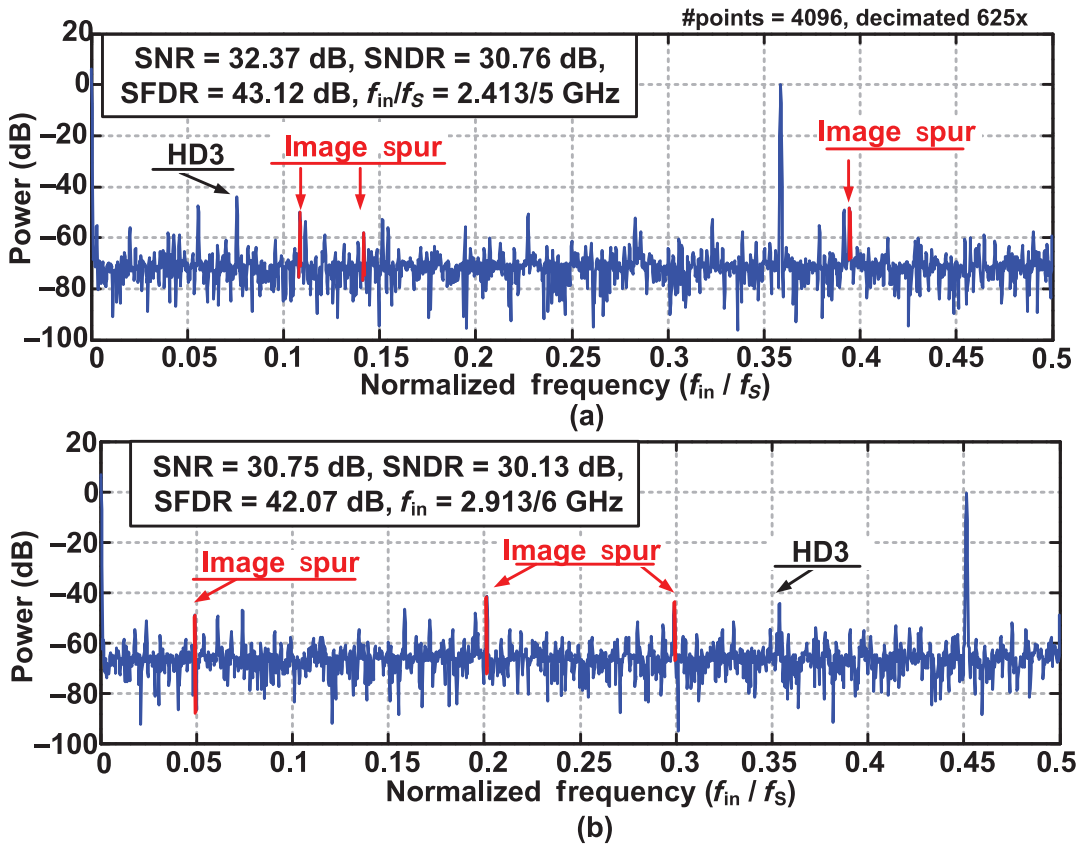

Fig. 15. Measured output spectrum of the ADC at near Nyquist input at (a) $f_S = 5$ GS/s and (b) $f_S = 6$ GS/s.

C. Interleaving Front-End

In order to avoid complicated timing calibration for a large amount of interleaving channels, only an interleaving factor of 4 is chosen. With only four channels, the layout can be optimized mainly for the important sampling clock, as illustrated in Fig. 12. The main clock generator is arranged at the center of each channel and the master sampling clock is equally distributed. Rather than splitting the sampling instants in different channels with a NAND gate or multiplexer [1], [14], a master clock control (Φ_{main}) at full sampling rate is used for all the pull-down switches in the bootstrap circuit among the channels as [18] and [22]. As the floorplan of the interleaving front-end is in a cross style, some sampling switches among the channels have different gate orientations which causes large mismatch at the interleaved sampling, due to the nonisotropic property of silicon transistors. Therefore, all the sampling switches are arranged to be in the same (vertical) gate direction and simultaneously maintaining the same routing distance (A, B, and C in Fig. 12) at input and output.

VI. Measurement Results

The 6 bit ADC prototype was fabricated in a 65 nm 1P7M digital CMOS process. Fig. 13 shows the micrograph of the chip whose active area is 0.09 mm^2 including the ADC core and the on-chip calibration (while only 0.008 mm^2 without

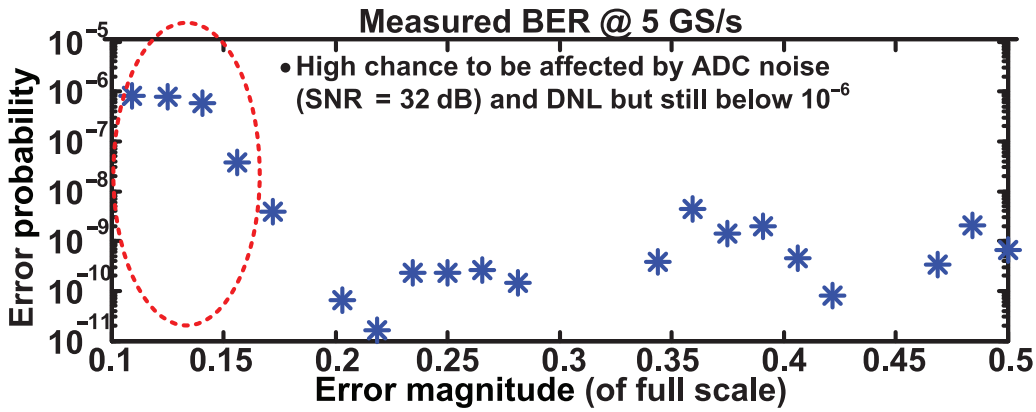

Fig. 16. Measured BER at sampling rate of 5 GHz.

TABLE II
BENCHMARK WITH STATE-OF-THE-ART ADCS

	ISSCC'10 [1]	VLSI'13 [5]	VLSI'12 [6]	ISSCC'14 [25]	A-SSCC'14 [26]	This work	
Architecture	Ti-pipelined B-S	Flash	Flash	Ti-SAR	Ti-SAR	Ti-multibit SAR	
Process	40 nm	32 nm SOI	40 nm	28 nm UTBB FDSOI	32 nm SOI	65 nm	
Supply voltage (V)	1.1	0.85	1.1	1.0	1.1	1.0	1.2
Sampling rate (GS/s)	2.2	5	3	10	36	5	6
Resolution (bit)	6	6	6	6	6	6	
Power (mW)	2.6	8.5	11	32	110	5.5	10.6
$SNDR_{min}$ in Nyq. band (dB)	29.6	30.9	33.1	33.8	31.6	30.25	30.13
Input cap.(fF)	200	135	72	100	N/A	31	
FoM at Nyq. (fJ/conv.=step)	40.0	59.33	100.48	81	98	39	67.37
Active area (mm^2)	0.03*	0.02*	0.021*	0.009*	0.048**	0.008*(0.09**)	
Calibration	Off-chip	Off-chip	Off-chip	Off-chip	On-chip	On-chip	

*Without calibration.
**With calibration.

calibration). The ADC has a full-scale input range of 1 V_{pp} differential and an input capacitance of only 31 fF including parasitic but without PAD and ESD devices. Three samples were measured and their SNDR and SFDR at a conversion rate of 5 GHz with Nyquist input are illustrated in Fig. 14(a). The SNDR and SFDR are maintained among the samples and the sample number 2 (with average performance) has been selected to report the following results. Fig. 14(b) depicts the SNDR and SFDR across low frequency and up to a larger frequency than the Nyquist input at 5 GS/s. The SNDR remains quite flat until around the 2.8 GHz input. Fig. 15(a) shows the ADC output spectrum at Nyquist input rate with 5 GS/s after calibration. The measured SNR and SNDR are 32.37 and 30.76 dB, respectively. The SFDR is 43.12 dB which is mainly limited by the third harmonic induced by the nonlinearity of the sampling front-end. The maximum INL/DNL is 0.95/1.4 LSB, respectively. After raising the supply to 1.2 V, a sampling rate of 6 GHz is achieved. The output spectrum of 6 GS/s with near Nyquist input is depicted in Fig. 15(b). The SFDR is 42.07 dB and is limited by the image spurs due to the interleaving, while the SNR and SNDR drop to 30.75 and 30.13 dB, respectively.

The measurement result of the error probability is also provided as in Fig. 16, which is obtained based on the setup suggested in [23] and [24]. The bit error rate (BER) at around 8 LSBs ($V_{ref}/8$) is less than 10^{-6} and rolls off to below 10^{-8} with larger error magnitude. Since the measurement setup does not contain memory and is not able to perform averaging, the result is expected to be affected by noise and DNL [24]. The measured SNR at 5 GS/s is 32.37 dB, indicating that the noise sigma of the ADC is 1.6 LSBs ($V_{ref}/40$) thus 5 sigma is 8 LSBs ($V_{ref}/8$). As the probability of 5 sigma is 3E–7, this implies that the measured error rate of 8 LSBs error magnitude is wrongly triggered by noise (but not metastable events) with at least a probability of 3E–7. Since this (3E–7) is close to the measured error probability at 8 LSBs ($V_{ref}/8$) ($\sim 7E-7$), it can be concluded that the obtained error probability at around 8 LSBs error magnitude is mainly limited by noise due to the measurement setup, and the actual probability should be lower. It is also worth noting that only noise is considered in the above discussion. Indeed, the DNL can also induce a significant influence [24]. If the BER of the ADC is indeed limited to 10^{-6}, it requires forward error correction (FEC) to be applicable for the optical communication system.

The total power consumption is 5.5 mW at a single 1 V supply with on-chip calibration. The analog power, including the dynamic preamplifiers, latches, and the sampling bootstrapped

circuits, is 2.3 mW and the logic and clock generator with buffer consume around 2.09 and 1.1 mW, respectively. It is worth noting that the switching power of the DAC is very small (less than 2%), thus, there is not much discussion on the switching energy throughout this work. The calculated Walden FoM at Nyquist input is 39 fJ and 67 fJ/conversion-step at 5 and 6 GS/s, respectively. Table II summarizes and compares this work with state-of-the-art ADCs. Although this ADC is implemented in a less advanced technology when compared with other circuits in the table, it achieves the best energy efficiency, smallest area, and input capacitance. Besides, this design has the lowest Walden FoM among the ADC designs with sampling rate higher than 2 GS/s.

VII. Conclusion

A 6 bit 5 GS/s $4\times$-interleaved 3 b/cycle SAR ADC has been presented. The large area and power overhead from the 3 b/cycle architecture are reduced by various techniques, including the dynamic preamplifier interpolation, DAC structure and switching simplification, BDCO and master-clock-control bootstrapped-switch. While through optimizing the floorplan and DAC layout structure, a compact area is also achieved by this prototype. Measurement results are reported which indicate the effectiveness of the BDCO scheme. This design exhibits a good energy efficiency at a high sampling rate in 65 nm. It draws only 5.5 mW power from a 1 V supply at a conversion rate of 5 GHz with a Walden FoM of 39 fJ/conversion-step.

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