A 2-μm InGaP/GaAs Class-J Power Amplifier for Multi-Band LTE Achieving 35.8-dB Gain, 40.5% to 55.8% PAE and 28-dBm Linear Output Power

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***Abstract*—This paper describes the first linear multistage class-J power amplifier (PA) fabricated in a 2-μm InGaP/GaAs HBT process for multi-band long-term evolution (LTE) applications. It includes a three-stage topology composed by a pre-driver, driver, and a class-J main stage, to optimize the output power and power-added efficiency (PAE) over 1.7–2.05 GHz, thus encapsulating the LTE bands 1 to 4, 9 to 10, 33 to 37, and 39. This is achieved through a novel analog pre-distorter linearizer, which features two sub-circuits for AM–AM and AM–PM linearization. The PA prototype meets the standard's adjacent channel leakage ratio ($\mathrm{ACLR} < -30$ dBc) at a maximum linear output power of 28 dBm. Tested at 2.05 GHz and for a 16-QAM scheme, the maximum error vector magnitude is 3.38% at a 28-dBm output power, which corresponds to a PAE of 40.5%–55.8% across bands. The input return loss is < -15 dB and the maximum power gain is 35.8 dB, while demonstrating an unconditional stable characteristic from dc up to 5 GHz. The die area is 950 μm $\times$ 900 μm. The performance metrics compare favorably with the state-of-the-art.**

***Index Terms*—Adjacent channel leakage ratio (ACLR), error vector magnitude (EVM), gallium–arsenide (GaAs), long-term evolution (LTE), power-added efficiency (PAE), power amplifier (PA), quadrature amplitude modulation (QAM).**

I. Introduction

THE LONG-TERM evolution (LTE) wireless systems rely on spectrally efficient modulation techniques to meet the demand of high data-rate transmission such as the quadrature amplitude modulation (QAM) and the orthogonal frequency division multiplexing (OFDM) access. The OFDM results in a nonconstant signal envelope with a high peak-to-average power ratio (PAPR). This sets stringent specifications in terms of linearity for the power amplifier (PA). Besides linearity, the power-added efficiency (PAE) is another critical specification that is essential in extending the handset's battery life. In order to transmit within the strict linearity specifications, PAs are forced to operate in a less efficient back-off region. This as well limits the wideband transmission capability of the PA, thus leading to the integration of multiple narrowband PAs for multiband operation. Yet numerous efforts have taken place to improve the LTE transmission bandwidth by introducing various efficiency enhancement techniques [1]–[5].

The Doherty technique has been explored to improve the back-off efficiency of the PA. This is achieved by modulating the load respective to the output power level [6]–[10]. The load modulation is achieved by realizing a quarter-wavelength delay at the input of the peaking amplifier, and at the output of the carrier amplifier. However, the sensitivity of the delays to the frequency, particularly the input delay of the peaking amplifier, which defines its turn ON time, limits its efficiency in broadband operation [11]. Despite such a limit, a wideband efficiency of $>$30% for LTE operation was proven by adding a phase compensation network and additional offset line with a supply voltage of 4.5 V [12].

In recent years, the envelope tracking (ET) methodology is gaining more popularity in the LTE PA design. ET involves the modulation of the supply voltage of the PA respective to its power level, thus enhancing the efficiency at the back-off power region [13]–[20]. This improvement is obtained as a result of reducing the supply voltage to the PA at low output power [21]. In ET methodology, the efficiency of the dynamic power supply does influence the overall PA performance. Thus, the supply modulator tends to become a bottleneck for wideband signals especially when the envelope signal has a wider bandwidth than the RF signals [22]. Nevertheless, using a complex supply modulator, LTE multi-band operation is proven even for a 300-MHz RF bandwidth with more than 30% PAE across bands [23].

In order to concurrently achieve wideband operation and a high PAE, this paper proposes a class-J PA fully integrated in a 2-μm InGaP/GaAs HBT process for multi-band LTE. The conventional practices were to use the class-J topology in GaN and LDMOS processes due to their advantage of high supply voltage swing [24]–[28]. Yet, in this work by

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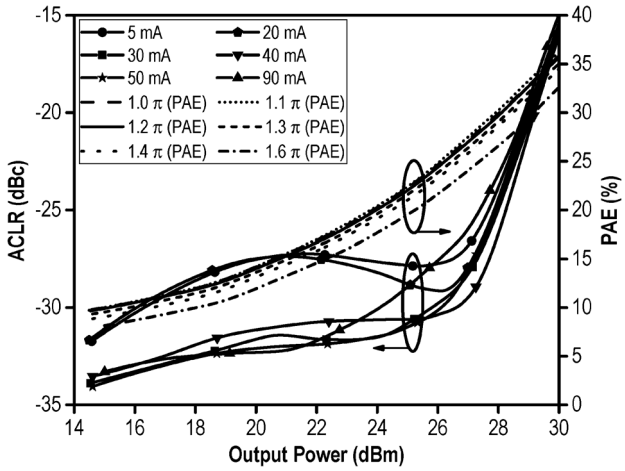

Fig. 1. ACLR and PAE plot for various biasing current for the single-stage amplifier.

incorporating an optimum positive reactance component to the load impedance of the GaAs HBT device followed by an optimum output impedance network, class-J operation is achieved. To ensure the class-J PA operates in the linear mode, a novel analog pre-distorter (APD) linearizer is integrated at its input. The APD consists of two sub-circuits, which are responsible for amplitude-to-amplitude modulation (AM–AM) and amplitude-to-phase modulation (AM–PM) linearization, respectively, for improving the operating bandwidth without penalizing the efficiency.

This paper is organized as follows. The design of the class-J PA is presented in Section II, and the operation of the APD is described in Section III. Section IV reports the measurement results, followed by conclusions in Section V.

II. Class-J Wideband PA Design

A. Optimum Bias Point—Measurement Analysis

The impact of the third-order component can be analyzed in the definition of the adjacent channel leakage ratio (ACLR) [29]. This is verified via measurements, where the final-stage amplifier is assessed by sweeping its biasing current to determine the optimum value for the best ACLR at the region close to the class-B biasing point. The resultant plot is shown in Fig. 1, where it is evident that the PA delivers the best ACLR at a quiescent current of 40 mA. The resulting PAE at the output power of 28 dBm is 28% where the measurement has been done at 1.98 GHz. Thus, this quiescent current is desirably chosen to bias up the final stage amplifier, which is later designed as the class-J PA main stage.

B. Class-J Output Impedance Analysis

The class-J PA was invented by Cripps [30]. It is capable of delivering the same efficiency and linearity as with the class-AB PA abstaining from the need of band limiting transmission line harmonic short [31]. Instead, it employs a reactance harmonic termination technique to improve the efficiency. Fig. 2 depicts the schematic of the HBT class-J PA. The transistor is biased in deep class-AB mode where the RF output current waveform is half-wave rectified. Hence,

$$I_T = \begin{cases} -I_{\max}\sin\theta, & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi. \end{cases} \tag{1}$$

The fundamental current component flowing in the matching network is given as

$$I_F = I_1 \sin(\theta + \phi) \tag{2}$$

where ϕ is the phase deviation of the matching network and I_1 is the fundamental current. The current flowing into C_{2fo} of Fig. 2 is

$$I_C = I_{CC} - I_F - I_T \tag{3}$$

where the dc output current, $I_{CC} = I_{\max}/\pi$. The output voltage V_O is expressed as

$$V_O = \frac{1}{\omega C_{2fo}} \left[\int_0^{\pi} I_C \, d\theta + \int_{\pi}^{2\pi} I_C \, d\theta \right]. \tag{4}$$

Therefore, from the conduction angle of $0 < \theta < \pi$,

$$\begin{aligned} V_{O1} &= \frac{1}{\omega C_{2fo}} \int_0^{\pi} \left(\frac{I_{\max}}{\pi} - I_1 \sin(\theta + \phi) - I_{\max}\sin\theta \right) d\theta \\ &= -\frac{1}{\omega C_{2fo}} (I_{\max} + 2I_1 \cos\phi). \end{aligned} \tag{5}$$

The negative sign indicates that the voltage and current are out-of-phase to each other. From the conduction angle of $\pi < \theta < 2\pi$, I_T in (3) is 0. Hence,

$$\begin{aligned} V_{O2} &= \frac{1}{\omega C_{2fo}} \int_{\pi}^{2\pi} \left(\frac{I_{\max}}{\pi} - I_1 \sin(\theta + \phi) \right) d\theta \\ &= \frac{1}{\omega C_{2fo}} (I_{\max} + 2I_1 \cos\phi). \end{aligned} \tag{6}$$

Fourier analysis is conducted on the output voltage component V_{O1} and V_{O2}, which are given as V_1 and V_2 in (7) and (8), shown at the bottom of the following page. From these equations, it can be observed that V_1 has a positive imaginary component, whereas V_2 has a negative imaginary component. Thus, the output impedance of the designed amplifier has to present a complex output impedance with a positive reactance component instead of the conventional resistive output impedance. The second condition imposes that the impedance presented to the second harmonic of the device has to be purely capacitive.

C. Class-J Second Harmonic Impedance Analysis

The presence of reactive components in (7) and (8) shifts the voltage waveform of the amplifier in the time domain, thus initiating the transition from deep class-AB to class-J operation. Adding a capacitive component to the second harmonic shifts the voltage waveform by 45°, as illustrated in Fig. 3(a). The

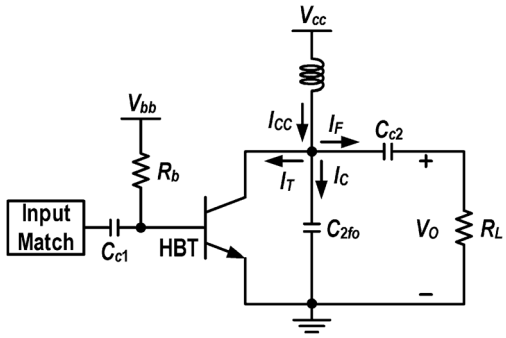

Fig. 2. Simplify schematic of an HBT class-J PA.

current and voltage waveform in Fig. 3 is represented in (9) and (10), respectively,

$$I(\theta) = I_{\max}\left(\frac{1}{\pi} + \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta) + \cdots\right) \tag{9}$$

$$V(\theta) = \pi V_{\rm dc}\left(\frac{1}{\pi} - \frac{1}{2}\cos(\theta+\delta) + \frac{2}{3\pi}\cos\left(2(\theta+\delta)\right) - \cdots\right) \tag{10}$$

where δ represents the phase shift of the voltage waveform. To present a class-J operation, the ratio between the second-order harmonic-voltage and fundamental-voltage waveforms, V_{2fo}/V_{fo} is set to $\cos(45^\circ)/2$. Thus, if $V_{fo} = \sqrt{2}/2$, then $V_{2fo} = -1/4$. Consequently, the second-order harmonic impedance is calculated as

$$Z_{2fo} = \left(\frac{3\pi}{8}\right)\cdot R_{\rm opt}\angle -90^\circ. \tag{11}$$

D. Simulation Analysis

The final stage class-AB amplifier's optimum output resistance $R_{\rm opt}$ is 5 Ω, which gives the optimum tradeoff for PAE

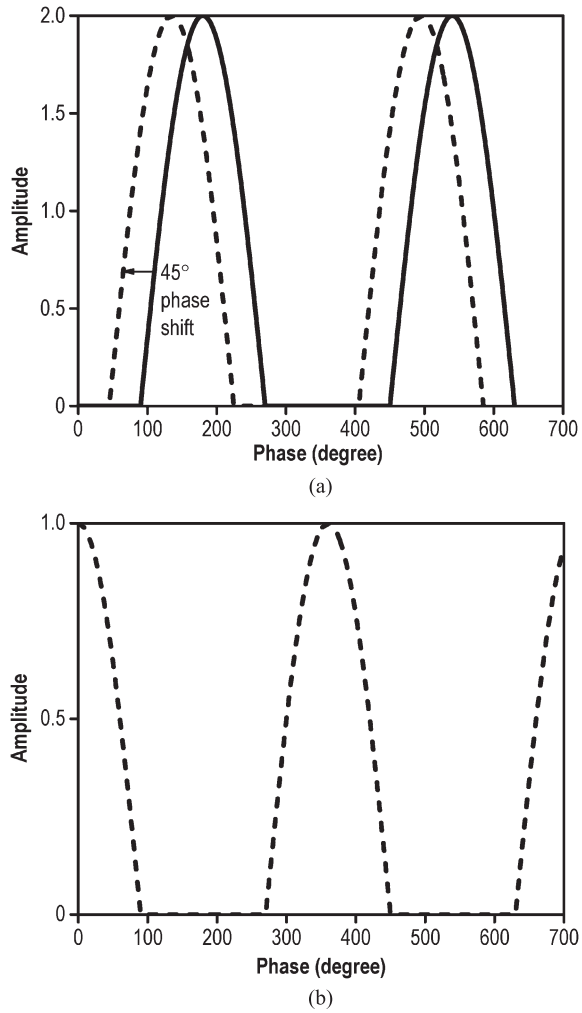

Fig. 3. (a) Modification of the voltage waveform. (b) Half-wave rectified current waveform.

$$\begin{aligned} V_1 = {} & \frac{1}{\omega C_{2fo}\pi}\left[I_{\max}\left[-2\sin\theta + \frac{1}{\pi}(\cos\theta + \theta\sin\theta - 1)\right]\right. \\ & \left. - I_1\left[\sin\theta\cos\phi + \frac{1}{2}\theta + \frac{1}{4}\left(\sin 2\theta\cos\phi + \sin\phi(1+\cos 2\theta)\right)\right]\right] \\ & + j\frac{1}{\omega C_{2fo}\pi}\left[I_{\max}\left[\frac{1}{\pi}(\sin\theta - \theta\cos\theta) - 2(1-\cos\theta)\right]\right. \\ & \left. - I_1\left[\cos\theta(1-\cos\theta) - \frac{1}{2}\left(\frac{1}{2}\cos\phi(1-\cos 2\theta)\right) - \sin\theta\left(\theta - \frac{1}{2}\sin 2\theta\right)\right]\right] \end{aligned} \tag{7}$$

$$\begin{aligned} V_2 = {} & \frac{1}{\omega C_{2fo}\pi}\left[I_{\max}\left[\frac{1}{\pi}\left(\frac{1}{2}\theta\sin 2\theta - \frac{1}{4}\cos 2\theta + \frac{1}{4}\right) - \sin 2\theta\right]\right. \\ & \left. + I_1\left[\sin(\theta-\phi) - \frac{1}{3}\sin\phi - \frac{1}{6}\sin(3\theta+\phi) - \frac{1}{2}\sin 2\theta\cos\phi\right]\right] \\ & - j\frac{1}{\omega C_{2fo}\pi}\left[\frac{1}{2}I_1\left(\cos\phi[1-\cos 2\theta] + \cos\phi[1-\cos\theta] - \frac{1}{3}\cos\phi[1-\cos 3\theta] - \sin\theta\sin\phi + \frac{1}{3}\sin 3\theta\sin\phi\right)\right. \\ & \left. - I_{\max}\left(\frac{1}{2\pi}\left(\frac{1}{2}\sin 2\theta - \theta\cos 2\theta\right) + \cos 2\theta - 1\right)\right] \end{aligned} \tag{8}$$

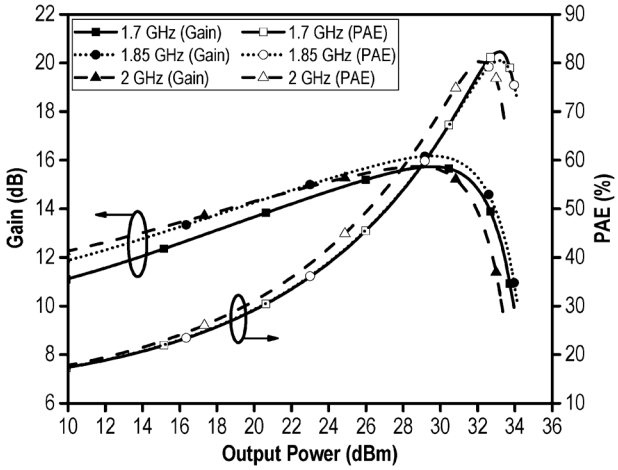

Fig. 4. Gain and PAE plot across output power for $Z_{\rm out} = 2 + j3$.

and maximum output power prior operating as a class-J amplifier. For class-J operation, the initial second-order harmonic reactive termination capacitive value is given by

$$C_{2fo} = \frac{1}{2\pi f \cdot Z_{2fo}}. \tag{12}$$

Since $Z_{2fo} = (3\pi/8)$, $R_{\rm opt}$, and $R_{\rm opt} = 5\ \Omega$, at the highest operating frequency of 2 GHz, C_{2fo} is computed to be 13.5 pF. By setting C_{2fo} to 13.5 pF, the fundamental load impedance is optimized to deliver the highest backed off PAE with saturated output power $(P_{\rm sat})$ of >32 dBm. The above calculated load impedance is used as a base line for a load–pull simulation to determine the optimum $Z_{\rm load}$ for class-J operation where $Z_{\rm load}$ is varied from the initial value of 5 Ω. The amplifier's quiescent collector current is set to 40 mA. From the load–pull result, for the optimum fundamental load impedance in terms of maximum output power and PAE, $Z_{\rm out}$ is observed to be $2 + j3$. The resultant plot is illustrated in Fig. 4. It can be observed that the maximum output power is indeed >32 dBm from 1.7 GHz up to 2 GHz, with a PAE >50% at 28 dBm of output power.

E. Output Matching Network Design

Fig. 5 illustrates the proposed output matching network to transform the 50-Ω load impedance to the desired $Z_{\rm out} = 2+j3$. The matching network can be divided into the following two sections.

- Network I, which represents the T-network comprises L_2, C_3, and L_3, where the 50-Ω load is transformed to an intermediate impedance of 25 Ω.
- Network II, which represents the L-network, consists of C_2 and L_1, which transform 25 Ω to $(2 + j3)$ Ω.

In Network I, the values of L_2, C_3, and L_3 are determined through the following equations [32]:

$$L_2 = R_1 \frac{\sqrt{N-1}}{\omega_o} \tag{13}$$

$$C_3 = \frac{\sqrt{N-1} + \sqrt{\left(\frac{N}{M}\right) - 1}}{\omega_o N R_1} \tag{14}$$

$$L_3 = R_2 \frac{\sqrt{\left(\frac{N}{M}\right) - 1}}{\omega_o} \tag{15}$$

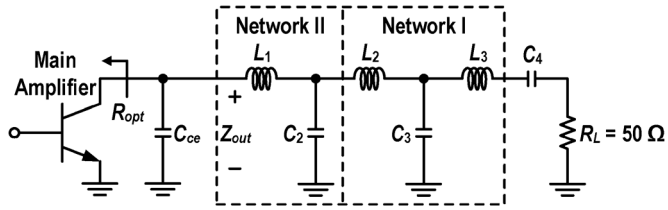

Fig. 5. Class-J output matching network topology.

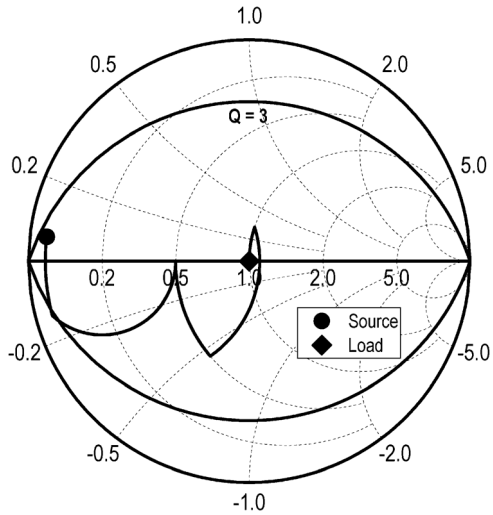

Fig. 6. Impedance transformation plot.

where $M = R_2/R_1 > 1$ and $N > M$.

In this work, $R_1 = 25\ \Omega$ and $R_2 = 50\ \Omega$. Therefore, $M = 2$ and N is set to 2.2. For Network II, the value of C_2 and L_1 are obtained through the following equations derived as:

$$L_1 = \frac{3 + \sqrt{46}}{\omega_o} \tag{16}$$

$$C_2 = \frac{\frac{\sqrt{46}}{50}}{\omega_o} \tag{17}$$

where $\omega_o = 2\pi f_o$ in which f_o is the center frequency at 1.85 GHz. The impedance transformation plot is shown in Fig. 6. The solid oval plot in the Smith chart represents the corresponding Q of the network, which is 3. The respective simulation results are illustrated in Fig. 7. The corresponding output impedance, which consists of the fundamental and second harmonics at the operating frequency from 1.7 to 2 GHz, is illustrated in Fig. 8. The voltage and current waveforms at the saturated output power $(P_{\rm sat})$ and backed-off output power $(P_{\rm bo})$ of 28 dBm are illustrated in Fig. 9(a) and (b) for 1.7 and 2 GHz, respectively. Referring to these waveforms, it is evident that the designed class-J main stage is able to operate over a wide range of frequencies. The peak voltage achieved is $> 2V_{cc}$ at an output power ≥28 dBm.

III. Linearization of Class-J PA—Single Chip Solution

Fig. 10 illustrates the complete schematic of the PA, where an APD linearizer is integrated at the input of the class-J amplifier. To increase the overall power gain of the PA, a pre-driver amplifier is added at the APD's input. Conventional APDs work only

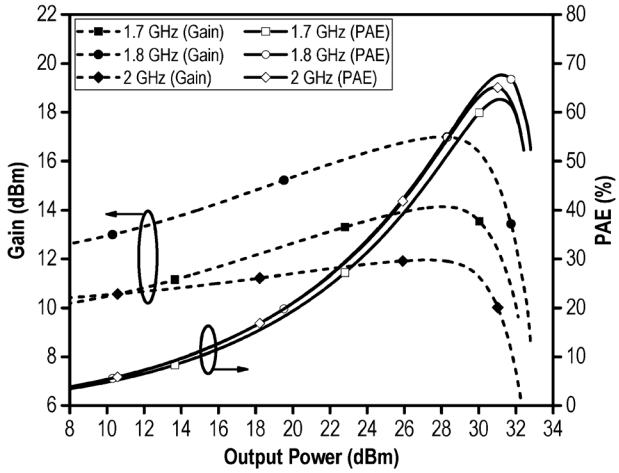

Fig. 7. Simulated output power and PAE of the final stage class-J amplifier with integrated output matching network.

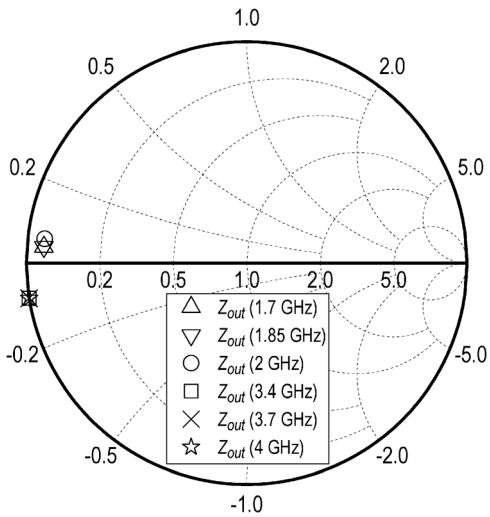

Fig. 8. Class-J output impedance and second-order harmonic plot across output power from 1.7 to 2 GHz. Second-order harmonic termination is purely reactive across the frequencies.

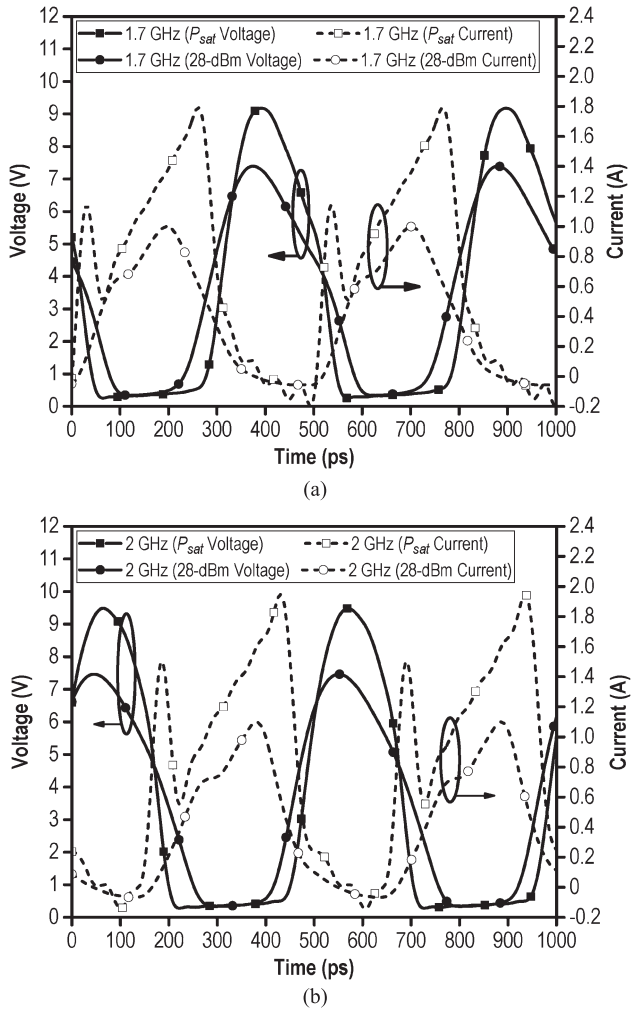

Fig. 9. Class-J voltage and current waveform at $P_{\rm sat}$ and $P_{\rm bo}$ of 28 dBm for: (a) 1.7 and (b) 2 GHz.

in narrowband operation [33], and in order to extend the operating LTE bandwidth, here the APD is divided in two sub-circuits, which are the phase and the amplitude pre-distorters.

In the HBT, spectral regrowth is mainly originated by its base–collector parasitic capacitance, $C_{\rm bc}$ [34]. To mitigate this effect, a novel phase cancellation method is proposed by integrating a base collector diode at the input of the driver amplifier. The reverse bias capacitance $C_{\rm bc-rb}$ and forward bias capacitance $C_{\rm bc-fb}$ are expressed as follows [35]:

$$C_{\rm bc-rb} = \frac{C_{\rm bc0}}{\left[1+\left(\frac{V_{\rm CB}}{\phi_0}\right)\right]^{n_c}} \tag{18}$$

$$C_{\rm bc-fb} = \frac{C_{\rm bc0}}{\left[1-\left(\frac{V_{\rm CB}}{\phi_0}\right)\right]^{n_c}} \tag{19}$$

where $C_{\rm bc0}$ is the collector–base capacitance when $V_{\rm CB}=0$, ϕ_0 is the collector–base junction built-in voltage, and n_c is the grading coefficient of the collector–base junction. In order to generate an opposite output phase response, the collector–base junction is forward biased as represented by (19).

Based on (18) and (19), the positive and negative phase insight in effect to $V_{\rm CB}$ cancels off the $C_{\rm bc-rb}$ with single forward biased base–collector diode integration, $C_{\rm bc-fb}$. However, with the aid of two base–collector diodes ($C_{\rm bc-fb} > C_{\rm bc-rb}$), an opposite phase response (AM–PM) is observed at the output of the APD. The simulated AM–PM responses at the output of the APD and class-J main amplifier are illustrated in Fig. 11. It can be observed that the driver's phase expansion and main amplifier's phase compression cancel out each other, thus contributing to the improvement of the third-order intermodulation distortion (IMD3) performance.

Generation of an opposite AM–PM response is achieved via the T section intermediate matching network that consists of C_6, L_2, C_7, and L_3. The Smith plot of Fig. 12 illustrates the location of the driver's output impedance denoted at point A. This impedance is potentially matched to X, B, or $B_{\rm con}$. Point B describes the input impedance of the main amplifier. Point X is the output impedance of the APD where else $B_{\rm con}$ is the conjugate of B. Based on the profile plot of Fig. 13, matching towards point X observes a favorable gain compression, which compensates the gain expansion of the main amplifier. Matching towards point B observes a gain expansion that begins from

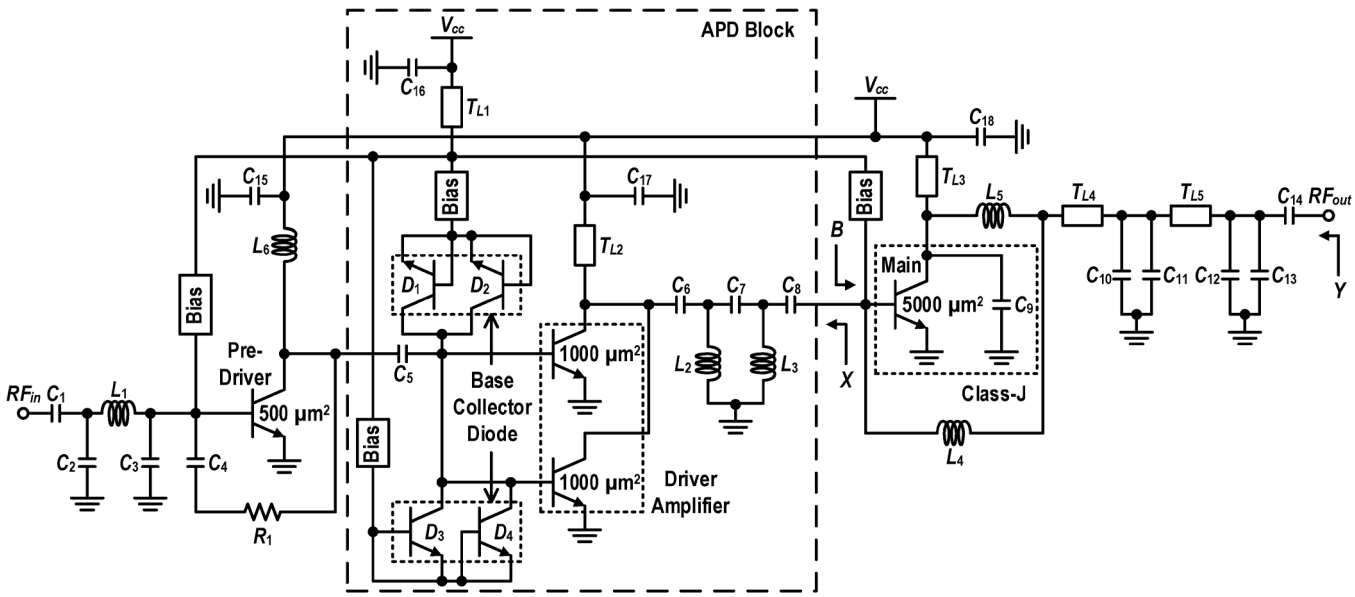

Fig. 10. Schematic of the designed PA. X denotes the output impedance of the APD and Y is the output impedance of the class-J amplifier.

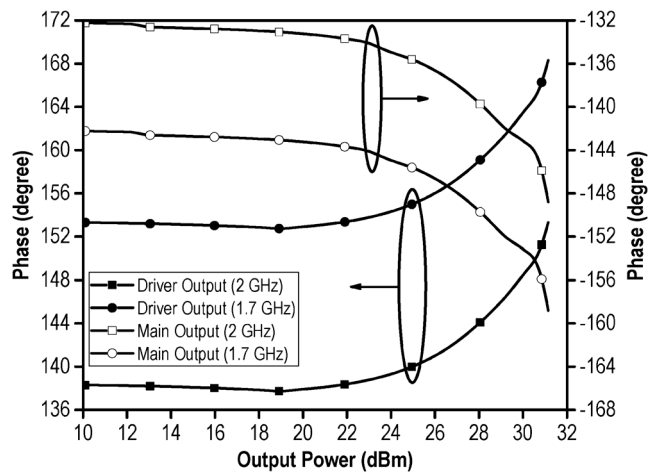

Fig. 11. Simulated AM–PM responses of the APD and main amplifier across operating band.

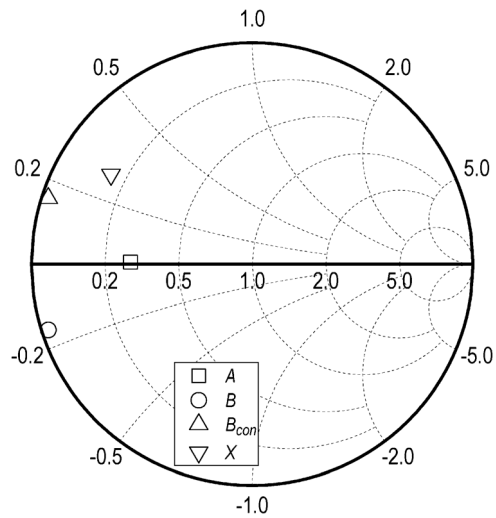

Fig. 12. Location of the impedance point of driver (A), main amplifier (B), and APD (X) at 1.7 GHz.

the lower output power, which would not result into a desirable IMD3 cancellation. Point $B_{\rm con}$ observes a flat profile until the 1-dB compression point, which results into a similar effect as with point B matching. Fig. 14 illustrates the IMD3 and PAE load–pull contours before and after linearization. Y is the output impedance of the main amplifier. These contours are plotted at an output power of 28 dBm. With the optimum biasing of 40 mA, Y is located close to the optimum IMD3 point at 2 GHz. Nevertheless, it is still located almost 8 dB away from the optimum IMD3 point at 1.7 GHz, as described in Fig. 14(a) and (b), respectively. The effect of AM–AM and AM–PM cancellation between the APD and main amplifier in the PA is illustrated in Fig. 14(c) and (d). The IMD3 optimum impedance moves to the location Y for 1.7 and 2 GHz, while the PAE degrades slightly due to the current consumption of the APD.

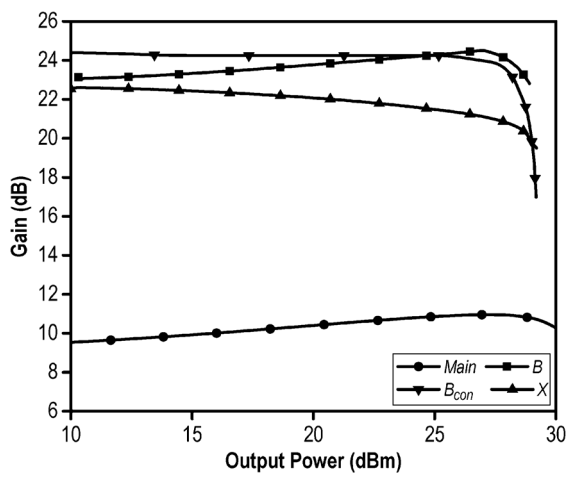

Fig. 13. Gain compression at various matching point.

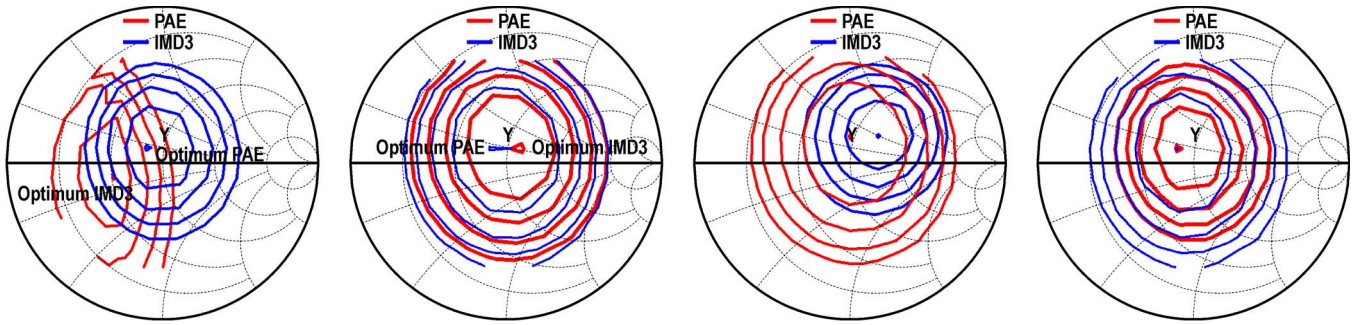

Fig. 14. IMD3 and PAE contour of the PA at: (a) 1.7 GHz prior linearization, (b) 2.1 GHz prior linearization, (c) 1.7 GHz after linearization, and (d) 2.1 GHz after linearization. The PAE contour is plotted in 1% step, whereas the IMD3 contour is plotted in a 2-dB step.

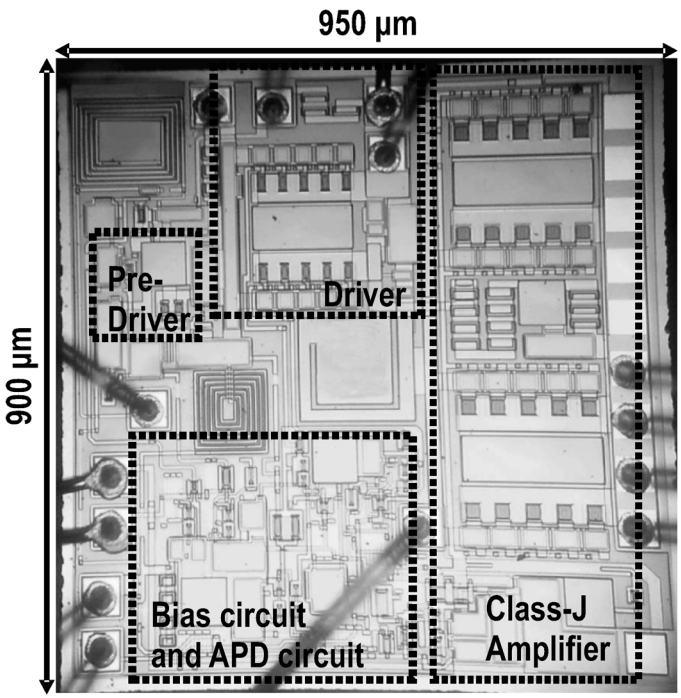

Fig. 15. Die microphotograph of the fabricated PA, where the die size is less than 1 mm^2.

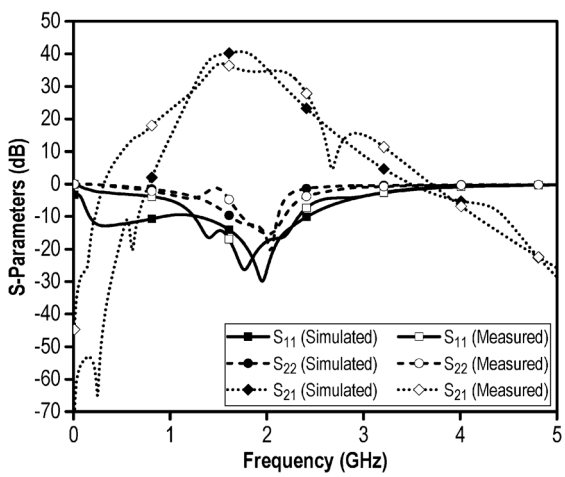

Fig. 16. Simulated and measured S-parameters of the PA with supply headroom of 3.3 V.

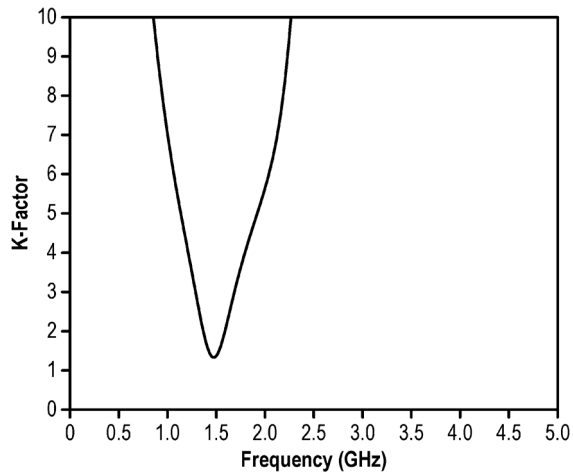

Fig. 17. PA has K-factor >1 from dc up to 5 GHz.

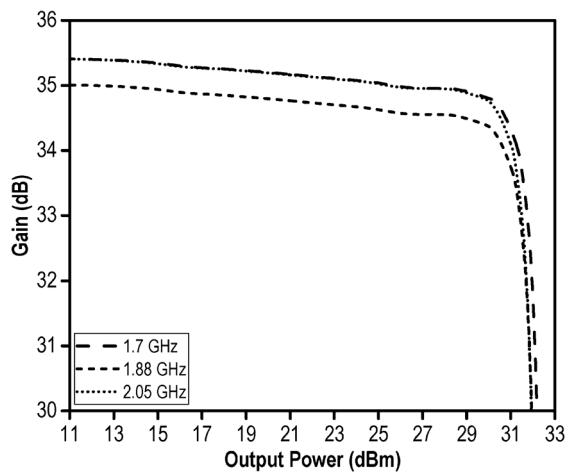

Fig. 18. Power gain plot across output power.

IV. Experimental Results

Fig. 15 illustrates the chip photograph of the PA fabricated in a 2-μm InGaP/GaAs HBT process, measuring 950 μm $\times$ 900 μm. The class-J PA is integrated into a single chip solution, along with the driver and pre-driver amplifiers. The simulated and measured S-parameter of the proposed PA is shown in Fig. 16. S_{11} and S_{22} are well matched from 1.7 to 2.1 GHz with a corresponding power gain, $S_{21} > 35$ dB, across the 300-MHz bandwidth. The PA maintains unconditionally stability for a gain >35 dB, as shown in Fig. 17 where the K-factor >1 from dc to 5 GHz. Fig. 18 illustrates the power gain plot across the

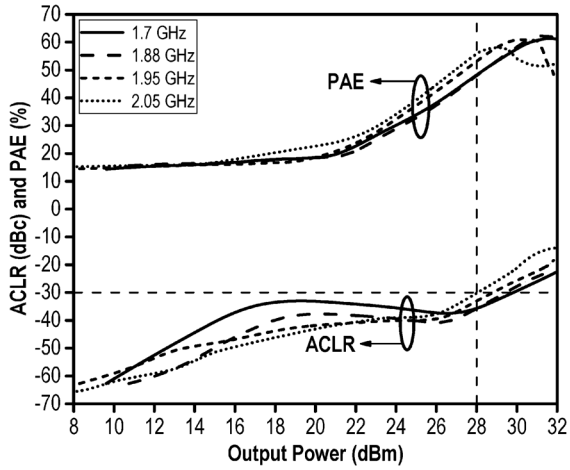

Fig. 19. ACLR and PAE performance of PA from 1.7 to 2.05 GHz.

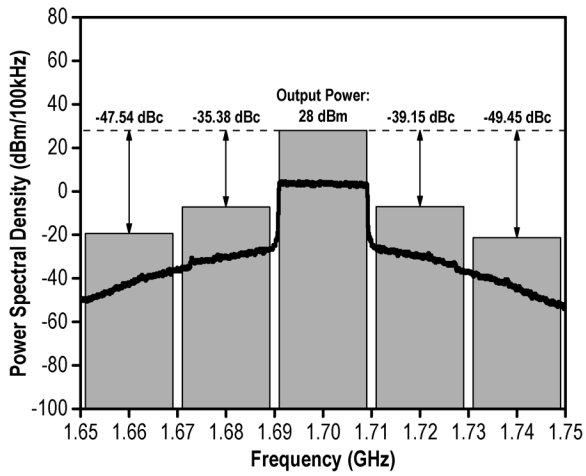

Fig. 20. ACLR and spectral mask at output power of 28 dBm.

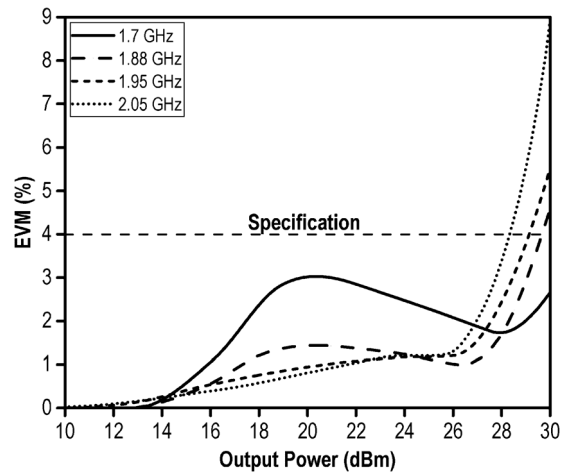

Fig. 21. EVM plot of the PA. The input signal is LTE 20-MHz 16-QAM.

output power for the three frequencies, which covers the LTE bands 1 to 4, 10, 33 to 37, and 39, in which it can be observed that the maximum output power of the PA is 32 dBm across the entire frequency range. For LTE operation, the designed PA is characterized with a 16-QAM modulated signal, which has a 20-MHz channel bandwidth. The PAPR of the signal is 7.88 dB (at 0.001%), and the resulting ACLR and PAE plots are shown in Fig. 19. With a supply voltage of 3.3 V, the PA is capable of delivering a PAE of $>$40% from 1.7 to 2.05 GHz

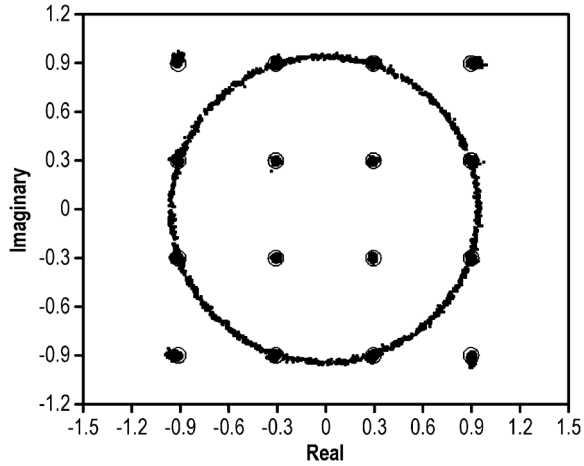

Fig. 22. Constellation diagram illustrating the OFDM measurement of the proposed LTE PA.

TABLE I
PERFORMANCE SUMMARY OF THE IMPLEMENTED PA

Parameters	Results
Technology	2-μm InGaP/GaAs HBT
Die Size	950 μm × 900 μm
Supply Voltage	3.3 V
Frequency	1.71 to 2.05 GHz
Mode	LTE
LTE Band	1, 2, 3, 4, 9, 10, 33, 34, 35, 36, 37, 39
Channel Bandwidth (BW)	20 MHz
Max. Linear Output Power	28 dBm
EVM (16-QAM)	1.74% to 3.38% at 28 dBm Output Power
PAE	40.5% to 55.8%
Gain	34.6 to 35.8 dB
S_{11}	< -15 dB
S_{22}	< -10 dB
Stability	Unconditionally Stable

at an output power of 28 dBm, with a maximum corresponding ACLR reading out to be -30 dBc, satisfying the requirement for the ACLR as stated in 3GPP specifications (3GPP TS 36.101), release 10.5 (2012).

Fig. 20 illustrates the ACLR spectrum at an output power of 28 dBm. The PA meets the regulated spectral mask and an error vector magnitude (EVM) $<$4% is achieved across the operating bands, as depicted in Fig. 21. The corresponding constellation diagram is given in Fig. 22. Finally, Tables I and II summarize the proposed PA's measured performances and performance benchmark with other recently reported designs, respectively.

V. CONCLUSIONS

A novel wideband high-efficiency LTE PA has been presented. The stringent linearity specifications are met via insightful analysis and the use of a novel APD linearizer. The class-J PA core provides a wideband efficiency from 1.7 to 2.05 GHz at a low backed-off output power. At an output power of 28 dBm, the PA delivers a high PAE of 56%, while complying with the ACLR and EVM specifications for a 20-MHz channel bandwidth. The small die area (< 1 mm^2) also benefits the cost of production. The result highlights the

TABLE II
PERFORMANCE COMPARISON OF THE PUBLISHED LTE PAS

Performance Parameter	Operating Frequency (GHz)	LTE Channel BW (MHz)	Supply Voltage (V)	Gain (dB)	Maximum Linear Output Power (dBm)	PAE (%)	Chip Size (mm^2)
[14]	2.5	10	3.3	24.8	25.8	31.6	2.6 × 1.7
[15]	2.5	20	6.0	29.0	30.0	45.0	1 × 1.6
[18]	2.4	5	4.2	16.0	24.3	42.0	1.1 × 1.5
[36]	1.7 - 2	10	4	18.3	26.5	38.6 to 35.1	1.95 × 0.8
[37]	2.35	20	3.5	41.5	28.3	19	1 × 2.6
[23]	1.7 - 2	10	3.4	26.8	28.0	33.3 to 39	-
This Work	**1.7 - 2.05**	**20**	**3.3**	**35.8**	**28.0**	**40.5 to 56**	**0.95 × 0.9**

potential applications of the proposed PA in handset transmitter systems, where it is capable of delivering a high linear output power at low supply voltage, when compared with the reported works in Table II, thus prolonging the battery's life.

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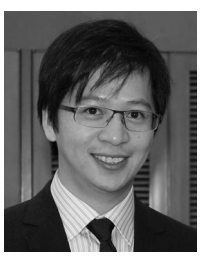

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