

tion density of the input signal [5]. The power saving for the $D1$ input sequence is $> 40\%$. The improvement is even greater in the presence of input glitching, as the proposed flip-flop dissipates 63% less power with respect to [2] for sequence C . Input glitching, in fact, results in switching activity only on node D , while node x is unaffected by glitching.

A thorough analysis including power dissipation due to clock drivers has also been carried out. The four inverters shown in Fig. 1a can be used as a local clock driver for an array of two or more flip-flops. A circuit composed of one driver and one, three, five or 10 flip-flops has been laid out and simulated with input sequences $D1$ and $D2$. Simulation results (see Fig. 4) show that average power dissipation (defined as total clock driver + flip-flop power dissipation divided by the number of flip-flops), is greatly reduced if more flip-flops share a single driver. On the other hand this is not true for the flip-flop proposed in [2] where the power dissipation due to the single inverter on the clock line is very small.

As a consequence, although the total power dissipation (clock driver + flip-flop) is greater for our circuit if a single flip-flop is considered, the situation rapidly changes as the number of flip-flops that share a local clock driver increases. For five flip-flops (see Fig. 4), the proposed circuit consumes less power than the comparison circuit, and the situation is better for the case with 10 flip-flops. Once again, the power saving is larger when the input signal is more active (sequence $D1$).

The simulation for 10 flip-flops sharing a clock driver shows that for sequences $D1$ and $D2$ the proposed flip-flop achieves a power saving of 28 and 16%, respectively, compared to [2].

Conclusions: In this Letter, a double edge-triggered flip-flop using a single latch is presented. SPICE simulations on the circuit extracted from the layout including parasitics show that the proposed flip-flop has lower power dissipation with respect to other recently reported circuits.

With reference to area occupation, the layout of an array of 16 flip-flops, including a local clock driver, requires 25% less silicon area with respect to the DET proposed in [2].

It should be pointed out that the proposed flip-flop, like those in [3, 4], has a hold time that can be larger than the setup time and clock to q delay, requiring a detailed hold timing analysis to avoid any possible timing failure.

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Offset- and gain-compensated and mismatch-free SC delay circuit with flexible implementation

Seng-Pan U, R.P. Martins and J.E. Franca

A novel SC delay circuit is presented that is insensitive to the DC offset and finite gain errors of operational amplifiers (OAs) as well as the capacitance ratio mismatch. The effectiveness is illustrated and consolidated by computer simulations. A comparison with typical compensated and uncompensated circuits in terms of magnitude, phase and offset errors is also presented. The circuit is also further extended to realise a wideband and very accurate successive-anticipatory gain compensation scheme and to flexibly implement arbitrary delay with only one OA.

Introduction: Switched-capacitor (SC) delay circuits can be applied in a variety of sampled-data signal processing areas, such as sample-and-hold interfaces, digital-based SC circuitry (i.e. FIR filtering), specialised multirate circuits etc. [1 - 8]. It has become increasingly necessary to compensate for nonlinear errors caused by the DC offset and finite gain of OAs and capacitor mismatch as the demand for accuracy in applications has increased, especially with trends towards reducing voltages. Unfortunately, many available SC delay circuits do not fully meet all these requirements [1 - 7]. In this Letter, we propose a novel SC circuit that fulfills the above demands.

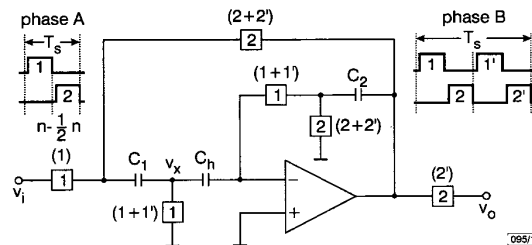


Fig. 1 Gain- and offset-compensated and mismatch-free SC delay circuits ($z^{-1/2}$)

Circuit architecture: Fig. 1 shows the proposed gain-, offset-compensated (GOC) and mismatch-free (MF) SC half-period delay circuit with phase scheme A modified from the well-known GOC integrator [7]. During phase 1, the circuit retains most of the previous output voltage at phase 2 due to the feedback capacitor C_2 , and at the same time the offset-storage capacitor C_h memorises the errors owing to the DC offset and finite gain of the OA as well as other input-referred low frequency noise developed at the inverting node. While in phase 2, the C_h is placed in series with the inverting node of the OA, thus forcing node x to be a 'super-virtual ground', the voltage of which is given by

$$v_x[n] = -\mu \left(v_o[n] - v_o \left[n - \frac{1}{2} \right] \right) \quad \mu = \frac{1}{A} \quad (1)$$

where A is the gain of the OA. It is obvious that the 'super-virtual ground' will not be affected by the offset but by the difference between two successive output voltages. If the bandwidth of the signal is relatively small compared to $f_s/2$, then the output will not vary much from one phase to the other, so this circuit will significantly compensate for the finite gain error, and its output is given by

$$v_o[n] \simeq \frac{1}{1 + \mu} v_{in} \left[n - \frac{1}{2} \right] + \frac{\mu}{1 + \left(2 + \frac{C_h}{C_2} \right) \mu + \left(1 + \frac{C_h}{C_2} \right) \mu^2} v_o[n-1] + \frac{\mu}{1 + \left(2 + \frac{C_h}{C_2} \right) \mu + \left(1 + \frac{C_h}{C_2} \right) \mu^2} v_{os} \quad (2)$$

Eqn. 2 shows clearly that there is no charge transfer and thus no matching required in this circuit. The trivial ratio C_h/C_2 can be set to unity. The gain and phase errors are simply derived by

$$m(j\omega) \simeq -\mu \left(1 - \frac{1}{1 + \mu(1 + C_h/C_2)} \cos(\omega T_s) \right) \quad (3a)$$

$$\theta(j\omega) \simeq -\frac{\mu}{1 + \mu(1 + C_h/C_2)} \sin(\omega T_s) \quad (3b)$$

The effectiveness of these expressions has been successfully verified by SWITCAP simulation. The resulting gain error is illustrated in Fig. 2, together with the comparison among some typical available SC delay circuits where $A = 100$ and all related capacitor ratios in the circuits are unity. It is seen that the proposed circuit of Fig. 1 achieves better gain compensation at all frequencies when compared with the GOC [4, 7] and conventional uncompensated (UC) delay circuits [1, 3, 4] except for the MF circuits [2, 5] when the signal frequency is greater than a quarter of the sampling rate. This new circuit also offers lower phase error (0.55° maximum) than those of other GOC schemes (1.1° maximum in [7], 2.2° in [4]). Table 1 shows that the new circuit obtains excellent suppression of the offset error among all the above delay circuits. Moreover, as this circuit does not need to be reset to the offset voltage during the compensated phase, there are no special requirements for the OA slew rate.

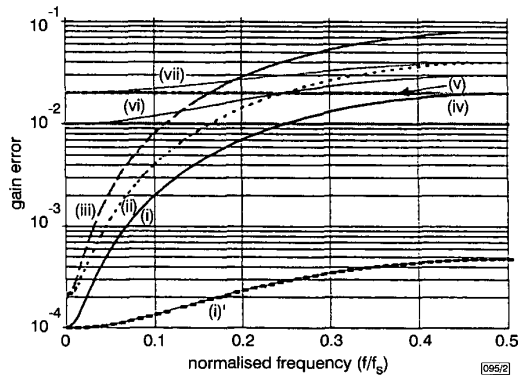


Fig. 2 Gain-error comparison of SC delay circuits ($A = 100$, $C_i/C_j = 1$)

- (i) proposed Fig. 1
- (ii) [7] with extra reset switch (GOC)
- (iii) Fig. 11b of [4] (GOC)
- (iv) [2] or Fig. 1 of [6] (MF) and [5] (MF and OC)
- (v) [3] (UC) and Fig. 11a of [4] (OC)
- (vi) Fig. 2 of [1] (UC)
- (vii) Fig. 1b of [1] (UC)

Table 1: Offset-error comparison of SC delay circuits ($A = 100$, $C_i/C_j = 1$)

SC delay circuits	Offset errors
Proposed Fig. 1	$\frac{\mu}{1 + 3\mu + 2\mu^2} v_{os} = 0.0097 v_{os}$
[5]	$\frac{\mu}{1 + 2\mu + \mu^2} v_{os} = 0.0098 v_{os}$
Fig. 11b of [4]	$\frac{2\mu}{1 + 5\mu + 6\mu^2} v_{os} = 0.0190 v_{os}$
[7] with extra reset switch	$\frac{2\mu}{1 + 4\mu + 4\mu^2} v_{os} = 0.0192 v_{os}$
Fig. 11a of [4]	$\frac{2\mu}{1 + \mu} v_{os} = 0.0198 v_{os}$
Fig. 2 of [1, 2]; Fig. 1 of [6]	$\simeq v_{os}$
Fig. 1b of [1, 3]	$\simeq 2v_{os}$

This circuit configured with the phases in parentheses (phase scheme B) in Fig. 1 will realise an anticipatory compensation scheme [4, 8] which accurately predicts gain error by a preliminary switching operation at phase 2 which will be stored in C_i in phase 1' and in turn be cancelled in the next phase 2'. Such a so-called successive anticipatory GOC scheme with its negligible, fairly small gain (<0.0042 dB) and phase error ($<0.01^\circ$) shown in Fig. 2 is almost frequency-independent. Moreover, this scheme requires fewer analogue components and no longer needs an S/H input in consecutive phases as required in the other schemes. Indeed it is especially suitable for sampling rate converters due to their multi-

rate nature. The extra error due to the charge division between C_1 and the parasitic on its left node during phase 1' can be eliminated by inserting a switch between C_1 and node x.

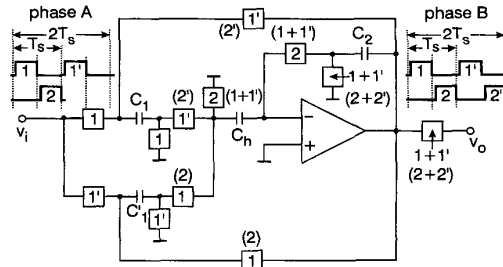


Fig. 3 Gain- and offset-compensated and mismatch-free SC z^{-1} (phase A) and $z^{-3/2}$ (phase B) delay circuits

Another advanced extension of this circuit is the simple and flexible realisation of an arbitrary delay period with one OA and the original compensation performance. For simplicity, the SC circuits with z^{-1} and $z^{-3/2}$ (parenthesised phases) delay, respectively, are proposed in Fig. 3 with the same architecture but different phases. The input sampling branches are doubled in parallel for delaying the input in a multiplexed manner. It can be straightforwardly extended to using n input branches with $n+1$ (or $2n$) phases for realising delay z^{-n} (or $z^{-(n+1/2)}$). Such a block is highly efficient in terms of required OAs when realising GOC delay lines (two OAs per unit delay by cascading conventional compensated units).

Conclusions: A new gain-, offset-compensated and mismatch-free SC delay circuit has been proposed with considerably better overall performances compared to other stereotyped compensated and uncompensated circuits, although it is indeed just a conservative study in view of the neglect of the mismatch problem in other SC delay circuits. A wideband and very precise successive-anticipatory gain compensation approach and a flexible arbitrary delay realisation with only one OA have also been investigated by simply modifying the original circuit. A good consistency between theoretical and simulated results of circuit behaviour has been achieved.

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