

The dispersal analysis on basis construction of digital predistortion techniques for power amplifiers

Yue Li¹ · Chak-Fong Cheang¹ · Pui-In Mak¹ · Rui P. Martins¹

Received: 19 May 2015 / Revised: 12 October 2015 / Accepted: 19 November 2015 / Published online: 28 November 2015
© Springer Science+Business Media New York 2015

Abstract Digital predistortion (DPD) exploiting the Volterra series can effectively compensate the strong nonlinearities (with memory effects) of power amplifiers. Diverse pruning schemes have been proposed to reduce the computational complexity with comparative performances. Regrettably, the mechanism of basis construction in different DPDs that is related to the complexity-efficiency tradeoff has not been well-studied. In order to compare *methodically* the Volterra-series based DPDs, the key parameters of the basis are studied here. Especially for the cross terms that describe the interaction between nonlinearities and memory effect, the complexity-efficiency tradeoff cannot be addressed directly. Thus, the basis construction of DPDs is firstly mapped to the general Volterra-series to observe the pruning property of each DPD. The diagonal dispersal property on basis construction is concluded as the most efficient and reliable way for pruning DPD techniques. The running complexity-accuracy tradeoff is quantitatively analyzed via the number of floating point operations. With the best performance settings found by the Qhull algorithm, the experimental results show that (1) the nonlinear order of the cross terms is more significant than the related memory depth, and (2) basis construction with diagonal dispersal properties effectively shows the complexity-efficiency tradeoff of

different DPDs. These results offer new angles to assess the feasibility of DPDs and their involved complexity.

Keywords Basis construction · complexity · Digital predistortion (DPD) · Floating point operations (FLOPs) · Nonlinearity · Power amplifier (PA) · Volterra series

1 Introduction

In modern communication systems, multicarrier non-constant envelope modulation techniques, such as orthogonal frequency-division multiplexing (OFDM), are common to boost the system throughput. With the high peak-to-average-power-ratio (PAPR) property of the OFDM signal, the power amplifier (PA) in the transmitter should operate at the small power-back-off regime to enhance the power efficiency, which however causes severe nonlinearities with memory effects. The resultant impairments are the spectral regrowth and degradation of error vector magnitude (EVM). Comparative analysis of PA behavioral models [1–3] has verified that Volterra-series based model provides the ability on describing the PA nonlinearities with memory effect. Thus, Volterra-series based digital pre-distortion (DPD) techniques [4–8] have been extensively studied in the literature. It is a multi-dimensional linear structure to include different order of *nonlinearities* and *memory effect*. Regrettably, its number of coefficients goes up exponentially. For realizing the predistorter in an Application-Specific Integrated Circuit or Field Programmable Gate Array, the running complexity is thus increased [9]. Besides, the accuracy of the coefficients extraction, which is based on the least square (LS) estimator [10] under indirect learning algorithm, is reduced. To minimize the number of coefficients, different DPDs have been derived in the literature based on pruned Volterra series with

Yue Li and Chak-Fong Cheang have contributed equally to this work.

R. P. Martins is leave from Instituto Superior Técnico, Universidade de Lisboa, Portugal.

✉ Pui-In Mak
pimak@umac.mo

¹ State-Key Laboratory of Analog and Mixed-Signal VLSI and Faculty of Science and Technology, Department of ECE, University of Macau, Macao, China

the tradeoff between complexity and efficiency. Memory polynomial (MP) DPD [5] simplifies the Volterra-series into a near-diagonal polynomial with respect to the static nonlinearities. Generalized memory polynomial (GMP) DPD [6] extends the MP by adding an extra degree of freedom on the memory terms. Dynamic-derivative-reduction (DDR) DPD [7] separates different dynamic orders of nonlinearities for the model restriction. The complexity-reduced Volterra series (CRV) DPD [8] is a novel structure derived from the feedback topology, providing high nonlinear orders and large memory depth.

This paper focuses on the basis construction analysis on different pruning techniques for memory DPDs including MP, 1st-order DDR (DDR1), 2nd-order DDR (DDR2), GMP and CRV, in terms of static nonlinear order, memory depth and the number of cross terms. To compare them properly, the key parameters related to DPD's basis construction are firstly introduced, and the dispersal property of these pruning techniques is then analyzed comprehensively using the general Volterra-series mapping method, prompting an extensive discussion on their key properties. The complexity-accuracy of the basis construction of memory DPDs can thus be predicted. Simulations on complexity-accuracy are based on the number of floating point operations (FLOPs) using the Qhull algorithm. The measurement results are discussed and a summary of insights obtained from the comparison is given.

2 Dispersal properties of DPD structures

Here the key parameters and dispersal analysis on basis construction of different DPD structures are addressed with respect to the general Volterra series. The efficiency related to the running complexity is analyzed for different DPDs.

2.1 General Volterra series

The Volterra series is essentially a nonlinear polynomial with a combination of linear convolution so that it can be used to model the PA nonlinearities with the fading memory. In the first frequency zone, a general Volterra PA baseband model can be written as

$$y[n] = \sum_{p=1}^P \sum_{m_1=0}^M \sum_{m_2=m_1}^M \cdots \sum_{m_{(p+1)/2}=m_{(p-1)/2}}^M \sum_{m_{(p+3)/2}=0}^M \sum_{m_p=m_{p-1}}^M h_p(m_1, m_2, \dots, m_p) \prod_{r_1=1}^{(p+1)/2} x[n-m_{r_1}] \prod_{r_2=(p+3)/2}^p x^*[n-m_{r_2}] \quad (1)$$

where $x[n]$ and $y[n]$ are the complex envelope of the PA input and output signals, respectively. $h_p(m_1, m_2, \dots, m_p)$ is the Volterra kernel of p dynamics. M is the truncated memory depth. P is the truncated nonlinear order.

The number of the kernels grows exponentially according to the increase of P and M for tackling severe nonlinearities and memory effect, which also increases the cost for model identification and DPD running. Simplified DPDs are thus developed in [5–8] based on different pruning schemes to lower the complexity for practical applications. Following a comprehensive way to analyze and compare those Volterra-series based DPDs is provided.

2.2 Key parameters on construction of DPDs

The basis is constructed based on several key parameters. Besides the conventional *static nonlinear order* P and *memory depth* M in the literature, the *dynamic order* r and *cross-term* K are also involved into the analysis. All the parameters are utilized in the following as metrics to acquire a comprehensive analysis of each DPD's characteristic:

- *Static nonlinear order* P describes the truncated order of static, memoryless nonlinearities where P is an odd number. In DPD, it is the most important index to describe the PA nonlinearities. All DPDs has the same order of dynamic nonlinear and static nonlinear terms. Except for CRV, its dynamic nonlinear order is $2P - 1$ due to the involvement of the first instance of the feedback FIR filter [8].
- *Memory depth* M describes the truncated memory length. The $x(n - m)$ related terms represent the memory effects in the basis construction, where $m = 1, 2, 3, \dots, M$.
- *Dynamic order* r describes the interaction between the static nonlinearities and linear/nonlinear memory effects, which counts the number of delayed items included in the multiplication. For example, $x(n) |x(n)|^{p-r-1} |x(n - m_1)| |x(n - m_2)| \cdots |x(n - m_r)|$ is a basis term with nonlinear order p and dynamic order r .
- *Cross-term* K describes the numbers of nonlinear memory effects included in each DPD. Different DPD structure will have a significant different on this number with different delays, for example, $x(n - m_1) |x(n - m_2)| |x(n - m_3)| \cdots |x(n - m_p)|$ with at least two different m_i where $i = 1, 2, \dots, p$. However, the number K cannot effectively talk the effectiveness of each DPD. The formula about K can mainly indicate the importance of the cross terms to each DPD. A more intuitive illustration on cross-term construction is provided in the next section.

Table 1 Key parameters of each DPD

DPD	Basis	r	K
MP	$x[n - m] x[n - m] ^{p-1}$	P	0
DDR1	$x[n] x[n] ^{p-1}$	1	PM
DDR2	$x[n - m_1] x[n] ^{p-1}$	2	$\frac{p+1}{2}M + \frac{p-1}{2}\left(M + \frac{M(M+1)}{2} + M^2\right) + \frac{p-3}{2}\frac{M(M+1)}{2}$
	Basis of DDR1		
	$x[n - m_3]x[n - m_4]x^*[n] x[n] ^{p-3}$		
	$x[n - m_5]x^*[n - m_6]x[n] x[n] ^{p-3}$		
GMP	$x^*[n - m_7]x^*[n - m_8]x^3[n] x[n] ^{p-5}$	P	* $G(M + 1)(P - 1)/2$ + $\frac{p-1}{2}\frac{M(M+1)}{2}$
	Basis of MP		
	$x[n - m] x[n - m - g] ^{p-1}$		
CRV	$x[n - m] x[n - m + g] ^{p-1}$	P	$(P^2 + 1)M/2$
	$x[n] x[n] ^{p-1}$		
	$x[n] x[n] ^{p-3} x[n - m] ^{k-1}$		
	$x[n - m] x[n] ^{p-1} x[n - m] ^{k-1}$		

* G represents the leading/lagging depth for GMP

These key parameters relate directly to the effectiveness and complexity of each DPD. A comparison for different DPDs is exhibited in Table 1. The same *memory depth* M is shared by all DPDs. r and K can be expressed by P , M and G based on each DPD’s structure. Especially, the cross terms are essential for a DPD structure to calibrate severe nonlinearities and nonlinear memory effects. Cross-term K is directly related to the basis construction and the mechanism of the dynamic-term expansion of each DPD. Analysis on this is crucial for all DPDs.

2.3 Analysis on basis construction

In the parameter extraction stage, each column of the signal matrix is constructed based on the considered nonlinearities and memory effects of different DPD structures as shown in Table 1. This defines the DPD basis constructions.

Considering the mechanism of basis construction, MP is the extension of the memoryless polynomial with unit delay dynamic and thus no cross terms involved in its basis. For DDR, different dynamic orders are separated and thus can be controlled. GMP adds lagging and/or leading factor to MP as an extra degree of freedom to gain additional cross terms for wideband calibrating purpose. CRV involves dynamic terms as multiplying memory polynomial by static nonlinearities. It provides representative basis terms with great disparity, high dynamic order and large number of cross terms which are directly proportional to P^2 .

Accordingly, for different DPDs a more intuitive view about the mechanism of the basis constructions is provided by the two basis-mapping diagrams in Fig. 1. The diagram

is mainly mapping the basis of each DPD back to the general Volterra series to highlight which term is preserved and which is pruned individually. Third- and fifth-order basis are shown as an exploration on the dimension of nonlinear order P . Memory depth M is set to 2 ($m = 0, 1, 2$), which is adequate for all DPDs to show their features on how to involve nonlinear, dynamic and cross terms. For instance, CRV occupies a basis with $(m_1, m_2, m_3) = (0, 2, 2)$ and $(m_4, m_5) = (0, 2)$ in Fig. 1(b). It means that term $x(n)x(n - 2)x(n - 2)x^*(n)x^*(n - 2)$ is involved in the basis construction for CRV with $P = 5, M = 2$.

Different properties of each DPD can be acquired based on the feature of corresponding basis dispersal. The simplicity of MP can be directly observed by its only diagonal allocation and small number of terms with no cross terms involved. DDR1 and DDR2 have the same manner that basis terms are concentrated at the upper-left region near the static nonlinearity ($m_{1-5} = 0$). Moreover, from Fig. 1(b), DDR2 involves much more dynamic terms than DDR1 by expanding along the frame with $r = 2$. GMP and CRV are both allocated along the diagonal as an expanded MP and diagonal of $m_1 = 0$, whereas CRV has more uniformly distributed basis than GMP which only assigns terms on particular memory delays (vertical lines).

All these phenomena are originated from the nature of the DPDs’ structural formulations. DDR is highly concentrated with terms positioned beside one another, which leads to a greater concern of its efficiency in practices. MP, GMP and CRV are more dispersive, while CRV seems to have the highest uniformity and continuity with a wide range basis allocation.

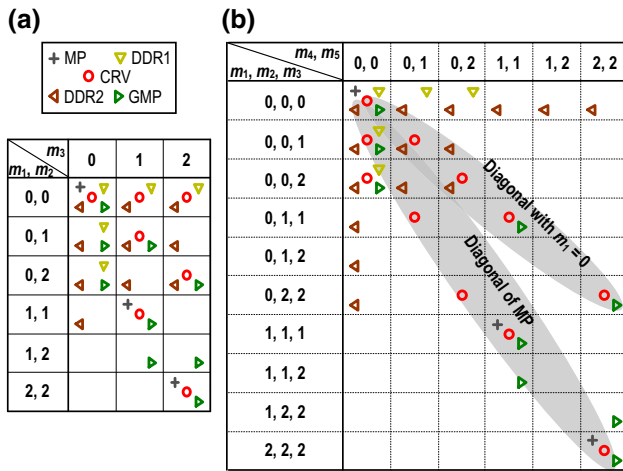


Fig. 1 Basis mapping diagrams of **a** $x(n - m_1)x(n - m_2)x^*(n - m_3)$ and **b** $x(n - m_1)x(n - m_2)x(n - m_3)x^*(n - m_4)x^*(n - m_5)$ for different DPDs

2.4 Complexity

Considering the DPD extraction process can be optimized and executed offline [3, 11], the *running complexity* which should be utilized for each DPD output is of the major concern. The *total number of coefficients* L and the basis-construction complexity in terms of FLOPs indicating the overall running complexity [3] of each DPD in terms of the key parameters are presented in Table 2. K takes a significant portion in L for most DPDs, which is the dominant source of complexity. Thus, K acts as a basic indicator of a memory DPD’s complexity where cross terms are crucial and related to the basis construction mechanism analyzed before.

Some basic information about each DPD can be gained from Table 2. MP has the lowest complexity as there is no cross term included. For DDR1, it describes only the 1st order dynamic and small amount of cross terms. Thus, for low-complexity-oriented applications, MP and DDR1 should be the potential candidates. DDR2, GMP and CRV

include higher dynamic order and more cross terms with heavier burden of complexity. The experimental results are reported next to show the complexity-efficiency tradeoff of each DPD with respect to their basis construction.

3 Experimental results

Based on our fair complexity-accuracy comparison of different pruning DPD techniques, the best performance parameters are determined by searching with a wide range of different nonlinear order P and memory depth M . Thus, >150 sets of parameters are simulated under various complexity with promising accuracy. By using the Qhull algorithm (Qhull 2012, Available: <http://www.qhull.org>), the best performance line is taken, which represents the best configurations of each pruning DPD [3]. The most complexity-efficient parameter settings were chosen for the forward validation, which allows comparing the effectiveness of each DPD.

For the experimental setup (Fig. 2), an Agilent E4438C vector signal generator (VSG) is employed to generate the test signal. The DUT is a commercial MAX2242 PA from Maxim Integrated. It operates at 2.4–2.5 GHz, with a power gain of 28.5 dB and a linear output power of +22.5 dBm. An Agilent DSO91304A oscilloscope synchronized by a 10-MHz trigger signal with the VSG, is utilized to capture the DUT’s input and output for further signal processing in MATLAB. The DUT is operated at 3.4-dB relative back-off from the 1-dB compression point (P_{1dB}).

The test data is a 20-MHz bandwidth, 64-QAM OFDM signal with 8.03-dB PAPR, 52 active subcarriers out of 64, 312.5-kHz subcarrier spacing and 5× oversampling. The test signal modulated to a 2.44-GHz carrier inherently has a 0.83 % EVM and ACPR of (−50.5, −50.4 dBc). Different sets of data are captured for extraction and validation separately. Each set contains 16,000 samples with 50

Table 2 Complexity of each DPD

DPD	Coefficient number (L)	Complexity of basis construction
MP	$(M + 1)(P + 1)/2$	$3 + (P - 1)$
DDR1	$(1 + M)(P + 1)/2$	$9 + (M + 1)(P - 1)$
	$+M(P - 1)/2$	$+6M(P - 3)/2$
DDR2	$\frac{P+1}{2}(1 + M) + \frac{P-1}{2}M^2$	$15 + 6M + (M + 1)(P - 1)$
	$+M + \frac{M(M+1)}{2} + \frac{P-3}{2} \frac{M(M+1)}{2}$	$+6M(\frac{P-3}{2}) + 6(\frac{P-3}{2})(M^2 + \frac{M(M+1)}{2}) + 6(\frac{P-5}{2}) \frac{M(M+1)}{2}$
GMP	$(M + 1)[\frac{P+1}{2} + G(P - 1)/2]$	$3 + P - 1 + (P - 3)G$
	$+ \frac{P-1}{2} \frac{M(M+1)}{2}$	$+(P - 3)M(M + 1)/2$
CRV	$(P + 1)/2 + (P^2 + 1)M/2$	$3 + (P - 1) + 2PM$

Fig. 2 a Block diagram of measurement setup and b photograph of DUT (MAX2242) for DPD identification and forward validation

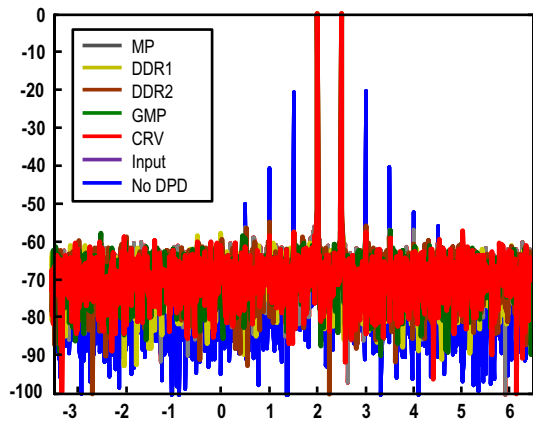
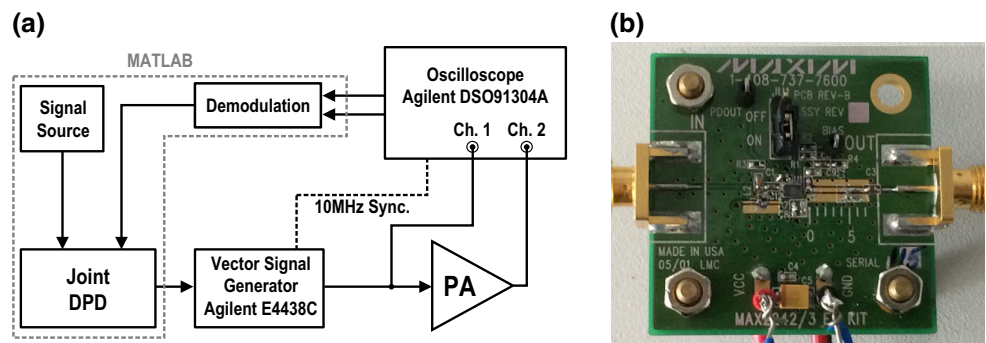


Fig. 3 Measured spectra of two-tone test, with the input, output without DPD, and output with different kinds of DPDs

OFDM symbols to ensure that at least 200 parameters can be accurately estimated [10].

In order to validate the performance of the DPDs, EVM is used as the measure of time-domain-signal accuracy and adjacent channel power ratio (ACPR) is used for measuring the spectral accuracy. The simulated convex hulls are searched for representing the best performance lines of each DPD with respect to EVM and ACPR versus FLOPs as plotted in Fig. 4, respectively. Cross terms can count a nonlinear time-lagging property related to its memory effect in different DPDs technique. The DPDs’ time-domain-signal accuracy (i.e., EVM) are sensitive to their dispersal properties as shown in both simulations and measurements. In the two-tone test at 2 and 2.5 MHz, all the intermodulation tones of different DPDs are suppressed

to -56.0 dB, which are shown in Fig. 3 and Table 3. For a low output power of 16.5 dBm from the DUT, the EVM and ACPR is 7.36 % and $(-34.2, -32.4$ dBc) without DPD. With DPD, EVM and ACPR of different DPDs are improved similarly up to 1.8 % and -43.7 dBc as the cross terms are insignificant as shown in Fig. 4(a), (b). For complexity-efficiency issue, less numbers of FLOPs are used on diagonal-allocated DPDs (MP, GMP and CRV) in two-tone test and low output power case. For a high output power of 19.5 dBm, the EVM and ACPR is 22.41 % and $(-20.5, -19.6$ dBc). The two figures of DDR2 are improved up to 3.67 % and -36.7 dBc with FLOPs = 925. Both GMP and CRV have better performances as their basis locate on the diagonals (Fig. 1) which represent a wide range of cross terms with significant disparities. In Fig. 4(c), EVM and ACPR of GMP is better for low complexity application (FLOPs < 400), which is simulated. CRV has the best performance on EVM reduction when the complexity restriction is relaxed ($500 < \text{FLOPs} < 800$). From Fig. 4(d), all DPDs show similar performances on ACPR reduction except MP. The extraction of MP diverges when the complexity increases, which has been experienced by [12]. The main reason is with $P \geq 15$, further increase of memory depth in the basis may lead crisis to the performance improvements (FLOPs < 1000). Thus, the best performance parameters for forward validation are selected within this range for the comparison of all the DPDs.

Additionally, a study on the best performance parameters of each DPD is utilized as shown in Fig. 5. Individual parameter setting is pointed respect to P and M separately on EVM and ACPR reduction. Figure 6(a), (b) have the

Table 3 Corresponding simulated and experimental calibrating performances in two-tone test

DPD	Parameters (P, M, G)	FLOPs	$\text{IM3}_{\text{max, sim}}$	IM3_{mea}
MP	15, 1, -	143	-62.2	$(-56.4, -56.2)$
DDR1	11, 1, -	187	-60.3	$(-54.4, -54.6)$
DDR2	11, 1, -	377	-61.5	$(-54.8, -54.7)$
GMP	11, 1, 1	243	-59.6	$(-53.9, -54.1)$
CRV	5, 1, -	143	-60.0	$(-56.0, -56.2)$

Fig. 4 Simulated best performance lines of different DPDs represented by **a** EVM versus FLOPs and **b** ACPR versus FLOPs in low power mode; **c** EVM versus FLOPs, and **d** ACPR versus FLOPs in high power mode

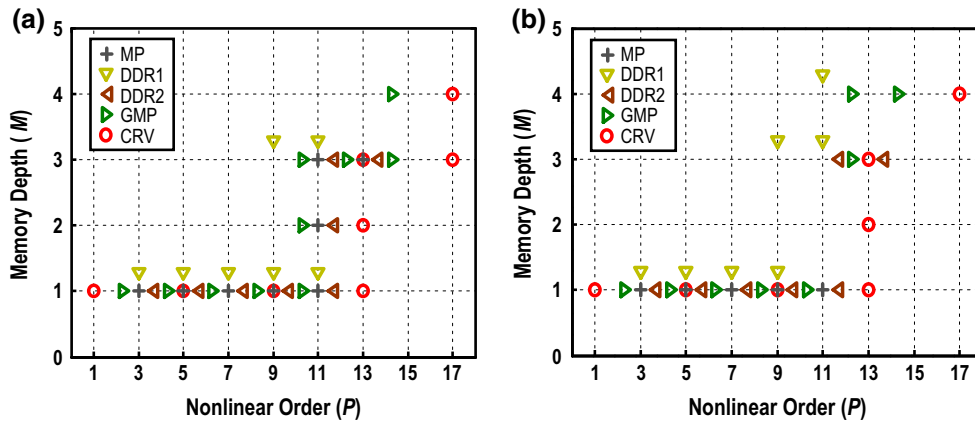
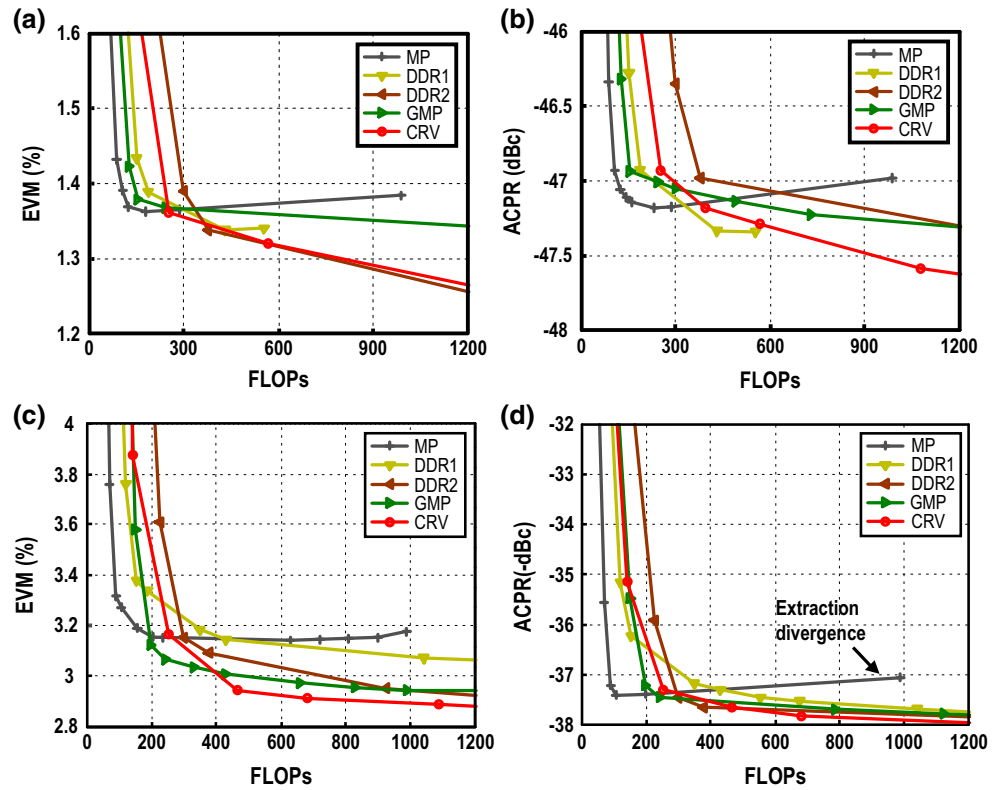


Fig. 5 Distribution of the best performance parameters of the simulated results on **a** EVM reduction [Fig. 3(a)] and **b** ACPR reduction [Fig. 3(b)]

same trend about the parameter setting for all DPDs to achieving best performance. The ‘]’ shape distribution indicates that the basis constructions for low complexity applications (FLOPs < 600) are concentrated mostly on the nonlinearities with low-memory cross terms. In other words, the parameters are applied better with high nonlinear order rather than large memory depth if the complexity is restricted.

Based on the simulated performance of both EVM and ACPR reduction, respect to Figs. 4 and 5, the selected best

performance parameters of each DPD are listed in Tables 4, 5, 6, and 7. The measured performances of each DPD are presented. In low power mode [Fig. 6(a), (b)], EVM and ACPR of the five considered DPDs have the same performance consistent with the simulations. Among the five considered DPDs in high power mode [Fig. 6(c), (d)], MP and DDR1 perform worse than the other three. GMP and DDR2 are similar having moderate performances. CRV outperforms others consistently on forward validation.

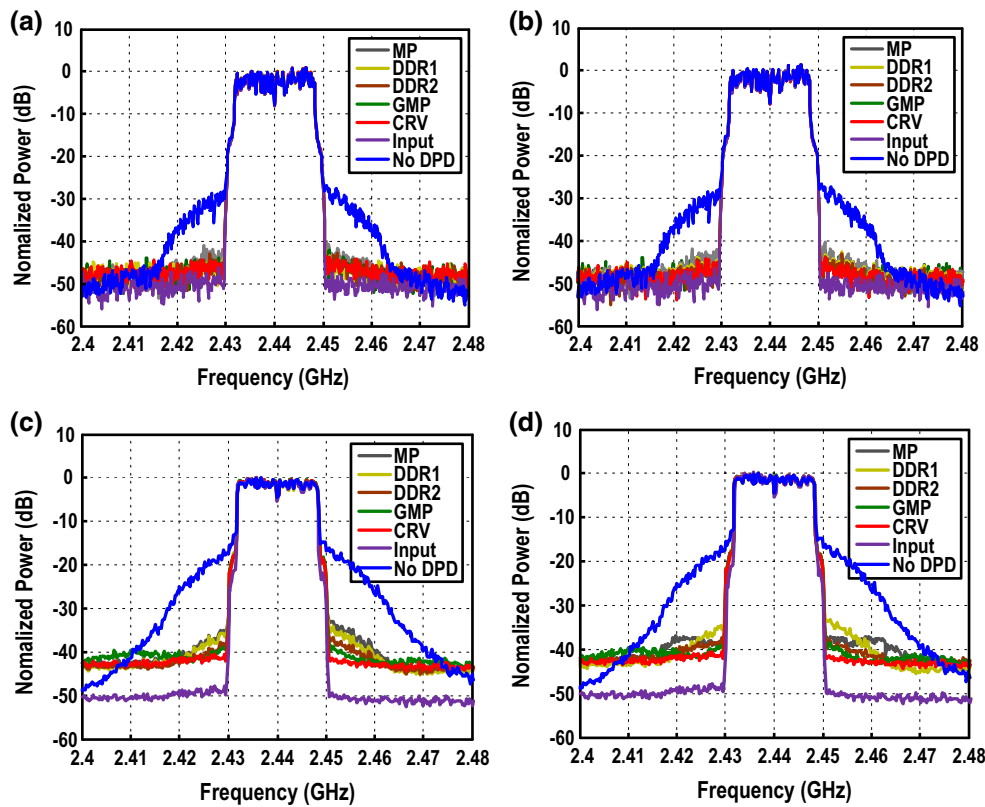


Fig. 6 Measured spectra of the system input, output without DPD and output with different kinds of DPDs: **a** DPDs with EVM-based parameters (Table 4) and **b** with ACPR-based parameters (Table 5) in

low power mode; **c** DPDs with EVM-based parameters (Table 6) and **d** DPDs with ACPR-based parameters (Table 7) in high power mode

Table 4 EVM-based selected parameters. Corresponding simulated and experimental calibrating performances in low power mode

DPD	Parameters (P, M, G)	FLOPs	EVM_{sim}	EVM_{meas}	$ACPR_{meas}$
MP	13, 1, –	181	1.36	2.02	(–43.1, –42.4)
DDR1	11, 1, –	187	1.39	1.72	(–44.1, –43.8)
DDR2	9, 1, –	301	1.39	1.78	(–43.7, –43.3)
GMP	11, 1, 1	243	1.37	1.92	(–42.7, –42.6)
CRV	7, 1, –	253	1.36	1.80	(–43.7, –43.5)

Table 5 ACPR-based selected parameters. Corresponding simulated and experimental calibrating performances in low power mode

DPD	Parameters (P, M, G)	FLOPs	$ACPR_{max, sim}$	EVM_{mea}	$ACPR_{mea}$
MP	15, 1, –	197	–48.07	2.08	(–43.0, –42.9)
DDR1	11, 3, –	431	–48.36	1.77	(–44.0, –43.5)
DDR2	11, 1, –	377	–47.53	1.77	(–44.0, –43.5)
GMP	11, 1, 1	243	–47.65	1.92	(–43.5, –43.6)
CRV	7, 1, –	253	–48.03	1.76	(–44.0, –43.7)

Besides, the predistorted accuracy of each DPD is of concern as shown in Tables 4, 5, 6, and 7. In Tables 4 and 5, similar simulated performances are chosen in the comparison. Basis construction with diagonal dispersal properties proves its complexity-efficiency. In Tables 6 and 7,

all results are degraded when compared with those from simulations. This is due to various kinds of systematic noise and imperfections. The crucial one is the quantization noise from both the VSG and oscilloscope, especially because the DUT is a medium-power PA. DDR2, GMP and

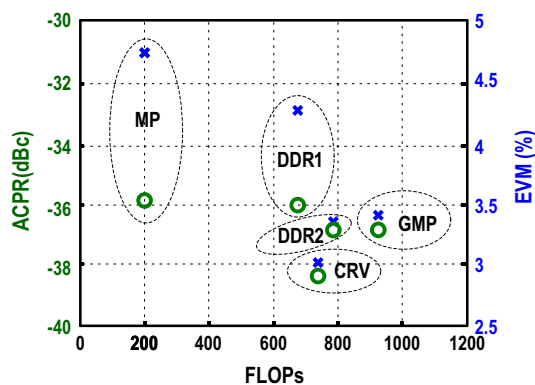
Table 6 EVM-based selected parameters. Corresponding simulated and experimental calibrating performances in high power mode

DPD	Parameters (P, M, G)	FLOPs	EVM_{sim}	EVM_{meas}	$ACPR_{meas}$
MP	13, 10, –	629	3.144	4.204	(–35.2, –34.2)
DDR1	11, 3, –	431	3.144	4.585	(–36.0, –33.8)
DDR2	11, 2, –	925	2.952	3.466	(–36.7, –36.0)
GMP	13, 3, 2	989	2.947	3.368	(–36.7, –36.4)
CRV	7, 3, –	681	2.916	3.057	(–36.8, –36.9)

Table 7 ACPR-based selected parameters. Corresponding simulated and experimental calibrating performances in high power mode

DPD	Parameters (P, M, G)	FLOPs	$ACPR_{max, sim}$	EVM_{mea}	$ACPR_{mea}$
MP	21, 1, –	197	–37.34	4.752	(–36.4, –33.8)
DDR1	11, 5, –	675	–37.53	4.263	(–36.3, –34.6)
DDR2	11, 2, –	925	–37.66	3.466	(–37.1, –35.7)
GMP	13, 3, 1	787	–37.69	3.417	(–37.1, –36.2)
CRV	7, 3, –	681	–37.84	3.057	(–36.8, –36.9)
	9, 2, –	741	–37.76	3.027	(–38.3, –37.0)
	9, 3, –	1087	–37.93	3.046	(–38.0, –37.1)

Best performance values indicate the bold

**Fig. 7** Measured ACPR and EVM performances of different DPDs in high power mode

CRV perform similarly in simulations, but are quite different in measurements since they tackle different nonlinear memory effect on their basis constructions. For the complexity-efficiency tradeoff in high power mode, the measured ACPR and EVM performance of different DPDs are compared in Fig. 7. CRV tackles the nonlinearity and memory effect with promising ACPR and EVM accuracy.

By synthesizing the above observations with the structure of each DPD, several important inferences can be drawn: *nonlinear order is essential*. All DPDs in the measurement require at least 11th order of overall nonlinearities. *Memory depth is less crucial*. To enhance this inference, additional configurations of CRV are explored

from the selected best performance parameter as shown in Table 7. ACPR and EVM are measured by using CRV with three different sets of parameters are listed in Table 7. *The CRV with $P = 9, M = 2$ outperforms the ones with $P = 7, M = 3$, which validates that nonlinearities are more essential*. For the complexity-efficiency tradeoff, *most DPDs are forward validated with $M \leq 3$* (Table 5) since the complexities of most DPD structures grow exponentially with the increase of memory depth. Finally, *larger numbers of coefficients L and dynamic order r do not necessarily indicate better performance*. It even leads crisis to the extraction process when the numbers are too large. Yet, *greater disparities among the basis terms* represented by the group of GMP and CRV in Fig. 1 do help with the calibration, and increase the practicability of the DPD structure. CRV has more uniformly distributed basis than MP and GMP as discussed in Sect. 2.3, which contributes to its outstanding performance.

4 Conclusions

This paper proposed a methodical way to analyze different DPDs showing their complexity-accuracy trade-off. Several popular DPD structures have been studied and compared based on a comprehensive analysis on the mechanism of their basis construction, using their several key parameters and the basis mapping method. The dispersal property does

help the analysis of the construction of DPD. For complexity-efficiency issue, CRV outperforms others consistently and achieves the best DPD practicability in both simulations and experiments. The results also offer adequate insights about the studied DPDs. Essentially, overall non-linear order and cross terms with significant disparity and representativeness are crucial to each DPD's performance.

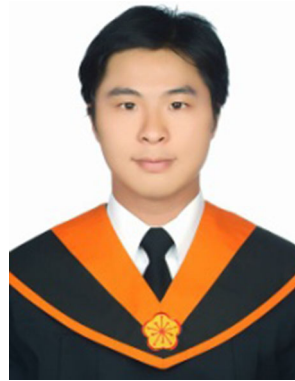
Acknowledgments This work is funded by the Macau Science and Technology Development Fund (FDCT) – SKL Fund and the University of Macau - MYRG2015-00040-FST.

References

- Pedro, J. C., & Maas, S. A. (2005). A comparative overview of microwave and wireless power-amplifier behavioral modeling approaches. *IEEE Transactions on Microwave Theory and Techniques*, 53(4), 1150–1163.
- Isaksson, M., Wisell, D., & Ronnow, D. (2006). A comparative analysis of behavioral models for RF power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 54(1), 348–359.
- Tehrani, A. S., Cao, H., Afsardoost, S., Eriksson, T., Isaksson, M., & Fager, C. (2010). A comparative analysis of the complexity/accuracy tradeoff in power amplifier behavioral models. *IEEE Transactions on Microwave Theory and Techniques*, 58(6), 1510–1520.
- Mirri, D., et al. (2002). A modified Volterra series approach for nonlinear dynamic systems modeling. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 49(8), 1118–1128.
- Kim, J., & Konstantinou, K. (2001). Digital predistortion of wideband signals based on power amplifier model with memory. *IET Electronics Letters*, 37(23), 1417–1418.
- Morgan, D., Ma, Z., Kim, J., Zierdt, M., & Pastalan, J. (2006). A generalized memory polynomial model for digital predistortion of RF power amplifiers. *IEEE Transactions on Signal Processing*, 54(10), 3852–3860.
- Zhu, A., Pedro, J., & Brazil, T. (2006). Dynamic deviation reduction based Volterra behavioral modeling of RF power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 54(12), 4323–4332.
- Mkadem, F., Fares, M. C., Boumaiza, S., & Wood, J. (2014). Complexity-reduced Volterra series model for power amplifier digital predistortion. *Analog Integrated Circuits and Signal Processing*, 79(2), 331–343.
- Gilbert, P. L., Montoro, G., & Bertran, E. (2011). FPGA implementation of a real-time NARMA-based digital adaptive predistorter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 58(7), 402–406.
- Ljung, L. (1999). *System identification: Theory for the user* (2nd ed.). Englewood Cliffs: Prentice-Hall.
- Suryasarman, P., Liu, P., & Springer, A. (2014). Optimizing the identification of digital predistorters for improved power amplifier linearization performance. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 61(9), 671–675.
- Liu, Y., Zhou, J., Chen, W., & Zhou, B. (2014). A robust augmented complexity-reduced generalized memory polynomial for wideband RF power amplifiers. *IEEE Transactions on Industrial Electronics*, 61(5), 2389–2401.



Yue Li received the B.Sc. and M.Sc. degrees in electrical and computer engineering from the University of Macau, Macao SAR, China, in 2012 and 2015, respectively, at the UM State-Key Laboratory of Analog and Mixed-Signal VLSI and Faculty of Science and Technology (ECE).



Chak-Fong Cheang received his B.Sc. and his M.Sc. degree in Dept. of Engineering Science from National Cheng Kung University (NCKU), Tainan, Taiwan, in 2008, 2010. He is currently working toward the Ph.D. degree at the UM State-Key Laboratory of Analog and Mixed-Signal VLSI and Faculty of Science and Technology (ECE) from University of Macau, Macao, China. His research interests are digital predistortion and digital mitigation on RF impairment and field-programmable gate-array (FPGA)-based embedded signal processing.



Pui-In Mak (S'00-M'08-SM'11) received the Ph.D. degree from University of Macau (UM), Macao SAR, China, in 2006. He is currently Associate Professor at UM, and Coordinator of the Wireless & Biomedical Research Lines of the *State-Key Laboratory of Analog and Mixed-Signal VLSI*. His research interests are on analog and RF circuits and systems for wireless, biomedical and physical chemistry applications. His involvements with IEEE are: Distinguished Lecturer ('14–'15) and Member of Board-of-Governors ('09–'11) of IEEE Circuits and Systems Society (CASS); Editorial Board Member of IEEE Press ('14–'16); Senior Editor of IEEE Journal on Emerging and Selected Topics in Circuits and Systems ('14–'15); Associate Editor of IEEE Transactions on Circuits and Systems Part I (TCAS-I) ('10–'11, '14–); Associate Editor of IEEE Transactions on Circuits and Systems Part II (TCAS-II) ('10–'13), and Guest Editor of IEEE RFIC Virtual Journal ('14). Prof. Mak received IEEE DAC/ISSCC Student Paper Award'05; IEEE CASS Outstanding Young Author Award'10; National Scientific and Technological Progress Award'11; Best Associate Editor for TCAS-II'12–'13. In 2005, he was decorated with the *Honorary Title of Value* for scientific merits by the Macau Government.



Rui P. Martins (M'88-SM'99-F'08), born in April 30, 1957, received the Bachelor (5-years), the Masters, and the Ph.D. degrees, as well as the *Habilitation* for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992 and 2001, respectively. He has been with the Department of Electrical and Computer Engineering (DECE)/IST, TU of Lisbon, since October 1980. Since 1992, he is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor since August 2013. In FST he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since

1997, being Vice-Rector (Research) since 2008. He created in 2003 the *Analog and Mixed-Signal VLSI Research Laboratory* of University of Macau, elevated in January 2011 to State Key Laboratory of China (the 1st in Engineering in Macao), being its Founding Director. Prof. Rui Martins is an *IEEE Fellow*, was the Founding Chairman of IEEE Macau Section (2003–2005), and IEEE Macau Joint-Chapter on CAS/COM (2005–2008) [2009 *World Chapter of the Year* of the *IEEECAS Society*]. He was Vice-President for Region 10 of *IEEE CASS* (2009–2011), Vice-President (World) Regional Activities and Membership of *IEEE CASS* (2012–2013), and Associate Editor of *IEEE T-CAS II: Express Briefs* (2010–2013), nominated *Best Associate Editor* for 2012 to 2013. Plus, he was a member of the IEEE CASS Fellow Evaluation Committee (Classes of 2013 and 2014). He was the recipient of 2 government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.

neering (DECE)/IST, TU of Lisbon, since October 1980. Since 1992, he is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor since August 2013. In FST he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since