Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters

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***Abstract*—The use of the polyphase decomposition technique applied to the noise transfer function (NTF) of band-pass sigma-delta ($\mathbf{BP\Sigma\Delta}$) modulators is introduced and theoretically analyzed. Schemes for a second-order and fourth-order band-pass noise shaping are discussed in detail. The method is usable for any order but the analog inaccuracy limits its application. It is shown that an extension to MASH configurations is possible. The method allows tunability of the centre frequency over a wide frequency range. Moreover, MASH schemes allow a rough-fine tuning with the rough tuning in the analog section followed by a fine digital adjustment. Simulation results verify the benefits and outline possible limits.**

***Index Terms*—Band-pass, noise transfer function, polyphase decomposition, sigma-delta modulators, tunability.**

I. Introduction

THE PRESENT trend in communication systems is to place the ADC as close as possible to the antenna. This maximizes the signal processing in the digital domain and realizes the so-called software defined radio (SDR) [1], [2]. The very high speed granted by scaling of CMOS nanometer technologies allows designing analog blocks running at GHz; this will lead, in the near future to analog interface of wireless receivers just made by an LNA and a band-pass ADC that will select the used frequency band, as shown in Fig. 1. The ADC must be tunable over a wide frequency range allowing the receiver to be able to support multiple standards.

Band-pass sigma delta ($\mathrm{BP\Sigma\Delta}$) converters are very convenient solutions because the shaping of the quantization noise occurs only in the frequency band of the signal. The noise outside that region is then removed in the digital domain. In the literature there are many examples of $\mathrm{BP\Sigma\Delta}$ implementations [3]–[8]. They use various techniques to realize the BP noise transfer function (NTF). Many of them are based on the use of resonators that replace the integrators of low-pass (LP) $\Sigma\Delta$ architectures. The circuit implementations can use the discrete time (DT) [9]–[15] or the continuous-time (CT) approach [16]–[20]. DT architectures replace the resistors or the transconductors used in the integrator with a switched capacitor circuit. This ensures a better accuracy and linearity, while speed and power are normally penalized. However, with Si-CMOS nanometer technologies it will be possible to operate DT modulators with very high sampling frequencies [21] that are reaching the GHz range and this opens new possibilities to band-pass DT solutions with band-pass response centered in the many hundred mega-Hz or even giga-Hz range.

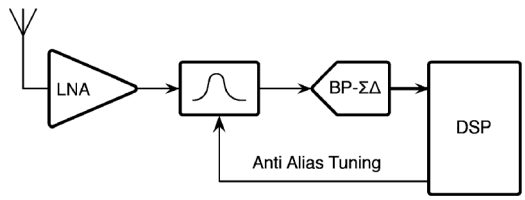

Fig. 1. Software-radio receiver with a directly sampled band-pass ADC and tunable anti-aliasing filter.

For software-radio applications obtaining tunability in a wide frequency range is important. Also ensuring accuracy of the band-pass frequency and having a solid link with the clock frequency is crucial. Conventional solutions control the band-pass frequency by tuning resonators. However, the frequency shift is limited because of the request on the quality factor Q of the resonant loop [22]. Therefore, in practice, the maximum shift is limited.

Changing z^{-1} to $-z^{-2}$ transforms the integrator block into the resonator. The zeros of the NTF of a LP $\Sigma\Delta$ modulator move around $\pm j$ on the unity circle. The method, as we will see shortly, is a simple implementation of the polyphase decomposition. The circuit uses two equal paths running at half of the clock frequency. A possible mismatch between the two paths, however, causes tones. An offset mismatch gives rise to a tone at $f_N/2$, where f_N is the Nyquist frequency; a gain mismatch $(1+\epsilon_G)$ determines a mirrored tone with amplitude $\epsilon_G V_{in}$. Both tones fall in the band-pass region. Timing mismatch imposes mirrored tones that fall in the same locations of one generated by gain mismatch. As shown in this paper, the choice of a proper

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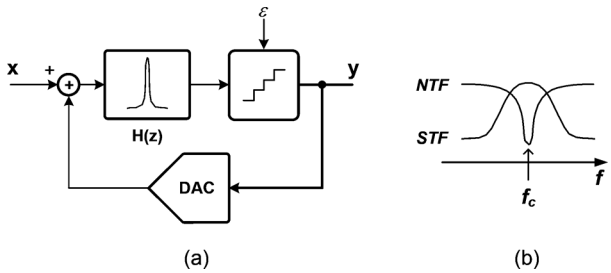

Fig. 2. (a) Conceptual scheme of a band-pass modulator. (b) Typical STF and NTF.

architecture leads to polyphase interleaved sigma-delta modulators mismatch-free, an important property that makes them superior to their conventional interleaved counterparts.

The class of architectures studied here does not use resonators and avoids spur tones in the signal band. Those architectures are based on the polyphase decomposition applied only to the NTF of band-pass modulators (or to any other NTF responses). The signal transfer function (STF) remains unchanged with respect to the originating single path.

This paper is organized as follows. Section II recalls conventional methods proposed in the literature. Section III describes the polyphase method for obtaining a desired NTF. Section IV analyzes circuits used in the implementation; Sections V and Section VI focus on low-order and high-order architectures. Section VII presents polyphase MASH schemes. Tunability is studied in Sections VIII and Section IX; Finally, the conclusions are given in Section X.

II. Tunable Band-Pass ΣΔ Architectures

A BPΣΔ modulator consists of a quantizer, a band-pass loop filter $H(z)$ and a feedback digital-to-analog converter (DAC). The conceptual scheme and the expected STF and NTF are shown in Fig. 2 [23], the center frequency f_c of the band-pass loop filter correspond to the zeros of the NTF. The transfer function of a BPΣΔ modulator can be derived as

$$Y(z) = \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)\epsilon(z) \tag{1}$$

where $\epsilon(z)$ is the quantization error.

To realize a DT BPΣΔ modulator normally it first starts from a LPΣΔ prototype, then the integrators in the modulator loop are replaced with resonators by an appropriate LP-to-BP transformation. To design a tunable BPΣΔ modulator in this way there are two possible transformation approaches, either to change the loop coefficients or to change the sampling frequency [24].

A. Changing the Loop Coefficients

In general, there are two types of architectures proposed to change the loop coefficients. First, using a DT loop filter based on a tunable resonator expressed in the $z-$domain as [25]

$$H_{\mathrm{BP}}(z) = \frac{\alpha z^{-1} - z^{-2}}{1 - 2\alpha z^{-1} + z^{-2}} \tag{2}$$

where α is the only tuning parameter between -1 and 1, resulting in the corresponding f_c of the band-pass filter changing from DC to half of the sampling rate $(f_s/2)$.

The tunable resonator of (2) is obtained from the integrator with one delay by the following transformation

$$z^{-1} \rightarrow \frac{z^{-2} - \alpha z^{-1}}{\alpha z^{-1} - 1} \quad \text{and} \quad \alpha = \frac{cos(\omega_c)}{cos(B/2)} \tag{3}$$

where ω_c is the center angular frequency and B is the bandwidth of the pass-band.

This architecture is first implemented in [26] using double sampling techniques, then a tunable DT BPΣΔ modulator based on the cascade of the tunable resonators with noise coupled architecture to effectively increase the order of the NTF by two was reported in [27].

Second, BPΣΔ modulators can also be implemented in single-loop or cascade of the fundamental blocks with transfer function $1/(1 \pm z^{-1})$ or/and $z^{-1}/(1 \pm z^{-1})$, including feedback, feedforward and hybrid topologies. There are three generic DT topologies of a ΣΔ modulator with such structure: (a) Cascade of Resonators with distributed Feedback (CRFB) [28]; (b) Cascade of Resonators with distributed Feedforward (CRFF) [29], [30]; and (c) low-spread CRFF (LSCRFF) [31]. All three of them require that the input feedforward coefficients match the feedback coefficients for a flat STF, which imposes difficulties in the control of the NTF when tuning the desired f_c by these coefficients, although an automatic coefficient design methodology for such high-order BPΣΔ modulators has already been proposed [32].

The approach of changing loop coefficients, however, requires the use of a loop filter with order $2L\text{-}th$ to achieve Lth-order noise shaping, thus introducing the stability issue. In addition, a single biquad resonator requires two-amps, resulting in poor power-efficiency.

B. Changing the Sampling Frequency

To overcome the limits from the approach of changing loop coefficients, another approach changing the sampling frequency is used. A BPΣΔ modulator tuned at $f_s/4$ can be designed from its LP counterpart by the standard transformation $z^{-1} \rightarrow -z^{-2}$, then changing the sampling frequency is equivalent to change the f_c. The scheme can be implemented by an interleaved two-path architecture [33].

Another solution is using the transformation $z^{-1} \rightarrow z^{-N}$ to change an Lth-order LP modulator into interleaved N-path structures, each path operated with a clock frequency f_s/N, to realize the $(N \cdot L)th$-order BPΣΔ modulators [23]. This solution leads to $f_c = f_s/N$ without introducing stability issues, but suffers from tones mirrored in the signal band caused by the offset, gain and timing mismatches among paths [34].

For the approach of changing the sampling frequency another disadvantage results from the fact that it is not practical for a wide tuning range. A wide tuning range means the switched capacitor circuits have to adapt to a wider sampling frequency.

LPΣΔ prototypes and transformation approaches aside, another way to design the BPΣΔ modulator is directly starting from the synthesis of NTF [35]–[38]. The use of a novel NTF synthesis technique, based on across-coupled two-path architecture, can obtain a mirror image free f_c, which is far away from $f_s/2$. The NTF synthesized in [36] is $(1 + \alpha z^{-1} + z^{-2})^2$, where α is the cross-coupled coefficient. They set α to 1, and

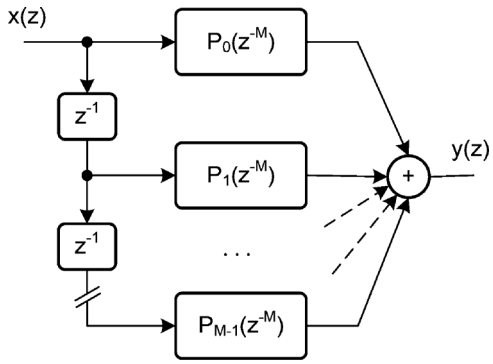

Fig. 3. Architecture of the polyphase filter.

a band-pass response centered around $f_s/3$ is implemented. As mentioned, changing the sampling frequency to tune the center frequency has a limitation, however, for this type of architecture, the tunability can also be obtained by adjusting α. Since the STF is just a delay in the NTF synthesis technique, which is free of α, it is easy to tune f_c by a capacitor ratio.

On the other hand [36] is just a specific case. This paper will propose a systematic approach using the polyphase decomposition of the NTF to design this kind of tunable BP$\Sigma\Delta$ modulator with cross-coupled M-path architecture.

III. Polyphase Decomposition of the NTF

The polyphase decomposition is a technique used in signal processing for operating a digital filter at a lower frequency when compared with conventional architectures. For a given decimation factor M the response of a pth-order FIR filter

$$P(z) = \sum_{k=0}^{p} a(k) z^{-k} = a_0 + a_1 z^{-1} + a_2 z^2 + \cdots + a_p z^{-p} \quad (4)$$

is decomposed into

$$\begin{aligned} P(z) &= P_0(z^{-M}) + z^{-1} P_1(z^{-M}) + \cdots + z^{-(M-1)} P_{M-1}(z^{-M}) \\ &= \sum_{i=0}^{M-1} z^{-i} P_i(z^{-M}) \end{aligned} \quad (5)$$

where

$$P_i(z^{-M}) = \sum_{j=0}^{k} a_{Mj+i} z^{-Mj} \quad (6)$$

the number of terms of the addition k is a integer, which is not more than p/M to hold $0 \le Mk+i \le p$. Fig. 3 shows a possible architecture of the filter.

The polyphase decomposition can be used for determining the requested NTF of a $\Sigma\Delta$ converter. This would require an interleaved connection of modulators like the one of Fig. 3. However, the signal to be filtered, the quantization noise, is generated inside the modulator. The output equals the input passed through the STF added to the quantization noise, that's supposed to be white spectrum, passed through the NTF. A polyphase z^{-M} decomposition applied to $\Sigma\Delta$ modulators leads to M quantizers; therefore, it is necessary to perform the polyphase decomposition of the NTF with M quantization noise sources.

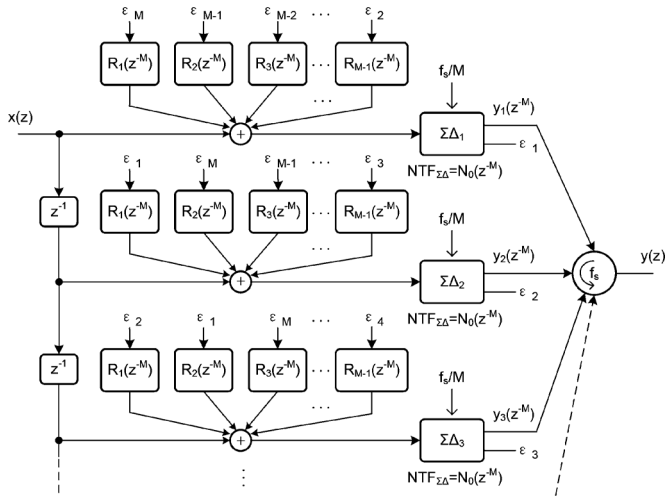

Fig. 4. Polyphase sigma-delta modulator.

Supposing that the pth-order NTF of a given $\Sigma\Delta$ modulator is

$$NTF_{\Sigma\Delta}(z) = 1 + \alpha_1 z^{-1} + \alpha_2 z^{-2} + \cdots + \alpha_p z^{-p} \quad (7)$$

its decomposition into the polyphase terms is

$$\begin{aligned} NTF_{\Sigma\Delta}(z) = N_0(z^{-M}) + z^{-1} N_1(z^{-M}) + \cdots \\ + z^{-(M-1)} N_{M-1}(z^{-M}) \end{aligned} \quad (8)$$

where

$$\begin{aligned} N_0(z^{-M}) &= 1 + \alpha_M z^{-M} + \alpha_{2M} z^{-2M} + \cdots \\ N_1(z^{-M}) &= \alpha_1 + \alpha_{M+1} z^{-M} + \alpha_{2M+1} z^{-2M} + \cdots \\ &\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\ N_{M-1}(z^{-M}) &= \alpha_{M-1} + \alpha_{2M-1} z^{-M} + \alpha_{3M-1} z^{-2M} + \cdots \end{aligned} \quad (9)$$

Let us define the following intermediate functions

$$\begin{aligned} R_1(z^{-M}) &= \frac{z^{-1} N_1(z^{-M})}{STF} \\ R_2(z^{-M}) &= \frac{z^{-2} N_2(z^{-M})}{STF} \\ &\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\ R_{M-1}(z^{-M}) &= \frac{z^{-(M-1)} N_{M-1}(z^{-M})}{STF} \end{aligned} \quad (10)$$

where the suffix indicates both the polynomial function and the number of delays added by the block to the function $N_i(z^{-M})/STF$.

Notice that the STF is a delay. It ranges from z^{-1} to z^{-M}, depending on how the deal of M clock periods available is distributed along the z^{-M} $\Sigma\Delta$ loop.

Using the functions of (10) we obtain the polyphase version of the $\Sigma\Delta$ modulators shown in Fig. 4.

Each modulator generates the digital output and at the analog output the quantization errors, $\epsilon_1, \epsilon_2, \ldots$, and ϵ_M. For example, ϵ_1, multiplied by $NTF_{\Sigma\Delta}(z^{-M})$ is part of the digital output $y_1(z^{-M})$. In the second path ϵ_1 multiplied by $R_1(z^{-M})$ passes through the STF of the modulator and appears as part of the output $y_2(z^{-M})$, and so forth. Therefore, ϵ_1, as well as all the other quantization noise generators, are processed as it is done in the conventional polyphase scheme of Fig. 3.

The simplest case is when all the $R_i(z^{-M})$ are equal to 0 and this is, actually, a plain time-interleaving of $\Sigma\Delta$ architectures.

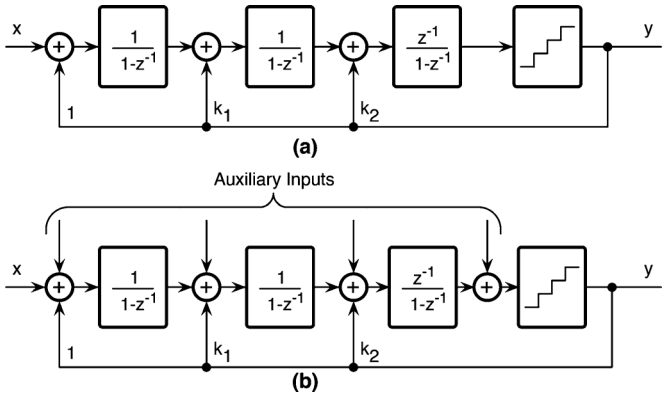

Fig. 5. (a) Third-order ΣΔ modulator. (b) Main and auxiliary inputs.

For example, the $NTF = (1 + z^{-2})$ that originates a band-pass response around half of the Nyquist frequency $f_N/2$ can be decomposed into two polynomials $N_0 = (1+z^{-2})$ and $N_1 = 0$. The implementation is the time interleaving of two ΣΔ realizing the basic $NTF_{\Sigma\Delta} = (1 + z^{-1})$.

Since high order ΣΔ architectures are realized with the cascade of integrators, they allow multiple inputs for the quantization noise injection. For example, the third-order scheme of Fig. 5(a), stable for three or more bit quantization, has three injection points. In addition, it is possible to inject the delayed quantization noise before the quantizer, as Fig. 5(b) illustrates. Since the transfer function from auxiliary inputs other than the signal input and output are not the STF, the transfer function related to the used input must replace STF in (10).

IV. Realization of Polyphase ΣΔ

For a polyphase realization it is convenient to have an NTF that suitably matches $N_0(z^{-M})$. The use of blocks with transfer function $1/(1 \pm z^{-1})$ and feedback leads to a useful set of transfer function to match the required $N_0(z^{-M})$. Fig. 6 shows several possible options.

The schematic of Fig. 6(a) corresponds to a conventional first-order ΣΔ modulator. The one of Fig. 6(b) uses a block whose transfer function is $1/(1 + z^{-1})$ with positive DAC feedback. By inspection

$$(x + y)\frac{z^{-1}}{1 + z^{-1}} + \epsilon = y \tag{11}$$

which leads to the expected NTF of $(1 + z^{-1})$. Similar derivations determine the NTF of other schemes in Fig. 6.

The functions of Fig. 6 are realized with conventional circuits. They are SC integrators for the $z^{-a}/(1 - z^{-1})$ transfer function $(a = 0, 1)$ and similar integrators with two square wave modulators one in front and the other at the output for generating the $z^{-a}/(1 + z^{-1})$ transfer function [36].

The circuit implementation of the first term of $z^{-1}N_1(z^{-M})$, $\alpha_1 z^{-1}$, can be problematic because of the time required by the quantizer. Since the total delay available is one clock period, it would be necessary to have a signal transfer function of each path equal to z^{-1} and to share part of this delay with the quantizer.

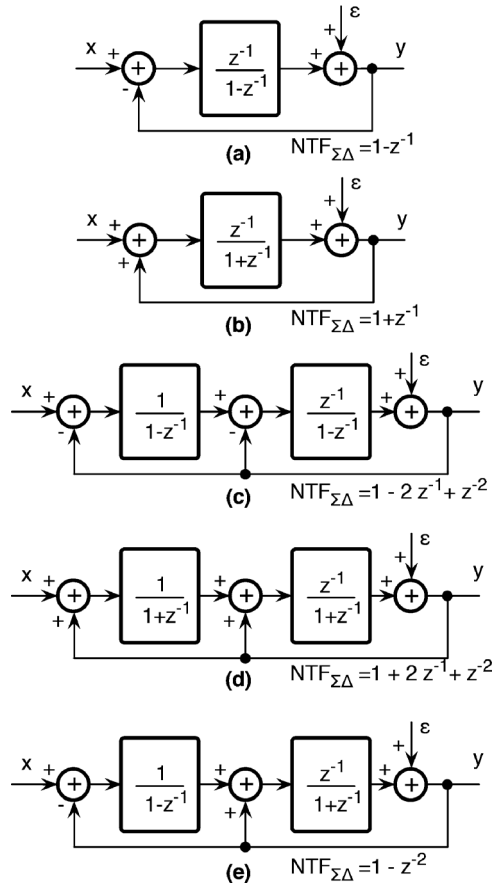

Fig. 6. Different alternatives of polyphase sigma-delta building blocks.

In Fig. 7 let us consider the z^{-M} polyphase path. The available M clock period delay is divided into p, $M - p$ between the forward and the feedback path. The result is $\text{STF} = z^{-p}$ and $\text{NTF} = 1 + z^{-M}$. In order to realize the $\alpha_1 z^{-1}$ term of the $\text{NTF}_{\Sigma\Delta}(z)$ it can be convenient to add $\alpha_1 z^{-1}\epsilon_i$ just before the quantizer of the next path. Since it results at the output multiplied by the NTF it is necessary to compensate for the additional $\alpha_1 z^{-M-1}\epsilon_i$ term. This would be possible realized by the paths in the grey blocks of Fig. 7. Since the $\alpha_1 z^{-1}$ term is already implemented, the rest of $N_1(z^{-M})$ becomes

$$N_1'(z^{-M}) = \alpha_{M+1} z^{-M} + \alpha_{2M+1} z^{-2M} + \cdots \tag{12}$$

that foresees suitable delays for an easy implementation.

The number of paths of the polyphase architecture depends on the specific NTF and a trade-off between benefits and costs. For example, the NTF

$$\text{NTF}_{\Sigma\Delta} = 1 - 3z^{-1} + 3z^{-2} - z^{-3} \tag{13}$$

can be realized with three paths whose NTF generates the $(1 - z^{-3})$ term and two cross coupled connections for the remaining terms.

The z^{-3} polyphase decomposition of (13) leads to

$$\begin{aligned} N_0(z^{-3}) &= 1 - z^{-3} \\ N_1(z^{-3}) &= -3 \\ N_2(z^{-3}) &= 3 \end{aligned} \tag{14}$$

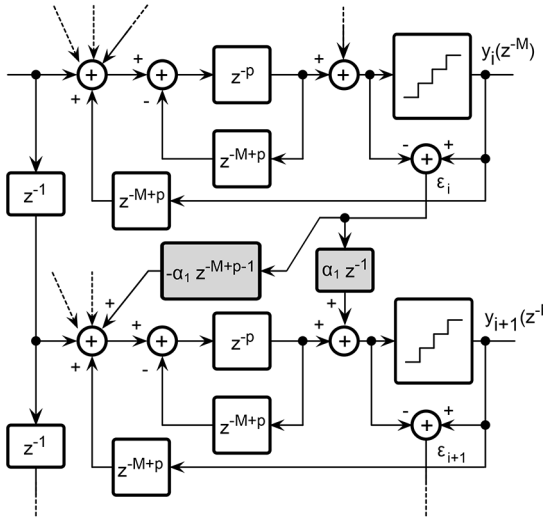

Fig. 7. Additional paths (in grey) to implement the first term of $z^{-1}N_1(z^{-M})$.

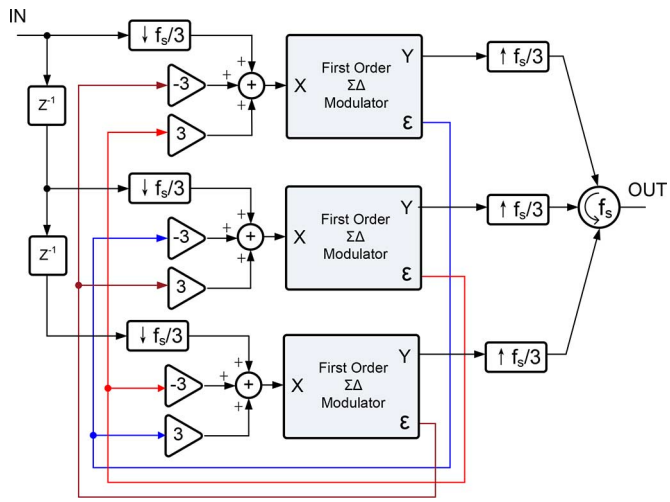

Fig. 8. A 3-path polyphase sigma-delta ADC.

One possible three-path polyphase implementation of the third-order NTF of (13) is shown in Fig. 8 [39].

Higher order NTF like, for example

$$\mathrm{NTF}_{\Sigma\Delta} = 1 - 4z^{-1} + 5z^{-2} - 5z^{-4} + 4z^{-5} - z^{-6} \quad (15)$$

that leads to five zeros at $z = 1$ and one at $z = -1$ can be realized by three paths giving $\mathrm{NTF} = (1 + z^{-3})(1 - z^{-3})$ and cross coupled branches that realize other terms.

For high order NTFs the sensitivity to coefficients is high and the method can become suitable for digital sigma-delta implementations.

V. Second- and Fourth-Order Polyphase ΣΔ

The NTF of a second-order BPΣΔ modulator with zeros at $z = e^{\pm j\alpha}$ is

$$\mathrm{NTF}_{\Sigma\Delta} = 1 + \beta z^{-1} + z^{-2} \quad (16)$$

where $\beta = -2\cos(\alpha)$. It is a single parameter for tuning the band-pass frequency. Changing it from -2 to $+2$ moves the poles on the unity circle form $z = 1$ to $z = -1$. $\beta = -2$ corresponds to the low pass response. Since the STF is the one of the generating ΣΔ architecture, if it is just a delay, the tuning of the noise shaping does not affect the signal and its amplitude at the output remains unchanged.

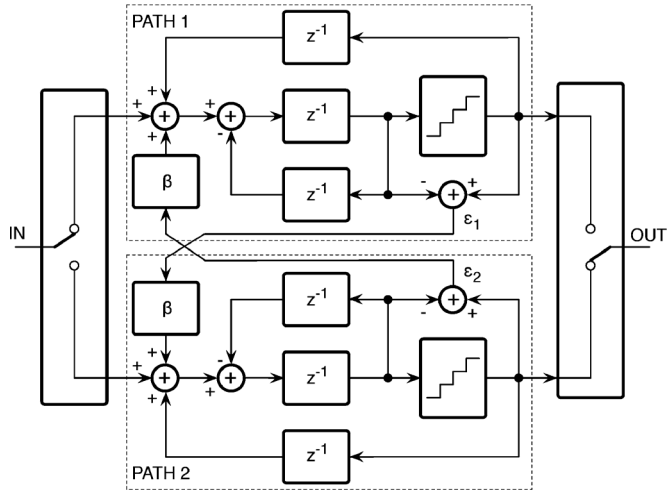

Fig. 9. Second-order band-pass polyphase sigma-delta ADC.

The z^{-2} polyphase decomposition of (16) leads to

$$N_0(z^{-2}) = 1 + z^{-2}$$
$$N_1(z^{-2}) = \beta. \quad (17)$$

Fig. 9 shows the equivalent block diagram, already implemented and experimentally verified in [35] with $\beta = 1$. Each branch of Fig. 9 is a first-order block with transfer function $z^{-1}/(1 + z^{-2})$. The feedback of the quantized signal ϵ_i obtains for each path the following signal and noise transfer functions:

$$\mathrm{STF} = z^{-1} \quad \text{and} \quad \mathrm{NTF} = 1 + z^{-2}. \quad (18)$$

The NTF is the required $N_0(z^{-2})$; the cross coupled injection realizes the second term of the polyphase decomposition, $N_1(z^{-2})$.

Behavioral simulations conform the band-pass response. Moreover simulations estimate the effect of the limitations caused by non-idealities. Fig. 10 shows the output spectrum for $\beta = 0.8$ that sets the band-pass frequency at $0.315\,f_s$. The resolution of the quantizer is 4 bits. A gain mismatch between the channels gives rise to a tone at the mirrored frequency $f_N - f_{\mathrm{in}}$, because the gain mismatch corresponds to a square wave modulation of the input at the frequency $f_N/2$. The spur tone is outside the band of interest, provided that $|\beta|$ is large enough to move the band-pass frequency sufficiently far away from $f_N/2$. An offset mismatch only causes a tone at f_s/M, where M is the number of paths used. For two-path architecture, it is $f_s/2$, so the offset mismatch is an irrelevant limit in the case of Fig. 10.

The NTF of a fourth-order band-pass ΣΔ modulator with double zeros at $z = e^{\pm j\alpha}$ is

$$\mathrm{NTF}_{\Sigma\Delta} = 1 + 2\beta z^{-1} + (2 + \beta^2)z^{-2} + 2\beta z^{-3} + z^{-4} \quad (19)$$

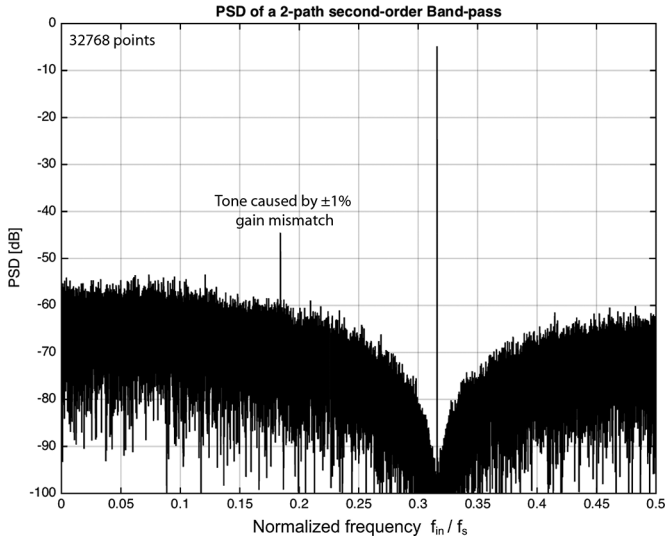

Fig. 10. FFT spectrum of the modulator in Fig. 9.

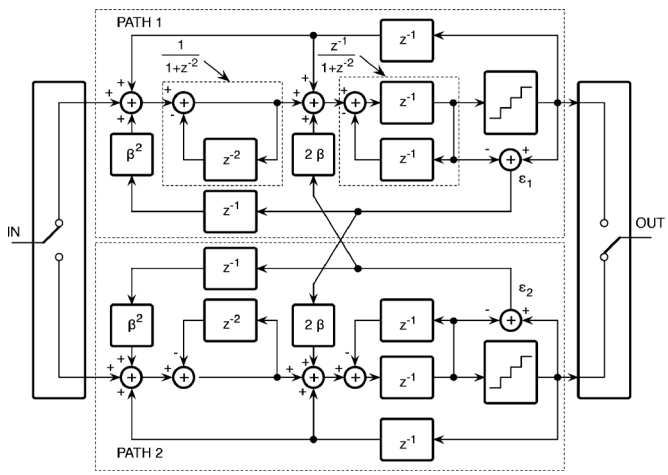

Fig. 11. Fourth-order band-pass polyphase sigma-delta ADC.

with z^{-2} polyphase decomposition expressed as

$$N_0(z^{-2}) = 1 + (2+\beta^2)z^{-2} + z^{-4}$$
$$N_1(z^{-2}) = 2\beta(1+z^{-2}). \tag{20}$$

A possible generating block diagram is shown in Fig. 11 [36]. It uses a two-path polyphase decomposition. Each path is the cascade of two blocks with transfer functions

$$H_1(z) = \frac{1}{1+z^{-2}}$$
$$H_2(z) = \frac{z^{-1}}{1+z^{-2}} \tag{21}$$

The signal and noise transfer function of the path are

$$\text{STF} = z^{-1}$$
$$\text{NTF} = 1 + 2z^{-2} + z^{-4}. \tag{22}$$

Moreover, the transfer function from the auxiliary input of the second block to the output is

$$H_{\text{aux}} = z^{-1}(1+z^{-2}). \tag{23}$$

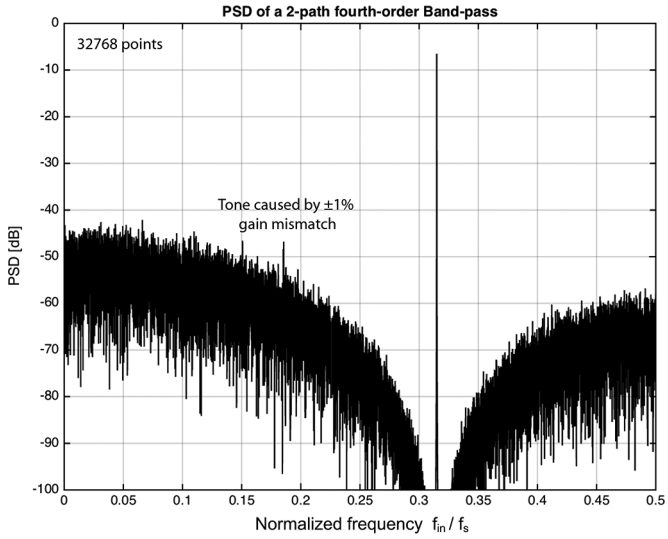

Fig. 12. FFT spectrum of the modulator in Fig. 11.

Comparing (20) and (22) it results that $\beta^2 z^{-2}$ is missing from the NTF. Moreover, H_{aux} has a convenient expression for achieving $N_1(z^{-2})$. These two observations lead to the two injections, and one cross coupled branch, of Fig. 11.

The output spectrum of Fig. 12 for $\beta = 0.8$ and 4-bit quantization verifies the fourth-order noise shaping. Even for this architecture a gain mismatch between the two paths generates a mirrored spur tone. The simulation of Fig. 12 uses a gain error of 0.02; the offset mismatch is an irrelevant limit as it leads to spur tones at zero frequency and Nyquist frequency.

Another possible polyphase decomposition uses four paths, in this case

$$N_0(z^{-4}) = 1 + z^{-4}$$
$$N_1(z^{-4}) = 2\beta$$
$$N_2(z^{-4}) = 2 + \beta^2$$
$$N_3(z^{-4}) = 2\beta \tag{24}$$

whose equivalent block diagram can be derived with the methods discussed above.

The tuning capability of the band-pass response depends on the value of the parameters β and its square value β^2. In the circuit implementation suitable capacitors realize these two coefficients. The effect of a mismatch between them moves the zeros of the $\text{NTF}_{\Sigma\Delta}$. This limit will be studied shortly.

VI. High Order Polyphase ΣΔ

The method discussed for second and fourth-order band-pass responses can be further extended to higher orders. For example, the use of the third-order scheme of Fig. 5 and a two-path polyphase decomposition leads to a sixth-order band-pass response. The NTF of the sixth-order BPΣΔ modulator with zeros at $z = e^{\pm j\alpha}$ is

$$\text{NTF}_{\Sigma\Delta} = 1 + 3\beta z^{-1} + 3(1+\beta^2)z^{-2} + \beta(6+\beta^2)z^{-3} + 3(1+\beta^2)z^{-4} + 3\beta z^{-5} + z^{-6} \tag{25}$$

with $\beta = -2\cos(\alpha)$.

The $\mathrm{NTF}_{\Sigma\Delta}$ can be decomposed into two or four polyphase terms for a suitable implementation using the methods discussed above.

The issue, in common with any high-order band-pass schemes that realize the resonant frequency based on the value of the passive element, is the accuracy of the coefficients. A small change of them moves the zeros out of the unity circle. Fig. 13 shows the position of zeros and the corresponding frequency responses for a variation of 0.1% of the coefficient of z^{-4}. The required accuracy makes it impossible to foresee tuning because it is necessary to trim the value of used elements.

VII. Polyphase MASH ΣΔ

Multi-stage noise shaping (MASH) structures use the cascade of ΣΔs to avoid problems related to stability. The outputs of a cascaded modulator are combined to produce a digital signal with high order noise shaping. The same method can be used for polyphase band-pass architecture.

The quantization noise at each output of a polyphase ΣΔ is at the decimated frequency. At the input of the cascaded modulator there are M noise generators with one sample every M clock periods. As a result, the polyphase processing of all inputs can be done in parallel. Supposing that the first modulator has used a z^{-2} decomposition and that the cascaded modulator must implement a $1+\beta z^{-1}+z^{-2}$ noise shaping, Fig. 14 shows the MASH architecture. The first modulator gives rise at the even and odd output digital signals and the quantization errors. The even and odd digital signals are

$$\begin{aligned} y_{1e} &= x_e STF_1 + \epsilon_{1e}N_0(z^{-2}) + z^{-1}\epsilon_{1o}N_1(z^{-2}) \\ y_{1o} &= x_o STF_1 + \epsilon_{1o}N_0(z^{-2}) + z^{-1}\epsilon_{1e}N_1(z^{-2}) \end{aligned} \quad (26)$$

where part of the noise shaping of the even quantization noise, ϵ_{1e}, exits from the even output, while the remaining part exits from the odd outputs and vice-versa for the odd quantization noise, ϵ_{1o}.

The outputs of the second modulator are

$$\begin{aligned} y_{2e} &= \epsilon_{1e} STF_2 + \epsilon_{2e}(1+z^{-2}) + \epsilon_{2o}\beta z^{-1} \\ y_{2o} &= \epsilon_{1o} STF_2 + \epsilon_{2o}(1+z^{-2}) + \epsilon_{2e}\beta z^{-1}. \end{aligned} \quad (27)$$

The digital processing block generates the two outputs $y_1(z)$ and $y_2(z)$ by time interleaving the even and odd data streams

$$\begin{aligned} y_1(z) &= y_{1e}(z^{-2}) + z^{-1}y_{1o}(z^{-2}) \\ y_2(z) &= y_{2e}(z^{-2}) + z^{-1}y_{2o}(z^{-2}) \end{aligned} \quad (28)$$

moreover,

$$\begin{aligned} \epsilon_1(z) &= \epsilon_{1e}(z^{-2}) + z^{-1}\epsilon_{1o}(z^{-2}) \\ \epsilon_2(z) &= \epsilon_{2e}(z^{-2}) + z^{-1}\epsilon_{2o}(z^{-2}). \end{aligned} \quad (29)$$

The power of $\epsilon_1(z)$ and $\epsilon_2(z)$ are $\Delta_1^2/12$ and $\Delta_2^2/12$ (Δ_1 and Δ_2 are the quantization steps of the quantizer in the first and second modulator, respectively), spreading over the f_s frequency interval. This, because the noise power of the each time interleaved term contributes with half of its $\Delta^2/12$ power to the total.

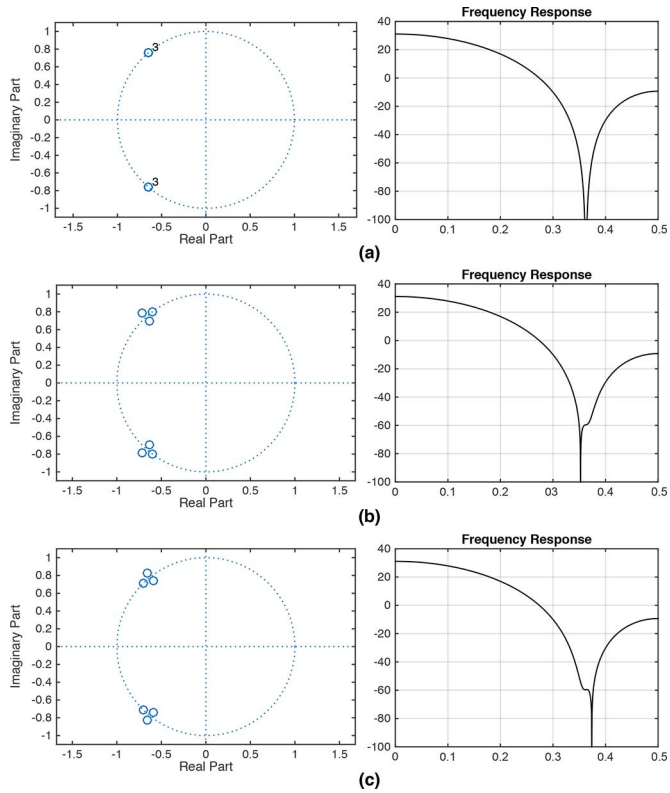

Fig. 13. Pole-zero plots and NTFs for polyphase band-pass ΣΔ (a) with no mismatch; (b) with 0.1% mismatch; (c) with −0.1% mismatch of the coefficient of z^{-4}.

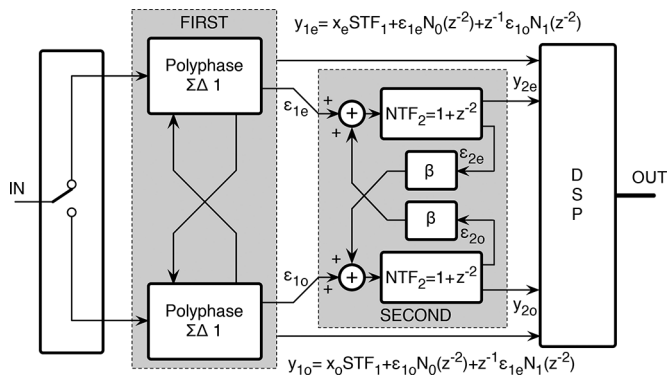

Fig. 14. MASH band-pass polyphase architecture.

Since input and outputs are

$$\begin{aligned} x(z) &= x_e(z^{-2}) + z^{-1}\, x_o(z^{-2}) \\ y_1(z) &= y_{1e}(z^{-2}) + z^{-1}\, y_{1o}(z^{-2}) \\ y_2(z) &= y_{2e}(z^{-2}) + z^{-1}\, y_{2o}(z^{-2}) \end{aligned} \quad (30)$$

combining the above equations, it results in

$$\begin{aligned} y_1(z) &= x(z)STF_1 + \epsilon_1(z)NTF_1 \\ y_2(z) &= \epsilon_1(z)STF_2 + \epsilon_2(z)NTF_2 \end{aligned} \quad (31)$$

where, according to the definition of $N_0(z^{-2})$ and $N_1(z^{-2})$, $NTF_1 = N_0(z^{-2}) + z^{-1}N_1(z^{-2})$ and, for this specific considered case, $NTF_1 = 1+\beta z^{-1}+z^{-2}$.

The following MASH processing

$$y_{\text{out}}(z) = y_2(z)NTF_1 - y_1(z)STF_2 \tag{32}$$

results in

$$y_{\text{out}}(z) = x(z)STF_1\, STF_2 + \epsilon_2(z)NTF_1\, NTF_2 \tag{33}$$

leading to higher order band-pass noise shaping, as expected.

An implementation of the polyphase MASH is proposed in [35]. It is a $2+2+2$ MASH architecture, moreover, each stage is a two-path second-order polyphase $\Sigma\Delta$ modulator, which generates transmission zeros at 1/3 of the clock frequency, thereby achieving a mirror image free band-pass response.

VIII. Band-Pass Tunability

Tuning a circuit requires changing its electrical parameters. The operation is feasible when changing one or two parameters with simple and easy to implement relationships. Since digital sections often control tuning, the step of changes is quantized and this must be small enough within the pass-band interval.

The centre frequency of the scheme of Fig. 9 depends on the value of β, a single parameter set by two capacitors that realize cross coupled paths. The mismatch between nominally equal capacitors caused by technology inaccuracy introduces tones out of the band of interest as verified by the simulations that lead to the spectrum of Fig. 10. As a result, the second-order architecture is easily tunable.

The centre frequency of a fourth-order scheme depends on two parameters, 2β and $2\beta^2$. Unfortunately, their relationship is not simple and tuning can require a look-up table that digitally controls pair of capacitors. Since the values of capacitors change in a discrete manner with the quantization interval Δ_u, also the tuning parameters change in a discrete manner

$$2\beta(i) = \gamma H(i)\Delta_u, \quad \beta^2(i) = \gamma K(i)\Delta_u \tag{34}$$

where $H(i)$ and $K(i)$ are integer numbers. If the capacitor C_u that makes $\beta = 1$ is made by r^2 quantized parts, because of the constraint of the second relationship in (34), the discrete values of β are only r. The used technology determines the minimum value. If C_u is 0.5 pF and $\Delta_u = 5$ fF the number of selectable frequencies over the entire range is only 20.

Using for the capacitor realizing β^2 an approximated value, $k\Delta_u$ (with k rounded integer), splits the zeros. If the rounded value is less than the nominal, the zeros still stay on the unity circle; if higher, the zeros move in orthogonal directions. Consider, for example, $\beta = 0.88$, realized with 88 elements of an array of 100 C_u. It originates a notch at $0.322\, f_s$, but the value of $\beta^2 = 0.7744$ must be rounded. If it goes to 0.77 the position of zeros and spectrum look like what is shown in Fig. 15(a). The response pops up between the split zeros and the expected SNR becomes worse. With a $\pm 0.5\%\, f_s$ bandwidth the SNR drops from 87.6 dB to 79.8 dB. For lower bandwidth the loss is worse. If the value of $\beta^2 = 0.7744$ is rounded to 0.78 the position of zeros and spectrum become the ones shown in Fig. 15(b).

The method grants a full tunability over the entire Nyquist range. However, the mismatch and stability requirements can limit the region of operation of architectures. Mismatches and offsets generate tones and it is not recommended to use signal intervals for which tones are not far away enough from the band of interest. For example, a gain mismatch between the channels gives rise to a tone at the mirrored frequency $f_s/2 - f_{\text{in}}$. From $f_s/2 - f_{\text{in}} = f_{\text{in}}$, we get that the modulator cannot be used for a center frequency at $f_s/4$, so the tuning range of the modulator is from DC to 0.5 f_s without the range let's say 0.225 f_s to 0.275 f_s (depending on the considered bandwidth).

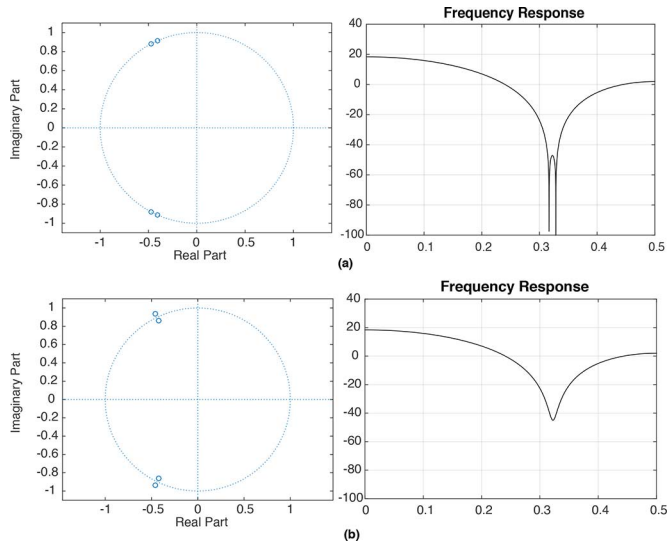

Fig. 15. Position of zeros and frequency response with rounded β^2 coefficient. (a) Lower than nominal. (b) Higher than nominal.

However, if such small limitation can be tolerated (depending on application bandwidth requirement), then the polyphase sigma-delta architecture can significantly improve the sampling frequency (and thus OSR-bandwidth tradeoff) over the single-channel technology limit, while completely insensitivity to the very headache interleave-mismatch problems that is always happening in the Nyquist TI converters. This is an important advantage and indeed a very worthy trade-off.

IX. Tunable Polyphase Band-Pass MASH

The main limit to the tunability of band-pass $\Sigma\Delta$ converters derives from the use of multiple tuning elements and their matching. The NTF of $\Sigma\Delta$ architectures implemented by a cascade of resonators with transfer functions $H_i(z) = P_i(z)/Q_i(z)$ is the product of the $Q_i(z)$s. The zeros of the NTF are the superposition of complex zeros generated by the resonators. The accuracy and the resolution depend on the precision of the resonant frequencies. A shift in the same direction shifts the NTF resonant value. Random variations of the resonant frequencies enlarge the pass-band region and diminishes the noise shaping. If, for example, two zeros at $0.325 f_s$ define the resonant frequency and this is set with a capacitor of 0.25 pF, an error of ± 2.5 fF splits the zeros by $0.2\%\, f_s$. With a clock of 4 GHz the split is 8 MHz.

The coefficients of a polyphase decomposition globally define the NTF; a possible error in one of them changes all the zeros of the NTF. For a fourth-order architecture and very small errors the zeros can remain on the unity circle: for higher order

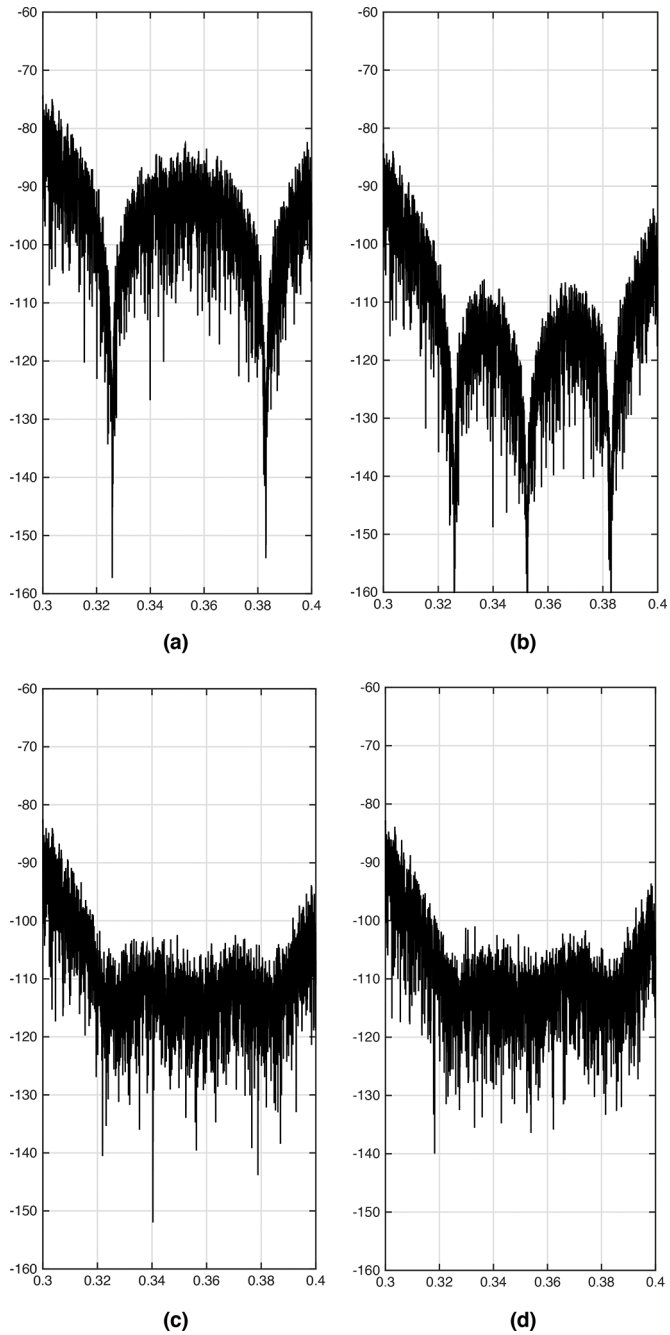

Fig. 16. (a) Noise spectrum of a fourth-order modulator with split zeros around the notch frequency. (b) Noise spectrum of a MASH sixth-order modulator. (c) and (d) Spectrum of the MASH with the β coefficient used in the digital processor changed by $\pm 1\%$.

the zeros definitely move away. Thus, ensuring a reliable tunability of polyphase $\Sigma\Delta$ requires extremely high accuracy of the components.

The use of band-pass polyphase MASH is the solution to the limit because being a cascade of blocks, the MASH separates the consequences of mismatch between elements in each modulator. In addition, the MASH architecture enables an interesting feature: the possibility of rough-fine trimming of the centre frequency.

A two stages MASH cancels the noise of the first modulator, ϵ_1, by passing its through a second modulator, shaping the output and subtracting the result from the processed second output in the digital domain. The cancellation relies on using a digital shaping that matches the NTF of the analog circuitry. If there is a difference, (33) should include an additional term (the STFs are supposed to be accurate) and becomes

$$y_{\text{out}} = x\, STF_1\, STF_2 + \epsilon_2 NTF_{1d}\, NTF_{2a} + \epsilon_1 (NTF_{1a} - NTF_{1d}) \tag{35}$$

where NTF_a refers to the analog noise transfer function of the modulator and NTF_d is the function used in the digital post-processing. If the first modulator is second order, with ideally an $NTF = 1 + \beta z^{-1} + z^{-2}$, the possible error is due to the mismatch between the βs and the additional term, limited by $\Delta\beta$, and it causes an unshaped leakage of ϵ_1 attenuated by the *OSR* ratio, f_{BP}/f_s.

For a very large *OSR* and reasonable accuracy in the analog β the leakage can be acceptable. Therefore, being the shaping of ϵ_2 given by $NTF_{1d}\, NTF_{2a}$, the result depends on the product of an analog NTF and a digital function. The analog NTF can provide a rough tuning by setting zeros on the unity circle around the desired centre frequency, the digital function can set precisely another zero at the centre frequency with a solid relationship with the clock frequency.

Behavioural simulations of a fourth-order *4-bit* $\Sigma\Delta$ with $\beta = 1.2$ and the coefficient of z^{-2} equal to $\beta^2 - 0.08$ leads to a spectral response with split zeros centred around $0.3525\, f_s$ and separated by $0.06\, f_s$ (Fig. 16(a)). The use of that modulator after a second-order scheme with the same β determines after digital processing the spectrum of Fig. 16(b). The zero of the second order at $0.3525\, f_s$ reduces the relative maxima at the two sides by about 25 dB. That corresponds to more or less $+4$-bit bonus in a relatively wide range. For small bandwidths the bonus is higher. Changing the value of β in the digital processing moves the centre zero but, as anticipated, a leakage of ϵ_1 augments the noise floor. A change of the digital β by $\pm 1\%$ moves the centre frequency by $\pm 0.001\, f_s$ but the increased noise floor almost fills the notch, as shown in Fig. 16(c) and (d), leaving just 1-bit of extra benefit with respect to the four bits of relative maxima. That is, for the considered design, the maximum range of fine tuning.

X. Conclusion

This paper proposes to synthesize the NTF of BP$\Sigma\Delta$ modulators using the polyphase decomposition technique. The important benefit, other than a reduction of operating frequency in the processing paths, is that spur tones caused by interleaved mismatch are far away from the signal band, thus ensuring a virtual interleaved-mismatch-free operation. The technique can be used for high order shaping and is suitable for MASH architectures. It is shown that at the cost of a limited noise leakage the NTF can be rough-fine tuned with the rough tuning established by the analog modulator and the fine tuning embedded in the signal processing required to enhance the shaping order. The use of a fine digital tuning with centre frequency linked to the sampling frequency permits a careful selection of the desired small bands.

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Dr. Maloberti was the recipient of the XII Pedriali Prize for his technical and scientific contributions to national industrial production, in 1992. He was co-recipient of the 1996 Institute of Electrical Engineers Fleming Premium, the best Paper award, ESSCIRC-2007, and the best paper award, IEEJ Analog Workshop-2007 and 2010. He was the President of the IEEE Sensor Council from 2002 to 2003 and Vice-President, Region 8, of the IEEE CAS Society from 1995 to 1997 and an Associate Editor of IEEE TCAS-II. He was serving as VP-Publications of the IEEE CAS Society 2007–2008. He was distinguished lecturer of the IEEE Solid State Circuits Society 2009–2010 and distinguished lecturer of the Circuits and Systems Society 2012–2013. He received the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, and the 2000 IEEE Millennium Medal. He received the IEEE CAS Society 2013 Mac Van Valkenburg Award. In 2009 he received the title of Honorary Professor of the University of Macau and he is currently the chairman of the Academic Committee of the Microelectronics Key-Lab of Macau. He is President elect of the IEEE Circuits and Systems Society.

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He is currently an Associate Professor in the Faculty of Science and Technology, University of Macau, and is the Coordinator of the Data Conversion and Signal Processing (DCSP) Research Line in State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. He has published one book entitled *Generalized Low-Voltage Circuit Techniques for Very High-Speed Time-Interleaved Analog-to-Digital Converters* (Springer), holds six U.S. and two Taiwan patents and over 80 technical journals and conference papers in the field of high performance data converters and analog mixed-signal integrated circuits.

Dr. Sin is/has been the member of Technical Program Committee of 2013–2015 IEEE Asian Solid-State Circuits Conference, 2015 International Wireless Symposium, Track Chair in TPC of IEEE TENCON 2015, IEEE Sensors 2011 and IEEE RFIT 2011–2014 Conference, Review Committee Member of PrimeAsia 2009 Conference, Technical Program and Organization Committee of the 2004 IEEJ AVLSI Workshop, as well as the Special Session Co-Chair and Technical Program Committee Member of 2008 IEEE APCCAS Conference. He is currently the Secretary of IEEE Solid-State Circuit Society (SSCS) Macau Chapter (with 2012 IEEE SSCS Outstanding Chapter Award) and IEEE Macau CAS/COM Joint Chapter (with 2009 IEEE CAS Chapter of the Year Award). He was the co-recipient of the 2011 ISSCC Silk Road Award, Student Design Contest Award in A-SSCC 2011 and the 2011 State Science and Technology Progress Award (second-class), China.

Rui P. Martins (M'88–SM'99–F'08) born in April 30, 1957, received the Bachelor (5-years), the Masters, and the Ph.D. degrees, as well as the *Habilitation* for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Tecnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering (DECE)/IST, TU of Lisbon, since October 1980. Since 1992, he has been on leave from IST, TU of Lisbon (now University of Lisbon since 2013), and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor since August 2013. In FST he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed (in 2013), as Vice-Rector (Research) until August 31, 2018. Within the scope of his teaching and research activities he has taught 21 bachelor and master courses and has supervised (or co-supervised) 38 theses, Ph.D. (17) and Masters (21). Co-authored: six books and four book chapters (refereed); 15 Patents, USA (13) and Taiwan (2); 312 papers, in scientific journals (78) and in conference proceedings (234); as well as other 60 academic works, in a total of 397 publications. He was a co-founder of Chipidea Microelectronics (Macao) (now Synopsys) in 2001/2002, and created in 2003 the *Analog and Mixed-Signal VLSI Research Laboratory* of UM, elevated in January 2011 to State Key Laboratory of China (the 1^{st} in Engineering in Macao), being its Founding Director.

Prof. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005, and of the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 *World Chapter of the Year* of the IEEE *Circuits And Systems Society (CASS)*]. He was the General Chair of 2008 IEEE Asia-Pacific Conference on CAS C *APCCAS2008*, and was the Vice-President for the Region 10 (Asia, Australia, the Pacific) of *IEEE CAS Society* (2009–2011). Since then, he was Vice-President (World) Regional Activities and Membership of IEEE CAS Society (2012–2013), and Associate Editor of IEEE TRANSACTIONS ON CAS II: Express Briefs (2010–2013), nominated *Best Associate Editor of T-CAS II* for 2012 to 2013. Plus, he was a member of the IEEE CASS Fellow Evaluation Committee (2013 and 2014), and the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—Director of the IEEE. He is now the General Chair of *Asia South Pacific Design Automation Conference C ASP-DAC2016*. He was also the recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.