Improving the Linearity and Power Efficiency of Active Switched-Capacitor Filters in a Compact Die Area

Yaohua Zhao, Pui-In Mak, Man-Kay Law, and Rui P. Martins

***Abstract*— The die size of multistandard wireless transceivers in ultrascaled CMOS is dominated by the baseband low-pass filters (LPFs), which typically count on passive-*RC* components to define the time constant. To break this area constraint, this paper revisits the active switched-capacitor (SC) LPF for its united benefits of clock-rate-defined bandwidth, accurate cutoff frequency, and small die size due to capacitor-ratio-based sizing and no spare elements. The key challenges of active-SC LPFs are the speed- and linearity-to-power tradeoffs, which are addressed by two circuit techniques: 1) switched-current assisting (SCA) and 2) precharging (PC). The SCA accelerates the charging speed of the integration capacitor, while the PC improves the linearity when charging the load capacitor. Three prototypes (first order, biquad, and fifth-order Butterworth) fabricated in a 65-nm CMOS process validate the feasibility of the proposed SCA and PC techniques.**

***Index Terms*— Bandwidth (BW), clock-rate defined, CMOS, die area, linearity, low-pass filter (LPF), switched capacitor (SC), tunability, gain-bandwidth product (GBW).**

I. Introduction

Multistandard wireless systems rely on high-linearity bandwidth (BW)-scalable low-pass filters (LPFs) to underpin a wide variety of channels and peak-to-average power ratios (e.g., 16-/64-quadratic-amplitude modulation orthogonal frequency-division multiplexing). Active-*RC* [1] and g_m-C [2] LPFs have been the common choices, but the BW scaling could mainly be achieved by tuning the supply voltage [3], bias current, and/or passive-*RC* banks [2]. The former two could lead to substantial variations of multiple metrics, while the latter could impact the chip size that is increasingly costly in ultrascaled CMOS.

The switched-capacitor (SC) LPF is revisited here as an alternative. No calibration loop or spare elements are entailed as the BW can be simply set or scaled by the clock rate. The main challenges of active-SC LPFs are the speed- and linearity-to-power tradeoffs due to the switching nature of discrete-time signal processing. Although the improved f_t and parasitics of fine linewidth CMOS could benefit the power efficiency of discrete-time circuits, the overall performance of an active-SC integrator is tightly coupled to the slew rate, gain–BW (GBW) product and linearity of its operational transconductance amplifier (OTA) [4]. Thus, gain regulation was proposed in [5] to relieve the stringent requirement of the OTA.

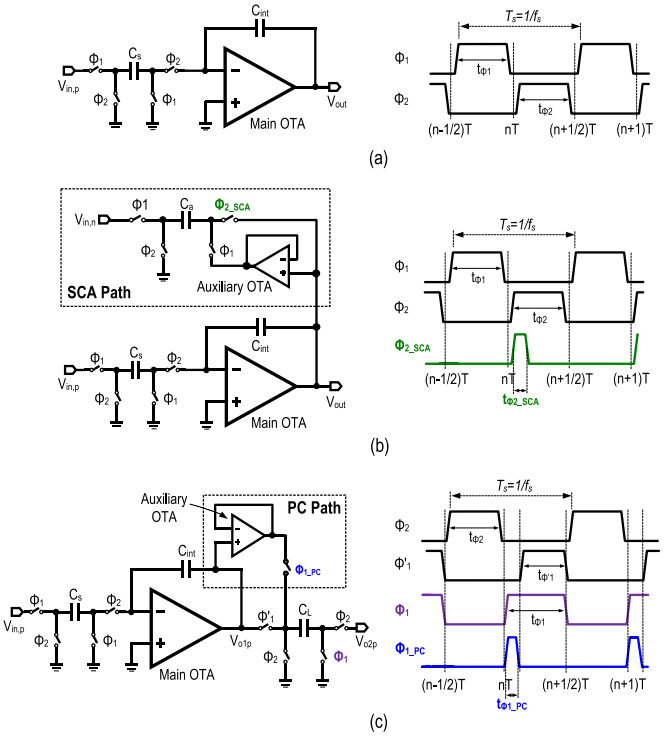

Fig. 1. (a) Typical SC integrator proposed. (b) SCA SC integrator. (c) PC-assisted SC integrator.

This paper proposes novel circuit techniques to improve the active-SC LPF via assisting it with a passive-SC network. Methods for the same goal were studied in [6] and [7], but the former calls for an active pseudoexponential pulse generator that is sensitive to process, voltage and temperature variations. For the latter, it involves complex circuitry and clock phases for effective compensation, while its simple precharging (PC) method also penalizes the accuracy.

Section II introduces two techniques for SC LPFs: 1) switched-current assisting (SCA) and 2) PC. An SCA SC integrator that corresponds to a first-order SC LPF is detailed. The speed and linearity improvements of the proposed techniques in an SC biquad are presented in Section III. The experimental results of three LPF prototypes are given in Section IV, and the conclusion is drawn in Section V.

II. Basic Principles of the SCA and PC Techniques

For a typical SC integrator [Fig. 1(a)], the input signal ($V_{\text{in},p}$) is sampled by C_S during Φ_1, while the main OTA drives the charge stored on C_S to the integration capacitor C_{int} during Φ_2. The finite GBW, slew rate, and intrinsic distortion of the OTA can result in imperfect charge transfer in every sampling period $T_S(= 1/f_s$, the sampling frequency), degrading the accuracy and linearity of the integration [4]. To alleviate the GBW (power)-to-performance

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Y. Zhao, P.-I. Mak, and M.-K. Law are with the State Key Laboratory of Analog and Mixed-Signal VLSI, Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau 563003, China (e-mail: yb07437@umac.mo; pimak@umac.mo; mklaw@umac.mo).

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI, Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau 563003, China, and also with the Instituto Superior Técnico, Universidade de Lisboa, Lisbon 1649-004, Portugal (e-mail: rmartins@umac.mo).

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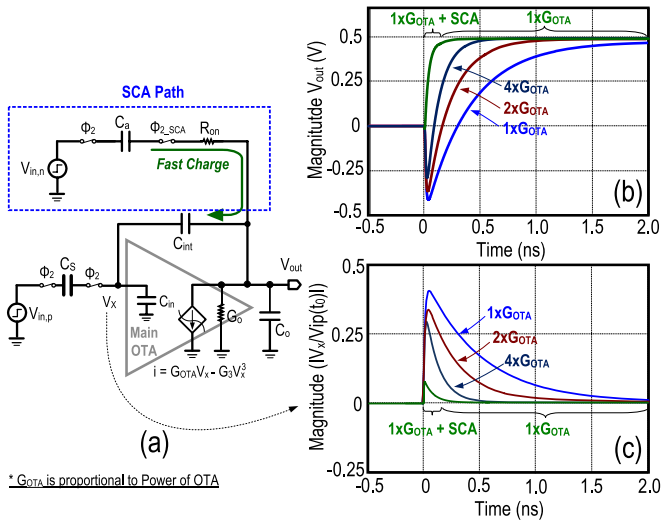


Fig. 2. (a) Small-signal equivalent circuit of the SCA SC integrator with the main OTA modeled by a weakly nonlinear model in the integration phase. (b) Transient waveforms of $|V_x/V_{\text{in},p}(t_0)|$ under different G_{OTA} and after adding the SCA path. (c) Transient outputs under different G_{OTA} and after adding the SCA path.

tradeoff, two circuit techniques are proposed [Fig. 1(b) and (c)] and their operating principles are described as follows: when the noninverting input ($V_{\text{in},p}$) is sampled by C_S during Φ_1, an SCA path [Fig. 1(b)] that includes the assisting capacitor C_a is added to sample the inverting input ($V_{\text{in},n}$), which is available in the differential mode. To store the desired charge on C_a and transfer it to C_{int}, an auxiliary OTA configured with unity-gain feedback is added. V_{out} can be copied to the assisting capacitor C_a such that only the desired charge is delivered to C_{int} during the assisting phase Φ_{2_SCA}. Upon completion, the SCA path is disconnected from V_{out} to remove its loading effect. As the SCA path already delivers most charge, the relaxed main OTA handles only the error correction during the rest of Φ_2, which is not speed demanding anymore (slew rate and GBW).

The SCA path is dedicated to assist in charging C_{int}, but any load capacitor (C_L) at the output will also load the main OTA. In general, an SC integrator will be interfaced by another SC branch to continue the signal processing. Thus, a second technique is proposed to deal with C_L that is the PC path, as shown in Fig. 1(c). Before Φ_1' that entails the main OTA to charge C_L, Φ_{1_PC} allows the power-efficient auxiliary OTA to precharge C_L first. There are two exponential settling processes when charging C_L: Φ_{1_PC} by the auxiliary OTA and Φ_1' by the main OTA. As the auxiliary OTA is already available, the PC path can share it with only one extra route from its output to C_L. Thus, the SCA and PC techniques are combinable in one SC integrator by sharing one auxiliary OTA, improving the charging efficiency of C_{int} and the linearity when driving C_L. In the analysis below, the focus is on the SCA path as it contributes more to the linearity and a similar procedure can be applied to the PC path.

A. Linearity Improvement of the SCA SC Integrator

The small-signal equivalent circuit of the SCA SC integrator is shown in Fig. 2(a), where the main OTA is modeled by a single-stage transconductor with an output conductance G_o and a capacitor C_o. The SCA path enhances the linearity by canceling the voltage peak at the virtual ground in Fig. 2(c). The slew rate limit of the main OTA is eliminated by the SCA path. The linear output current is written as $I_{\text{out}}^1 = G_{\text{OTA}} \cdot V_X$, whereas the third-order term output current is given as $I_{\text{out}}^3 = G_{\text{OTA}} \cdot (V_X)^3$. Using the small-signal equivalent circuit (without SCA path) in Fig. 2(a), $V_X(t)$ can be obtained (assuming a step input signal)

$$V_X(s) = \frac{C_s(C_{\text{int}} + C_o)}{\alpha s + G_{\text{OTA}} \cdot C_{\text{int}}} \tag{1}$$

where C_{in} and G_o are ignored and $\alpha = C_{\text{int}}C_S + C_oC_S + C_oC_{\text{int}}$. From (1), the corresponding time domain signal is a decaying pulse signal. Here, $V_x(t)$ is reduced by signal cancelation using the SCA path. $V_X(s)$ of the SCA SC integrator is given as

$$V_X(s) = \frac{\begin{array}{c} s \cdot (C_a \cdot (C_{\text{int}} \cdot V_{\text{in},n} + C_S \cdot V_{\text{in},p}) + V_{\text{in},p} \cdot C_S \\ \cdot (C_{\text{int}} + C_o)) + V_{\text{in},p} \cdot C_S \cdot G_o \end{array}}{s \cdot \left[\begin{array}{c} C_a(C_S + C_{\text{in}}C_{\text{int}}) + C_{\text{int}}(C_S + C_{\text{in}} + C_o) \\ + C_o(C_{\text{in}} + C_{\text{int}}) \\ + G_o(C_S + C_{\text{in}}C_{\text{int}}) + G_{\text{OTA}} \cdot C_{\text{int}} \end{array}\right]} \tag{2}$$

where $V_{\text{in},p} = -V_{\text{in},n}$. A value of C_a can be chosen to nullify $V_x(s)$ during the integration when $G_O \to 0$

$$C_a = \frac{s \cdot C_S \cdot (C_{\text{int}} + C_o)}{s \cdot (C_{\text{int}} - C_S)} \tag{3}$$

where C_L is included in C_o. In practice, R_{ON} is not ignorable in low-power design, and the mismatch between the two paths and parasitic capacitances will damage the voltage cancelation in practice. The exact linearity improvement is detailed in Section III. Meanwhile, when C_S is close to or larger than C_{int}, the sought C_a will approach infinite or will turn negative. Fortunately, in SC LPFs, C_{int} is typically several times larger than C_S.

B. Speed Improvement of the SCA SC Integrator

The SCA path is used to share the charging operation with the main OTA (G_{OTA}) in a short interval defined by Φ_{2_SCA}. Yet, the SCA path is not power free during Φ_1, as shown in Fig. 1(b), where the auxiliary OTA has to sample $V_{\text{in},n}$. Thus, the speed-to-power efficiency should be optimized. During Φ_1, C_a is charged by the auxiliary OTA. During Φ_{2_SCA}, the charge stored on C_a is transferred to the integrator's output (V_{out}). The transferred charge depends on f_s, the size of C_a, the duration of Φ_{2_SCA}, and the on-resistance (R_{ON}) of the switches. The charging accuracy is related to G_a during Φ_1, and $V_{\text{in\_eq}}$ is the voltage difference of C_a in this phase. During Φ_{2_SCA} in Fig. 2(a), the charge on C_a that can be delivered to C_L' is given by

$$Q_{\text{dis}}(t) = V_{\text{in\_eq}} \cdot \left(1 - e^{\frac{G_a}{C_a}t}\right) \cdot \frac{C_L' C_a}{C_L' + C_a} \cdot \left[1 - e^{\frac{-(C_L' + C_a)}{2R_{\text{ON}}C_L'C_a}t}\right] \tag{4}$$

where G_a is the transconductance of the auxiliary OTA and C_L' is the C_{int} in series with C_S. From (4), the charge transferred in the assisting phase can be estimated as

$$\begin{aligned} &Q_{\text{dis}}(t_o) \\ &= V_{\text{in\_eq}} \cdot \left[1 - e^{\frac{-G_a}{C_a}t_{\Phi 1}}\right] \cdot \frac{C_L' C_a}{C_L' + C_a} \cdot \left[1 - e^{\frac{-(C_L' + C_a)}{2R_{\text{ON}}C_L'C_a}t_{\Phi 2\_\text{SCA}}}\right] \end{aligned} \tag{5}$$

where R_{ON} can be downsized by enlarging the MOS switches such that $(C_L' + C_a)/2R_{\text{ON}}C_L'C_at_{\Phi 2\_\text{SCA}} \gg G_a/C_at_{\phi 1}$ is satisfied in most cases. Thus, the settling accuracy of C_a is dominated by the first term, the relation between accuracy and G_a can be plotted, and the optimum value can be obtained via a mathematical tool like Maple on (5). For instance, a value of $G_a/G_{\text{OTA}} = 0.2$ can be chosen for balancing the power and the accuracy. The output comparison is plotted in Fig. 2(b) by the same procedure given in [8], and a 1.76× improvement of the speed-to-power efficiency is obtained.

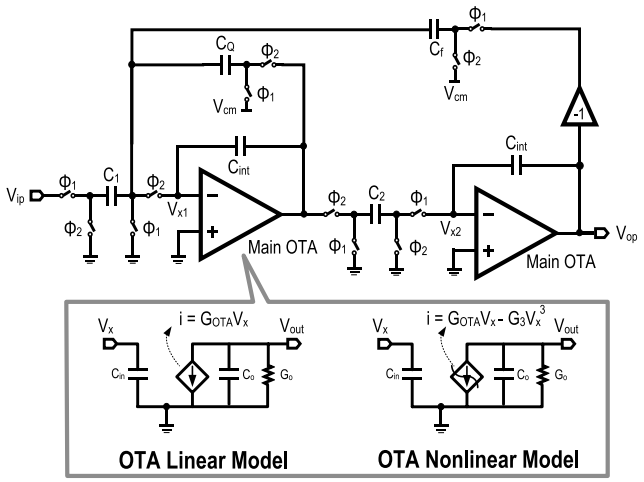


Fig. 3. Typical Tow-Thomas SC biquad in its single-ended form. The main OTA can be referred to a linear or weakly nonlinear model.

C. Noise Consideration of the SCA Path

When the continuous-time output noise is considered, the output noise includes the dominant sample-and-hold (S/H) noise (narrow-band) and the wideband direct noise [4]. As they are uncorrelated, the total output noise power is their sum. The noise of the SCA path will not be exacerbated because: 1) the assisting phase only lasts for a small portion of the whole period; 2) the SCA path will not affect the S/H noise of the C_S path; and 3) C_a connected to the output will lower the direct noise generated by the OTA and the switch's ON-resistance.

III. Proposed Techniques for Active-SC Biquads

The SCA technique can be extended to an SC biquad. Fig. 3 shows the single-ended equivalent circuit of an SC biquad with linear and nonlinear models of the OTA. Its speed improvement is analyzed here for the Tow-Thomas topology, which consists of two integrators connected in a loop. Thus, the biquad pole frequency ω_0 [9] experiences a change that can be expressed in the form of the integrator's unity-GBW (f_t)

$$\frac{\Delta\omega_0}{\omega_0} \approx \frac{1}{2}(I_1(\omega_0)+I_1(\omega_0)) = -\frac{1}{2}\left(e^{-K_1}\left[1-\left(\frac{C_{\text{int}}}{C_{\text{int}}+C_1}\right)\cos(\omega_0 T)\right] + e^{-K_2}\left[1-\left(\frac{C_{\text{int}}}{C_{\text{int}}+C_2}\right)\cos(\omega_0 T)\right]\right) \quad (6)$$

where $K_n = \pi(C_{\text{int}}/C_{\text{int}}+C_n)(f_t/f_t)$. The BW improvement of the biquad according to (6) is plotted in Fig. 4 under the same power with and without the SCA path. $G_{\text{OTA}} = 3$ mS is chosen for balancing the performance with power.

Volterra operators are employed for distortion analysis of the main OTA that can be replaced with a weakly nonlinear model (Fig. 3). From [10], the third-order distortion of the biquad can be expressed as follows using a two-loop model:

$$D_3(S_1,S_2,S_3) = \frac{H_3(S_1,S_2,S_3)}{T_1(S_1)\cdot T_1(S_2)\cdot T_1(S_3)\cdot T_1(S_1+S_2+S_3)} \quad (7)$$

where T_1 is the loop gain and H_3 is the third-order Volterra operator of two integrators in cascade. As the typical linearity tests are based on two closely spaced tones, T_1 can be considered as a frequency-independent variable. Thus, if G_{OTA} is raised without burdening the input and output capacitances, the loop gain is proportional to G_{OTA}, leading to an IM_3 improvement of ~18 dB from (7) for continuous-time LPFs [1]. Differently here, due to the pulse-decaying waveform of the SC circuits at the virtual ground, the linearity is related to both the signal swing and the decaying speed. Thus, if the two paths are well matched, IM_3 reduction is significant. For instance, with two 200-kHz spaced tones (200 mV_{pp}) applied to the SC biquad, the IM_3 can be simulated with respect to the average frequency swept from $0.2f_0$ to $1.8f_0$ (f_0: the designed cutoff band edge). When the SCA path is enabled, the linearity is improved by voltage cancelation. With it, the simulated IM_3 is improved more than 2 dB (Fig. 4) for the same power consumption.

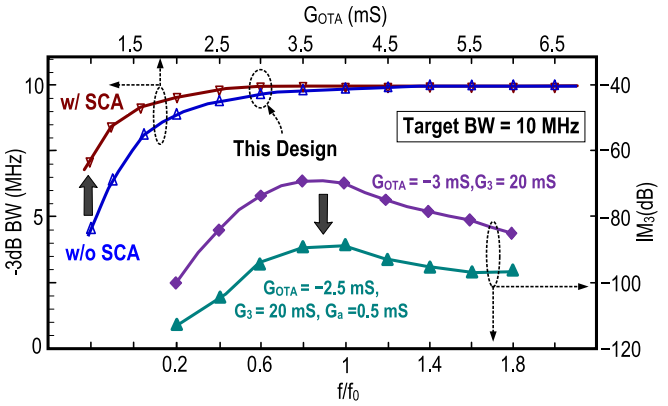


Fig. 4. Simulated BW and linearity improvement of biquad under the same power consumption with and without SCA path.

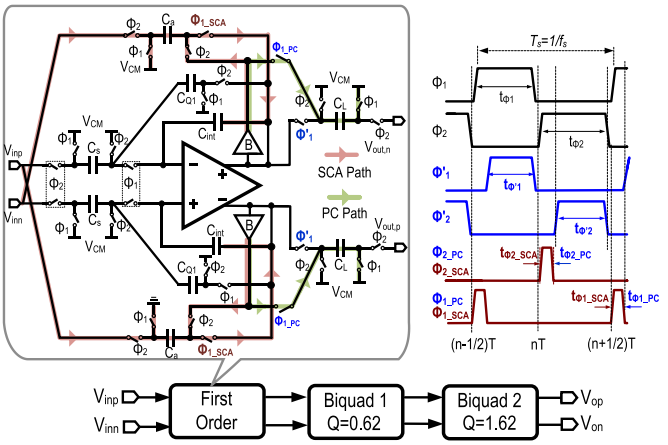
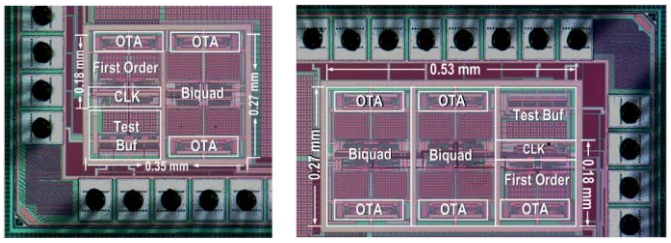


Fig. 5. Schematic of the fifth-order Butterworth SC LPF by cascading the first-order filter (fully differential with load capacitor) with the SCA and PC techniques applied in two biquads.

IV. Circuit Implementation and Experimental Results

Three SC LPFs (first order, biquad, and fifth-order Butterworth) were designed to verify the proposed techniques (Fig. 5). The fifth order is based on the cascade of one first order and two biquads. To maximize the dynamic range, the high-Q (1.62) biquad is located at the last stage to balance the swing at the internal nodes. The SCA and PC paths can be disabled so that their effectiveness can be assessed fairly. The selected f_s is 20× the $f_{-3\text{ dB}}$. For the biquad with $Q = 0.71$, the normalized capacitor ratio is summarized as follows: $C_{S2} = C_1 = C_2 = 1$, $C_{\text{int2A}} = C_{\text{int2B}} = 3.18$, and $C_{Q2} = 0.71$. The two biquads of the fifth-order LPF only differ in the C_{Q2} value for $Q_1 = 0.62$ and $Q_2 = 1.62$. Similarly, the optimized unit capacitor C_{unit} is 288 fF (metal-over-metal cap cell



(a) (b)

Fig. 6. Chip photo of the (a) first order, biquad, and (b) fifth-order SC LPFs fabricated in 65-nm CMOS.

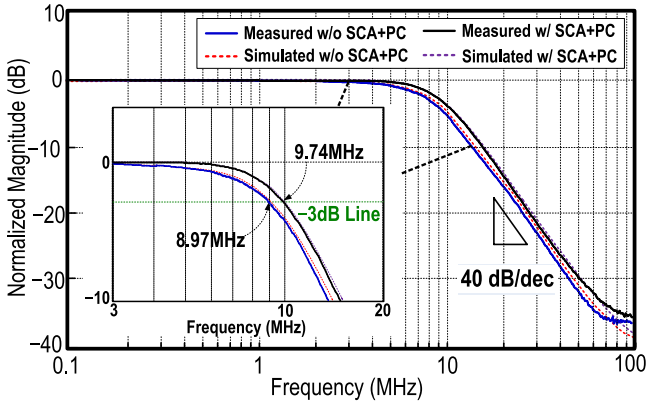


Fig. 7. Measured and simulated BW accuracy of the SC biquad with and without the proposed techniques for a 10-MHz BW target.

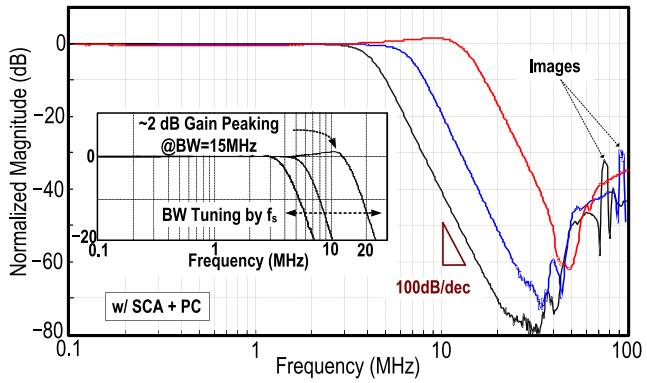


Fig. 8. Measured transfer function of the fifth-order SC Butterworth LPF with the proposed techniques.

with 19.2 fF×15), which balances the layout effort with the required matching accuracy. The schematics of the main OTA (folded-cascode) and auxiliary buffer have been described in [8]. For multistage OTAs that entail Miller or other feedforward compensations, the assisting path will be more complicated as in the continuous-time domain [1], but a similar analysis can be applied as above. The total bias current of the main OTA is 500 μA, which results in a 64-dB dc gain and a 380-MHz GBW at a 600-fF load for a 10-MHz BW. For the auxiliary OTA, it is a simple differential pair with a current-mirror load for a high speed-to-power efficiency. The simulated dc gain is 31 dB and GBW is 150 MHz at a 600-fF load and 100-μA bias current.

The first-order, biquad, and fifth-order SC LPFs fabricated in 65-nm CMOS (Fig. 6) occupy 0.032, 0.048, and 0.127 mm^2, respectively, excluding the test buffers. The signal path is powered at 1.2 V, while the clock generator is operated at 1 V. The results reported here are mainly focused on the SC biquad, which is the key building block for higher order synthesis. Fig. 7 shows the measured and simulated transfer functions for a BW target of 10 MHz. The BW accuracy is enhanced from 9 to 9.7 MHz with the proposed

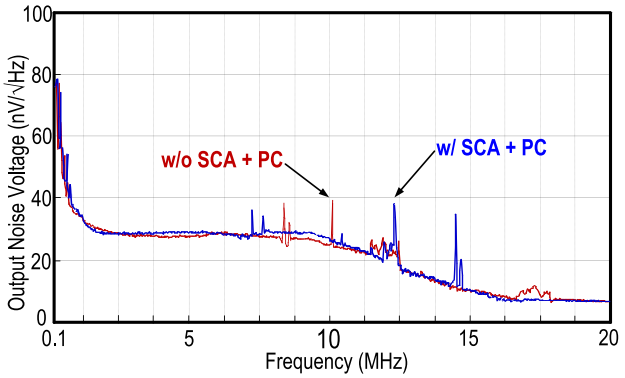


Fig. 9. Measured output noise voltage with and without the proposed techniques of the biquad with the BW target at 10 MHz.

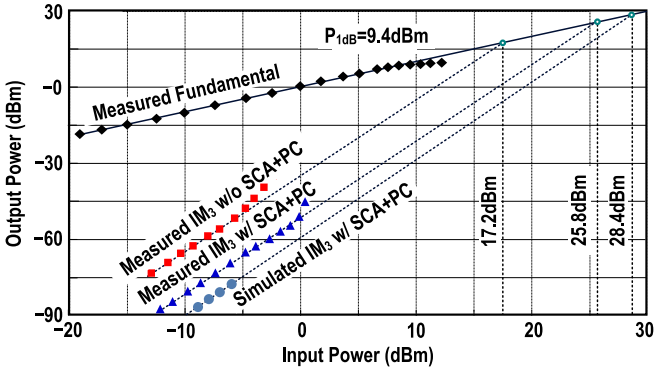


Fig. 10. Linearity improvement of the proposed SC biquad under the same power with and without the proposed SCA and PC techniques.

TABLE I
SUMMARY OF PERFORMANCE FOR FIRST ORDER AND BIQUAD SC LPFS WITH AND WITHOUT THE SCA AND PC TECHNIQUES

		Biquad SC LPF		First order SC LPF	
		w/o SCA + PC	**w/ SCA + PC**	w/o SCA + PC	**w/ SCA + PC**
Power @ 10 MHz BW	Main OTA	1.68mW	**1.2mW**	0.84mW	**0.6mW**
	Auxi. OTA	N/A	**0.48mW**	N/A	**0.24mW**
	CLK Gen.	1.0mW *	**1.0mW ***	1.0mW *	**1.0mW ***
	Total	2.68mW	**2.68mW**	1.84mW	**1.84mW**
Cutoff Acc. @ 10 MHz		90%	**97%**	92%	**98%**
In-band IIP3		+17.2 dBm	**+25.8 dBm**	+20.6 dBm	**+29.8 dBm**
-1-dB Comp. Point		+6.4 dBm	**+9.4 dBm**	+7.5 dBm	**+11.2 dBm**
IRN		30 nV/√Hz	**31.4 nV/√Hz**	24.7 nV/√Hz	**26.9 nV/√Hz**
Die Area		0.048 mm^2		0.032 mm^2	

*:First order and Biquad share the same clock generator

techniques. The BW of the fifth-order can be tuned by adjusting f_s (Fig. 8). The stopband profile (100 dB/decade) is consistent in all cases. The images are due to the discrete-time nature of the signal processing [5] that can be suppressed by an antialiasing filter in practice. The peaking of ~2 dB at a 15-MHz BW is due to the limited GBW of the main OTA when it is comparable with f_s. The stopband rejection is >70 dB for a BW < 10 MHz.

The measured output noise power spectral density (Fig. 9) of the biquad is roughly the same with and without the SCA and PC techniques as analyzed above. The average input-referred noise is ~31 nV/$\sqrt{}$Hz over a BW of 10 MHz.

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART LPFS

	This Work	JSSC'11 [2]	ISSCC'12 [3]	TVLSI'14 [11]
Technology	65 nm	90 nm	90 nm	55 nm
Architecture	Active SC + SCA + PC	Gm-C	Ring Osc. Integrator	Gm-C + Active SC
Filter Order, *N*	5^{th}, Butterworth	6^{th}, Butterworth	4^{th}, Butterworth	3^{rd}, Butterworth
Bandwidth (MHz), BW	1.5 to 15	8.1 to 13.5	7 to 30	2.5(Fixed)
Bandwidth Tuning	Clock Rate	Coarse (Cap Bank) Fine (Bias Current)	Supply Voltage	N/A
In-Band IIP3 (dBm)	+23.5 @ 10MHz BW	+22.1 @ 10MHz BW	16.7@ 7MHz BW	+12 @ 2.5MHz BW
Out-of-Band IIP3 (dBm)	+24.8 @ 20 & 32 MHz	+18.9 @ 20 & 32MHz	N/A	+33 @ 10 & 19.5MHz
IRN (nV/√Hz), P_N	35	75	23.7 to 32.8	6.8
Area (mm²)	0.127	0.24	0.29	0.2
Power (mW), P_c	2.3 to 7.8	4.35	2.9 to 19.1	0.365
FOM (fJ) *	0.014	0.024	0.0228	0.0031

$$* \text{FOM} = \left({}^{P_C}/_{N \cdot BW}\right) / \left(\left(\frac{IIP3}{P_N}\right)^{2/3} \cdot N^{4/3}\right)$$

The in-band linearity is assessed at a 10-MHz BW. With two cutoff band-edge tones (9.4 and 9.6 MHz) applied, the input-referred 3rd-order intercept point is improved from +17.2 to +258 dBm after enabling the SCA and PC paths (Fig. 10). The difference of the measured (+258 dBm) and simulated (+284 dBm) performances is mainly due to the mismatch between paths and parasitic capacitances. The results for the first-order SC filter are summarized in Table I. The fifth-order LPF is compared with the prior art in Table II.

V. CONCLUSION

Two circuit techniques, SCA and PC, have been proposed for improving the speed and linearity of active-SC LPFs without penalizing the power and the area. The SCA enhances the charging speed of the integration capacitor, while the PC improves the linearity when charging the load capacitor. Only one auxiliary OTA is entailed for realizing both SCA and PC paths. Three SC LPFs were fabricated to verify the effectiveness of the proposed techniques; both are applicable to other differential SC circuits like the analog-to-digital converters.

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