Nested-Current-Mirror Rail-to-Rail-Output Single-Stage Amplifier With Enhancements of DC Gain, GBW and Slew Rate

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***Abstract*—For better area and power efficiencies, rail-to-rail-output single-stage amplifiers are a potential replacement of their multi-stage counterparts, especially for display applications that entail massive buffer amplifiers in their column drivers. This paper describes a nested-current-mirror (NCM) technique for a single-stage amplifier to achieve substantial enhancements of DC gain, gain-bandwidth product (GBW) and slew rate (SR). Specifically, NCM is customizable for different mirror steps, and sub mirror ratios, to balance the performance metrics and capacitive-load (C_L) drivability, avoiding any compensation passives while preserving a rail-to-rail output swing. Analytical treatments of the NCM technique in terms of performance limits and robustness reveal that the NCM amplifier can surpass the fundamental power-efficiency limit set by the basic differential-pair (DP) amplifier. Two prototypes, 3-step and 4-step NCM amplifiers, were fabricated in 0.18 μm CMOS for systematic comparison with the DP amplifier. The former represents a robust design exhibiting 72 dB DC gain and 0.0028–0.27 MHz GBW over 0.15–15 nF C_L with $>80°$ phase margin (PM). The latter embodies an aggressive design attaining 84 dB DC gain and 0.013–1.24 MHz GBW over 0.15–15 nF C_L with $>62°$ PM. All amplifiers were sized for the same area (0.0013 mm_2) and power (3.6 μW).**

***Index Terms*—Area efficiency, CMOS, current mirror, DC gain, differential-pair (DP) amplifier, frequency compensation, gain-bandwidth product (GBW), low temperature polysilicon LCD, multi-stage amplifier, nested current mirror, rail-to-rail output swing, single-stage amplifier, slew rate (SR), stability.**

I. Introduction

FOR display applications like wide-dimension low-temperature polysilicon (LTPS) LCD panels that involve thousands of buffer amplifiers in their column drivers, the area and power budgets of each buffer amplifier are extremely tight to meet the market pressure on cost and display quality [1]. Plus, due to the fabrication spread and scale alternative of the panels, the buffer amplifiers should master a wide range of capacitive load (C_L) up to tens of nF, while securing adequately large DC gain (e.g., $>$ 66 dB for 10 bit resolution [2]) and output swing. Currently, multi-stage amplifiers dominate those applications owing to their key advantages of high DC gain and rail-to-rail output swing. However, the need for frequency compensation increases their design complexity, which also restricts their drivability of C_L (range and size), area and power efficiencies [3].

Single-stage amplifiers utilizing C_L itself for frequency compensation can be an attractive solution to optimize the area and power. They can be almost unconditionally stable at any C_L, naturally widening the C_L drivability. In particular, the current-mirror amplifier [Fig. 1(a)] shows this prospective by preserving a rail-to-rail output swing, and the current-mirror factor K offers a freedom to leverage the various performance metrics such as effective transconductance ($G_{m,eff}$), output resistance (R_o), gain-bandwidth (GBW) product and slew rate (SR). Yet, the intrinsic DC gain is relatively low, only comparable to that of the differential-pair (DP) amplifier [Fig. 1(b)]. This reality confirms that most classical single-stage amplifiers were underused in large-C_L applications when compared with their multi-stage counterparts. In fact, under the same power budget no matter how large is K, the current-mirror amplifier is still lagging behind the DP amplifier for most performance metrics (Table I). As a result, the DP amplifier is in general chosen as the "golden reference" for benchmarking different amplifier topologies [4]. Table I also includes the two-stage amplifier with simple Miller compensation (SMC) [Fig. 1(c)]. We see that except the DC gain and output swing, the DP amplifier typically performs better than the SMC amplifier for most metrics at equal power, regardless of C_L size.

This paper introduces a nested-current-mirror (NCM) single-stage amplifier [5] that can alleviate the tight performance trade-offs in conventional single-stage amplifier topologies, including the fundamental DP amplifier. The prototyped 3-step and 4-step NCM amplifiers achieve favorable performances with respect to the standard DP amplifier, and are comparable with the state-of-the-art of three-stage amplifiers. The developed NCM principle and circuit implementation are different from those recently developed for low-dropout (LDO) regulator [6] and large-C_L amplifier [7], even they also aim to improve the DC gain, GBW and SR via efficiently using the small-gain stages.

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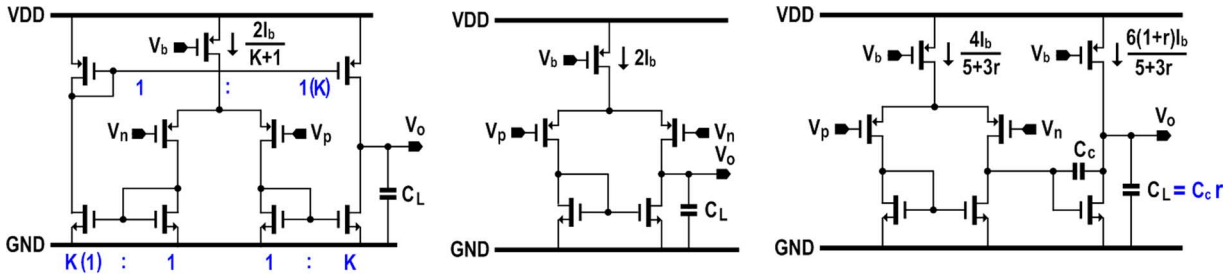


Fig. 1. Conventional (a) current-mirror amplifier, (b) differential-pair (DP) amplifier, and (c) simple Miller compensation (SMC) amplifier [3].

TABLE I
PERFORMANCE COMPARISON BETWEEN THE DP, CURRENT-MIRROR, AND SMC AMPLIFIERS UNDER EQUAL POWER

	Current-Mirror Amplifier	Differential-Pair (DP) Amplifier	SMC Amplifier*
$G_{m,eff}$	$\frac{K}{K+1}g_{mp}$	g_{mp}	$\frac{2}{5+3r}g_{mp}$
R_o	$\frac{K+1}{K}(r_{on}\|\|r_{op})$	$r_{on}\|\|r_{op}$	$\frac{5+3r}{6(1+r)}r_{on}\|\|r_{op}$
GBW	$\frac{K}{K+1}\frac{g_{mp}}{C_L}$	$\frac{g_{mp}}{C_L}$	$\frac{2r}{5+3r}\frac{g_{mp}}{C_L}$
DC Gain	$g_{mp}(r_{on}\|\|r_{op})$	$g_{mp}(r_{on}\|\|r_{op})$	$[g_{mp}(r_{on}\|\|r_{op})]^2$
Slew Rate	$\frac{K}{K+1}\frac{2I_b}{C_L}$	$\frac{2I_b}{C_L}$	$\frac{2r}{5+3r}\frac{2I_b}{C_L}$
Noise	$\frac{8\kappa_B T\gamma}{g_{mp}}\frac{(K+1)^2}{K}\left(1+\frac{g_{mn}}{g_{mp}}\right)$	$\frac{8\kappa_B T\gamma}{g_{mp}}\left(1+\frac{g_{mn}}{g_{mp}}\right)$	$\frac{5+3r}{2}\frac{8\kappa_B T\gamma}{g_{mp}}\left(1+\frac{g_{mn}}{g_{mp}}\right)$
Phase Margin	$< 90°$ depends on K	~90°	~70°

Transconductance & output resistance of NMOS [g_{mn}, r_{on}] and PMOS [g_{mp}, r_{op}];

*For the SMC amplifier, the pole associated with the output is placed at 3x GBW to achieve ~70° PM.

Section II discusses the current-mirror amplifier and its variants, while giving the essential insights that inspire the proposed NCM solution as detailed in Section III. The analytical treatments of mismatch and robustness under different steps of NCM are given in Section IV, followed by the experiment results given in Section V. The conclusions are drawn in Section VI.

II. Benefit and Performance Limits of Existing Single-Stage Amplifiers

This section evaluates the benefit and performance limits of the state-of-the-art single-stage amplifiers [8]–[10] that are variants of the rail-to-rail output current-mirror topology [Fig. 1(a)]. Their capability of enhancing the DC gain, GBW and SR are explored that stimulates the proposed solution.

A. Current-Mirror Amplifier With Shunt Current Sources

Fig. 2(a) depicts a current-mirror amplifier with shunt current sources [8], where the diode-connected transistors M_{5a-6a} are shunt by a pair of fixed current sources M_{3a-4a}. Adding M_{3a-4a} allows budgeting more bias current to the input stage, while reducing that in the output stage. The mirror ratio K_2 can be sized as that of the typical current-mirror amplifier, but already improving the effective transconductance $G_{m,CS}$, output resistance $R_{o,CS}$, SR (SR_{CS}), and noise performance. The compromise is the parasitic effect induced by M_{3a-4a} that slightly lowers the position of the non-dominant pole at node X_1 or Y_1 penalizing the PM. The key metrics: $G_{m,CS}$, $R_{o,CS}$, SR_{CS}, and input-referred thermal noise, are calculated respectively as

$$G_{m,CS} = \frac{K_2(K_1+1)}{K_2+K_1+1}g_{mp} \tag{1}$$

$$R_{o,CS} = \frac{K_2+K_1+1}{K_2}(r_{on}\|r_{op}) \tag{2}$$

$$SR_{CS} = \frac{K_2(0.5K_1+1)}{K_2+K_1+1}\frac{2I_b}{C_L} \tag{3}$$

$$\overline{v_{n,CS}^2} \approx \frac{8\kappa_B T\gamma}{g_{mp}}\left(\frac{K_2+K_1+1}{K_1+1}\right) \cdot \left(1+\frac{K_2+K_1+1}{K_1+1}\frac{g_{mn}}{g_{mp}}\right). \tag{4}$$

B. Current-Mirror Amplifier With Current Reuse

The bias current of the shunt current sources in [8] can be recycled by introducing another DP (M_{3b-4b}) to cross-couple M_{5b-6b} [9], as shown in Fig. 2(b). This cross-connection ensures the transconductances of M_{3b-4b} are summed in phase with those of M_{1b-2b}, resulting in further augmented effective transconductance $G_{m,CR}$. It also saves the use of extra circuitry that biases M_{7b-8b}. During the large-step responses, the added DP disables M_{7b} or M_{8b}, rendering more current to be amplified

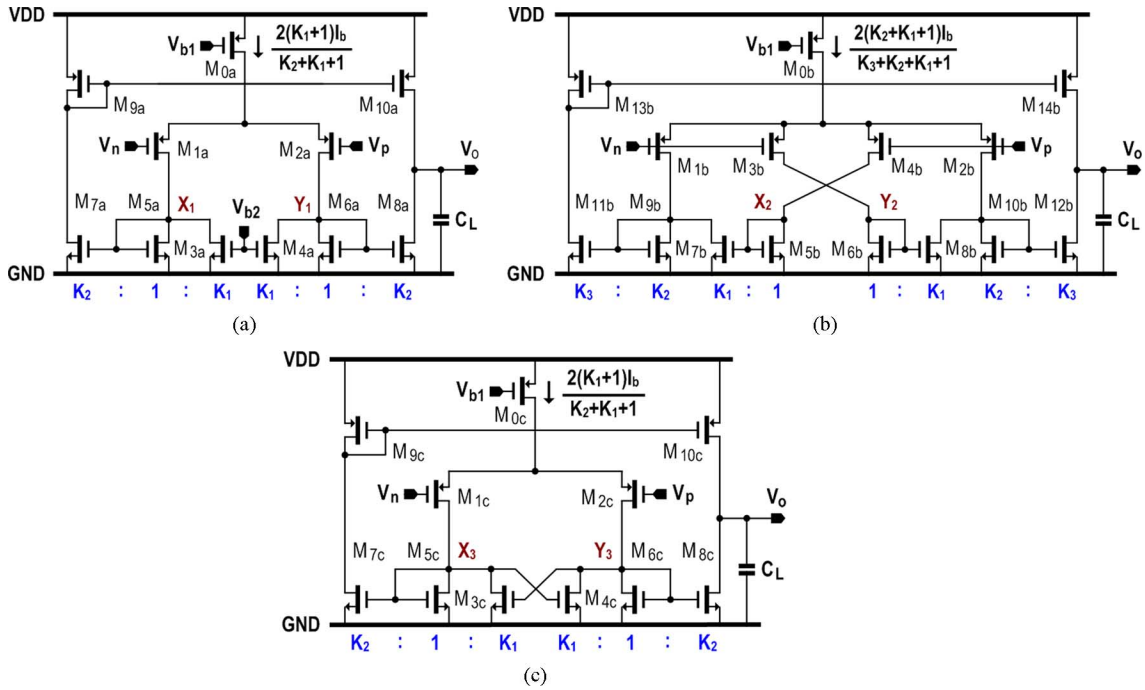


Fig. 2. Single-stage amplifiers developed from the current-mirror amplifier: (a) with shunt current sources; (b) with current reuse; (c) with local positive feedback. All feature a rail-to-rail output swing.

by the last current mirror ($M_{9b} : M_{11b}$ or $M_{10b} : M_{12b}$). Thus, the SR of this topology (SR_{CR}) can surpass that of [8] with only the shunt current sources. Additionally, as this topology features two more current mirrors, there is more design freedom to leverage the DC gain, GBW, SR and noise. The added current mirrors also create a pole that associated with X_2 and Y_2. M_{1b} and M_{2b} form the feedforward signal paths, generating a left-half-plane (LHP) zero which together with the added pole constitutes a pole-zero doublet. The extent of the PM's loss depends on the size of C_L and the ratios of the current mirrors. The key metrics are derived as

$$G_{m,CR} = \frac{K_3}{K_2}\frac{K_2+2K_1}{K_3+K_2+K_1+1}g_{mp} \tag{5}$$

$$R_{o,CR} = \frac{K_3+K_2+K_1+1}{K_3}\left(r_{on}\|r_{op}\right) \tag{6}$$

$$SR_{CR} = \frac{K_3}{K_2}\frac{K_2+K_1}{K_3+K_2+K_1+1}\frac{2I_b}{C_L} \tag{7}$$

$$\overline{v_{n,CR}^2} \approx \frac{8\kappa_B T\gamma}{g_{mp}}\left[\frac{(K_3+K_2+K_1+1)(2K_2+K_1+1)}{(2K_1+1)^2}\right] \cdot \left(1+\frac{g_{mn}}{g_{mp}}\right). \tag{8}$$

C. Current-Mirror Amplifier With Local Positive Feedback

The current-mirror amplifier with local positive feedback is shown in Fig. 2(c) [10]. Unlike the solutions in [8] and [9], two cross-coupling transistors M_{3c-4c} are placed in parallel with the diode-connection transistors M_{5c-6c}. This act not only performs bias-current redistribution, but also generates a negative equivalent resistance to partially cancel the AC resistances of M_{5c-6c}. As a result, the impedances at X_3 and Y_3 are boosted, enhancing the small-signal mirror ratio to $K_2/(1-K_1)$ without altering the large-signal mirror factor K_2. The improved effective transconductance $G_{m,PF}$ is thus significant. During the large-signal step responses, the local positive feedback effect forces the current in M_{0c} to flow only in M_{5c} or M_{6c} while nullifying that in M_{3c} or M_{4c}, and finally being multiplied by the current mirror $M_{5c} : M_{7c}$ or $M_{6c} : M_{8c}$, respectively. Hence, this topology gives the largest SR enhancement. Yet, with K_1 approaching to unity, the resultant drawback is the poles associated with X_3 and Y_3 shift to substantially low frequencies, degrading the PM and tightly constraining the achievable GBW. Also, the GBW will be sensitive to the matching between M_{3c} to M_{6c}. Ultimately, K_1 must be < 1 to limit the amount of positive feedback. Otherwise, the circuit becomes a latch or Schmitt trigger circuit [11]. A reasonable K_1 (e.g., 0.8) can balance the performance boost and robustness against process variations and component mismatches. $G_{m,PF}$, $R_{o,PF}$, SR_{PF}, and input-referred thermal noise of this amplifier can be expressed as

$$G_{m,PF} = \frac{K_2}{1-K_1}\frac{K_1+1}{K_2+K_1+1}g_{mp} \tag{9}$$

$$R_{o,PF} = \frac{K_2+K_1+1}{K_2}\left(r_{on}\|r_{op}\right) \tag{10}$$

$$SR_{PF} = \frac{K_2(K_1+1)}{K_2+K_1+1}\frac{2I_b}{C_L} \tag{11}$$

$$\overline{v_{n,PF}^2} \approx \frac{8\kappa_B T\gamma}{g_{mp}}\frac{K_2+K_1+1}{K_1+1}\left(1+\frac{g_{mn}}{g_{mp}}\right). \tag{12}$$

D. Summary of the Existing Current-Mirror Single-Stage Amplifiers and Their Small-Signal Efficiencies

We studied above if the bias current between the input and output stages of the current-mirror amplifier is distributed efficiently, the effective transconductance, output impedance and

SR can be concurrently improved. This approach is friendlier than the technique of cascoding transistors, as the latter has to sacrifice part of the output swing, while the GBW is not improved due to no change of the effective transconductance. Also, the SR is fixed by the amount of bias current in the tail current source. Alternatively, we can stack multiple DPs to produce a group of amplifiers without increasing the static current [12], equivalently enhancing the overall transconductance, but not the GBW for each single amplifier. The SR is not improved because the transient current available to charge or discharge C_L is not boosted. It also penalizes the voltage headroom and still requires cascoding to boost the output impedance. Finally, this amplifier or a set of amplifiers can only be used for applications that support a set of distinct input common-mode voltages. Class-AB operation can improve SR, but normally entails extra power to contribute to the effective transconductance. To this point, inverter-based amplifiers can be an exception, but at the cost of lower power-supply rejection and narrower input common-mode range. Thus, for a single-stage amplifier, current redistribution should be a more general approach that can simultaneously alleviate the GBW-to-power trade-off, while boosting the output impedance and SR.

The small-signal efficiency $\mathrm{EFF_{ss}} = \mathrm{GBW} \cdot C_L/I_Q$ is widely used to assess the GBW-to-power efficiency of an amplifier [13], where I_Q stands for the amplifier's static current. Assume the transistors follow the square-law drain-current model and their overdrive voltage (V_{ov}) is selected to be 0.2 V. The $\mathrm{EFF_{ss}}$ of the DP amplifier is $1/(2\pi V_{ov}) \approx 800\ \mathrm{MHz \cdot pF/mA}$. This figure bounds how much power is entailed for the DP amplifier to attain the desired GBW at a given C_L. Similarly, the $\mathrm{EFF_{ss}}$ of SMC and class-AB SMC amplifiers, the current-mirror amplifier and three advanced single-stage amplifiers [8]–[10] with a set of typical K, K_1, and K_2 can be calculated against the last mirror ratio as plotted in Fig. 3. As expected, when the last mirror ratio goes up, all the current-mirror amplifiers discussed above can break the limit of GBW-to-power efficiency set by the DP amplifier. For instance, with $K_2 = 5$, the current mirror with local positive feedback attains the highest $\mathrm{EFF_{ss}}$ that is roughly 7× better that of the DP amplifier, but at the expense of PM. Furthermore, the $\mathrm{EFF_{ss}}$ saturates faster when the last mirror ratio is increased. Inspired by this study, a NCM single-stage amplifier that alleviates the hard tradeoffs above is proposed; we utilize different NCM steps and a group of mirror ratios to allow flexible and systematic enhancement of DC gain, GBW and SR.

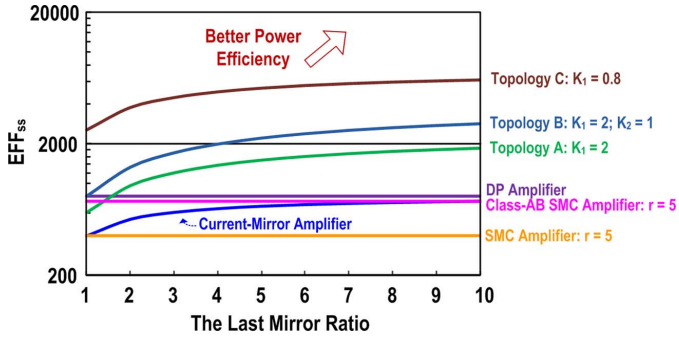


Fig. 3. Performance comparison among the DP, conventional current-mirror, SMC and Class AB SMC amplifiers. Note: topology A, B and C refer to the current-mirror amplifiers with shunt current sources, current reuse and local positive feedback, respectively.

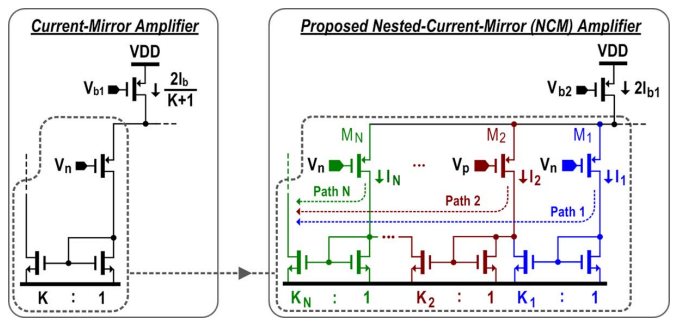
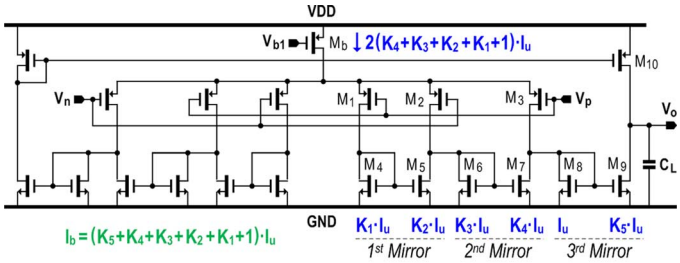


Fig. 4. Development of the NCM amplifier from the current-mirror amplifier.

III. Proposed NCM Single-Stage Amplifier

A. Basic Principles of NCM

The description of the NCM technique consists of two steps (Fig. 4). The first step is to split the DP transistor of the current-mirror amplifier into N sub-transistors M_1 to M_N, and alternately connect their inputs with V_n and V_p. Next, the outputs of M_1 to M_N are combined in sequence via the NCM formed by subdividing a current mirror into pieces with different ratios, which concurrently increases the effective transconductance $G_{m,NCM}$ and output resistance $R_{o,NCM}$ beyond those of the DP, and other single-stage amplifiers [8]–[10]. Specifically, by sharing the current I_{b1} (for the left-half side) with N divided DP transistors $[(I_1, M_1), (I_2, M_2), \ldots, (I_N, M_N)]$, their outputs are combined via N nested current mirrors with ratios $[(1 : K_1), (1 : K_2), \ldots, (1 : K_N)]$. Their inputs are alternately routed with V_n and V_p to ensure their outputs are in-phase summed. Since M_1–M_N are located in the signal path, all their transconductances contribute to $G_{m,NCM}$, and are *customizable* via choosing K_1 to K_N properly. For instance, for Signal Path 1, $g_{m1}(M_1)$ is multiplied by N times, contributing $(K_1 \cdot K_2 \cdots K_N)g_{m1}$ to $G_{m,NCM}$. If high DC gain and GBW are desired, more mirror stages and bigger of their ratios are preferred. Yet, to reduce the noise and random offset voltage, the largest amount of current should be allocated to the 1st mirror with a small K_1. To enhance SR, most of the current can be assigned to the 2nd-last mirror with augmented K_{N-1} and K_N. Indeed, the mirror stages and ratios are limited by the PM and transistor mismatches. If a large C_L is imposed, PM is no longer the stability constraint. For the mismatches, the W and L of transistors can be upsized for better matching (details in Section IV) and higher intrinsic gain. Both are decisive to the expected value of $G_{m,NCM}$ and $R_{o,NCM}$. For very low-power design (e.g., nW regime), the leakage current might be a factor that limits the number of mirror stages. This is because at the highest temperature and fast corners the intrinsic gain of the transistors is significantly reduced. Along such a NCM process, $R_{o,NCM}$ is improved as well since less current is directed to the output stage. Thus, the DC gain can be as high as that of single-stage cascode amplifier, but without the output swing penalty. Moreover, unlike the typical current-mirror amplifier, cutting the current of the output stage does not essentially



Device	Size(μm/μm)	Device	Size(μm/μm)	Device	Size(μm/μm)
M_1	2/0.8 (x2)	M_5	1.3/1.3 (x3)	M_9	1.3/1.3 (x5)
M_2	2/0.8 (x4)	M_6	1.3/1.3	M_{10}	2/0.8 (x5)
M_3	2/0.8 (x4)	M_7	1.3/1.3 (x3)	M_b	3/2 (x4)
M_4	1.3/1.3 (x2)	M_8	1.3/1.3		

Fig. 5. The schematic of the 3-step NCM amplifier with the half-side device sizes.

degrade the SR. In fact, as long as $K_N \cdot I_N > I_b$, the SR of the proposed NCM amplifier can still outperform that of the DP amplifier.

The number of NCM step is a design parameter. We show below the 3-step and 4-step designs as they can provide appreciable performance gain, while allowing the design metrics to be analytically tractable and usable. A NCM step ≥ 5 will raise the design complexity dramatically as there will be many parameters to manage. In addition, the benefit of SR boost will diminish.

B. Three-Step NCM Single-Stage Amplifier

Fig. 5 shows the schematic of a 3-step NCM amplifier, with the sizing details marked on the right half. The DP transistors are split into M_1–M_3. Their outputs are summed via the NCM mirrors realized by M_4–M_9. M_{10} collects the output of the left, to form the single-ended output together with M_9. To show how the mirror ratios K_1 to K_5 contribute to the effective transconductance ($G_{m,NCM3}$), GBW, DC gain, SR, and noise, quantitative analyses are conducted, and they are valid for both single-ended output and differential output implementations.

1) $G_{m,NCM3}$ is first calculated by finding the small-signal short current at the output with respect to the input, which is given by

$$G_{m,NCM3} = \frac{K_5\left[2K_4\left(\frac{K_3+K_2}{K_3}\right)+1\right]}{\sum_{i=1}^{5} K_i + 1} g_{mp}. \tag{13}$$

As indicated in (13), $G_{m,NCM3}$ is mainly determined by the product of K_5 and $K_4 \cdot (K_3+K_2)/K_3$ with a given sum of K_1 to K_5. Since the product is readily sized to be much higher than the sum, $G_{m,NCM3}$ is significantly boosted, usually in one or two order(s) of magnitude higher than that of the DP amplifier (i.e., g_{mp}) for the same power consumption. This also indicates that the 3-step NCM amplifier has the same GBW improvement over the DP amplifier.

2) The DC gain of the 3-step NCM amplifier is expressed as the product of $G_{m,NCM3}$ and its output resistance $R_{o,NCM3}$. In addition to $G_{m,NCM3}$ that already considerably improves its DC gain, $R_{o,NCM3}$ is also enhanced over that of the DP amplifier, and can be represented by

$$R_{o,NCM3} = \frac{\sum_{i=1}^{5} K_i + 1}{K_5}\left(r_{on} \parallel r_{op}\right). \tag{14}$$

The gain enhancement seen in $R_{o,NCM3}$ is attributed to substantial bias current reduction in the output stage in comparison with that of the DP amplifier. Thus, an overall DC gain enhancement of > 30 dB over the DP amplifier can be observed, while should be better than those (10 to 20 dB) of other topologies as discussed in Section II.

3) SR determines the amplifier's settling performance. The SR of the 3-step NCM amplifier SR_{NCM3} can be analyzed according to Fig. 6. Suppose a large negative step appears at V_p, it follows that the 2nd mirror turns off. Consequently, almost all the current in M_3 is directed into M_8 and amplified by the 3rd mirror to discharge C_L. As long as the amplified current is $> 2I_b$, the negative SR can be better than the DP amplifier. Similar analyses can be applied when there is a large positive input step occurring at V_p, resulting in a symmetric SR expressed by

$$SR_{NCM3} = \frac{K_5\left(K_4+1\right)}{\sum_{i=1}^{5} K_i + 1}\frac{2I_b}{C_L}. \tag{15}$$

Examining (15) implies that if $K_5 \cdot (K_4+1) > K_5 + K_4 + K_3 + K_2 + K_1 + 1$, the SR of the proposed amplifier surpasses that of the DP amplifier at equal power, which can be realized by selecting relatively large K_4 and K_5.

4) Noise can be a limiting factor in certain applications. Since the analysis of both thermal and flicker noise follows the same procedure outlined in [14], only the input-referred thermal noise of the 3-step NCM amplifier is provided here, which is given by

$$\overline{v_{n,NCM3}^2} \approx \frac{\left(\sum_{i=1}^{5} K_i+1\right)\left[\left(\frac{K_4}{K_3}\frac{K_2}{K_1}\right)^2 K_1+\left(\frac{K_4}{K_3}\right)^2(K_3+K_2)+K_4+1\right]}{\left[2\left(\frac{K_4}{K_3}K_2+K_4\right)+1\right]^2} \cdot \frac{8\kappa_B T\gamma}{g_{mp}}\left(1+\frac{g_{mn}}{g_{mp}}\right). \tag{16}$$

Compared to that of the DP amplifier, it is unobvious from (16) that the NCM amplifier generates more noise. But intuitively when $G_{m,NCM3}$ is enhanced by the NCM, the transistors' noise is also amplified by the mirror ratios. Thus, the NCM amplifier has to tradeoff the noise performance for a better $G_{m,NCM3}$.

5) The main sources of random mismatch in a pair of identically designed MOS transistors are from the threshold voltage (ΔV_{th}) and the current factor ($\Delta\beta$ where $\beta = \mu C_{ox} W/L$) [15]. Assume that A_{thn} and A_{thp} are threshold

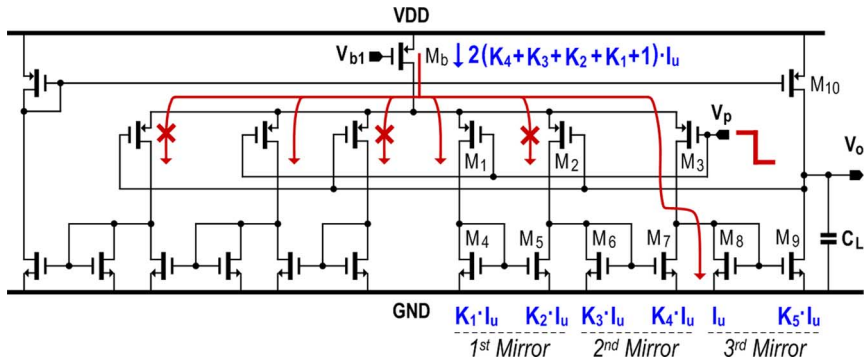


Fig. 6. SR analysis of a 3-step NCM amplifier.

mismatch factors of NMOS and PMOS, respectively, while $A_{\beta n}$ and $A_{\beta p}$ correspond to the current mismatch factors of NMOS and PMOS. The input-referred offset voltage of the 3-step NCM amplifier can be obtained by calculating the total drain-current standard deviation (σ) at the output and then referred to the inputs of the DP transistors by dividing $G_{m,NCM3}$, which is given as in (17), shown at the bottom of the page. Since the mirror ratios are the key sizing parameters of NCM, using multiple unit-transistors in parallel is helpful for accurate matching (this often translates into the finger design in the layout). Thus, the unit- transistors with the device area $W_{un} \cdot L_{un}$ (NMOS) and $W_{up} \cdot L_{up}$ (PMOS) are utilized in (17). Also, g_{mnu} (g_{mpu}) denotes the transconductance of the unit-NMOS (PMOS) transistor biased with the unit-current I_u. Generally, the offset contribution due to the current factor mismatches can be neglected as it is much smaller than that from the threshold voltage mismatches with a typical g_m/I_D designed for the input transistors. To further simplify (17), and obtain quantitative assessment of the offset voltage tradeoff, we assume both unit-NMOS and PMOS transistors generate the same transconductance (i.e., $g_{mnu} = g_{mpu}$) and contribute the same amount of offset voltage. For instance, if the mirror factors are selected as the design case to be given below (i.e., $K_1 = 2$, $K_2 = K_4 = 3$, $K_3 = 1$, and $K_5 = 5$), the 3-step NCM amplifier has to tradeoff 1.8× increment of the offset voltage when compared with that of the DP amplifier.

C. Design Case

The sub mirror ratios are handy to increase the design flexibility. A summary of the main performance concerns with mirror ratios is given in Table II, under the knowledge of (13)–(17). For the 3-step NCM, the total bias current ($2I_b = 3\ \mu A$) is divided into 30 unit-current ($I_u = 100$ nA). To leverage the key metrics, the 1st mirror ($M_4 : M_5$) uses a small ratio of only 1.5 ($K_1 = 2$ and $K_2 = 3$). The 2nd mirror ($M_6 : M_7$) draws less current under a larger ratio of 3 ($K_3 = 1$ and $K_4 = 3$) to boost the DC gain and GBW, as they contribute less noise. Also, a larger K_4 enhances the SR. The 3rd mirror ($M_8 : M_9$) is assigned the largest ratio ($K_5 = 5$) to benefit the SR and $G_{m,NCM}$. Substituting these values into (13)–(15), the DC gain, GBW and SR are theoretically improved by 28 dB, 8.33× and 1.33×, respectively, when compared to the DP amplifier. Although the noise voltage of the 3-step NCM amplifier is 1.39× that of the DP amplifier, it is only 0.52× that of the current-mirror amplifier under $K = 5$ (equivalent as K_5 in Fig. 5).

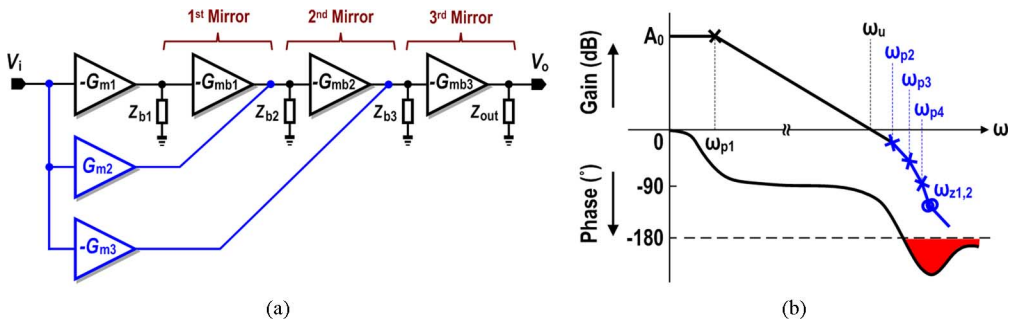
TABLE II
SUMMARY OF MAIN PERFORMANCE CONCERNS WITH MIRROR RATIOS FOR THE 3-STEP NCM AMPLIFIER

	1st mirror	2nd mirror	3rd mirror
Main Concerns	Noise, Offset	Gain, GBW, SR	GBW, SR
Mirror Ratio	Smaller	Larger	Larger
K1 to K5	K1 = 2, K2 = 3	K3 = 1, K4 = 3	K5 = 5

D. Stability Analysis

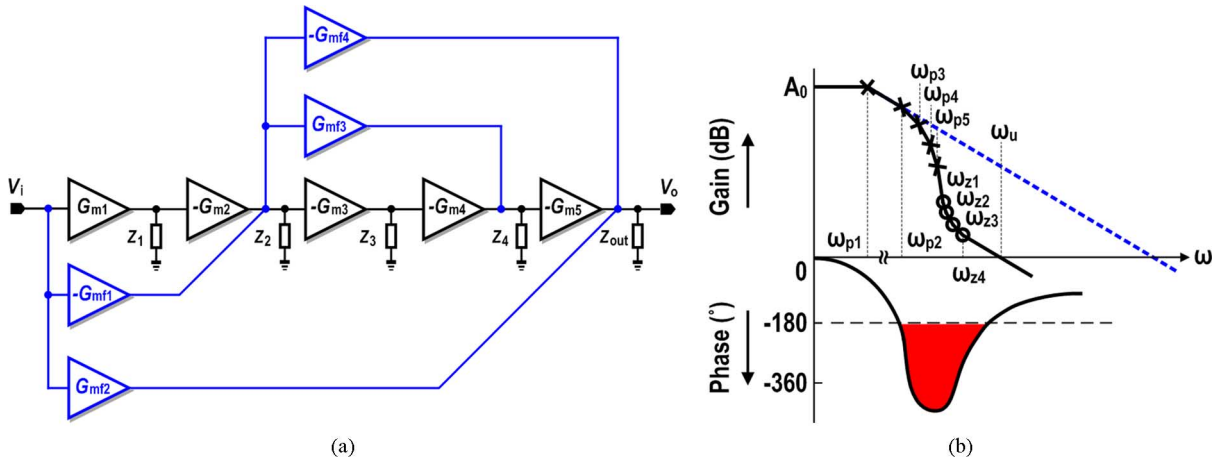
The equivalent small-signal diagram of the 3-step NCM amplifier is shown in Fig. 7(a). G_{m1}, G_{m2}, and G_{m3} are the transconductances of M_{1-3} respectively while Z_{b1}, Z_{b2}, and Z_{b3} correspond to the input impedances of the 1st to 3rd mirrors. The transconductances of the transistors in the three mirrors are respectively represented by G_{mb1-3}, while Z_{out}

$$\sigma_{NCM3}(V_{os}) \approx \frac{\sqrt{\left[\left(\frac{K_4}{K_3}\right)^2\left(K_3+K_2+\frac{K_2^2}{K_1}\right)+K_4+1\right]\left[\frac{A_{thp}^2}{W_{up}L_{up}}+\left(\frac{I_u}{g_{mpu}}\right)^2\frac{A_{\beta p}^2}{W_{up}L_{up}}\right]+\left[\left(\frac{K_4}{K_3}\right)^2\frac{K_2(K_2+K_1)}{K_1}+\frac{K_4(K_4+K_3)}{K_3}+1\right]\left[\left(\frac{g_{mun}}{g_{mpu}}\right)^2\frac{A_{thn}^2}{W_{un}L_{un}}+\left(\frac{I_u}{g_{mpu}}\right)^2\frac{A_{\beta n}^2}{W_{un}L_{un}}\right]}}{2\left(\frac{K_4}{K_3}K_2+K_4\right)+1} \quad (17)$$



(a) (b)

Fig. 7. (a) Block diagram of the proposed 3-step NCM amplifier; (b) its conceptual Bode plot.



(a) (b)

Fig. 8. (a) Block diagram of the feedforward amplifier in [14]; (b) its conceptual Bode plot.

models the output impedance that includes C_L. To derive the transfer function, we assume the following: 1) r_{onu} (r_{opu}) is the output resistance of the unit-NMOS (PMOS) biased with I_u, respectively; 2) the intrinsic gain of the unit NMOS (PMOS) is $\gg 1$; 3) C_{p1-3} correspond to the lumped node capacitances at the gates of the 1st to 3rd mirrors; G_{m1}, G_{m2} and G_{m3} are equal to $K_1 \cdot g_{mpu}$, $(K_2 + K_3) \cdot g_{mpu}$, and $(K_4 + 1) \cdot g_{mpu}$, respectively, and G_{mb1}, G_{mb2}, and G_{mb3} are $K_2 \cdot g_{mnu}$, $K_4 \cdot g_{mnu}$, and $K_5 \cdot g_{mnu}$, respectively. The obtained transfer function of the 3-step NCM amplifier is calculated as

$$A_v(s) = A_0 \frac{\left(1 + \frac{s}{a_1} + \frac{s^2}{a_1 a_2}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)\left(1 + \frac{s}{\omega_{p3}}\right)\left(1 + \frac{s}{\omega_{p4}}\right)} \tag{18}$$

where A_0 is the DC gain, i.e., the product of $G_{m,NCM3}$ in (13) and $R_{o,NCM3}$ in (14). Like all other single-stage amplifiers, ω_{p1}, the dominant pole, is associated with the output stage. ω_{p2}, ω_{p3}, and ω_{p4} are the non-dominant poles due to the 3rd, 2nd, and 1st mirrors, respectively. The two LHP zeros (ω_{z1-2}) are roots of the numerator in $A_v(s)$ and created by the inherent feedforward stages (i.e., G_{m2-3}). Depending on the values of K_1 to K_4, ω_{z1-2} are typically in the form of complex conjugate zeros. As illustrated in Fig. 7(b), they are beneficial to compensate the phase shift produced by ω_{p2-4} at the high frequencies.

Although the explicit multi-path feedforward compensation [Fig. 8(a))] could be employed to generate the LHP zeros for offsetting phase shift at the unity-gain frequency (UGF) ω_u, it requires additional power and circuitry [16]. Moreover, because the non-dominant poles locate at low frequencies, the created LHP zeros locate far beyond them and thus cannot recover the phase lag to be $< 180°$ above ω_u [Fig. 8(b)]. Thus, the explicit multi-path feedforward compensation amplifier is only *conditionally stable* [17], leading to large-signal stability concerns during startup, large transients or saturation recovery [18]. In contrast, the proposed NCM amplifier, except the output node, creates merely low-impedance nodes in the signal path, allowing all the non-dominant poles and LHP zeros to be positioned beyond ω_u. The phase response at all the frequencies below ω_u shows a phase shift much less than 180°. To this end, the NCM amplifier can be considered as *absolutely stable* [17] in large-signal operation. The details of the pole and zero positions of the designed 3-step NCM are shown in Fig. 9, where the Bode plot shows the stability of the proposed amplifier is bounded by the small-C_L condition. For PM $> 65°$ at the smallest C_L (i.e., the highest GBW), ω_{p2} (ω_{p3}) should be placed $\sim 4\times$ ($8\times$) higher than ω_u, while ω_{p4} is positioned at a further higher frequency so that its phase shift at ω_u can be counteracted by ω_{z1-2}.

IV. Transistor Mismatches and Robustness

To investigate the impact of transistor mismatches on the key metrics, a 4-step NCM design with aggressive mirror ratios and reduced transistor area is also designed, as shown in Fig. 10. The static current is 3 μA and divided into 60 units. The consideration shown in Table II justifies the selection of K_1 to K_7.

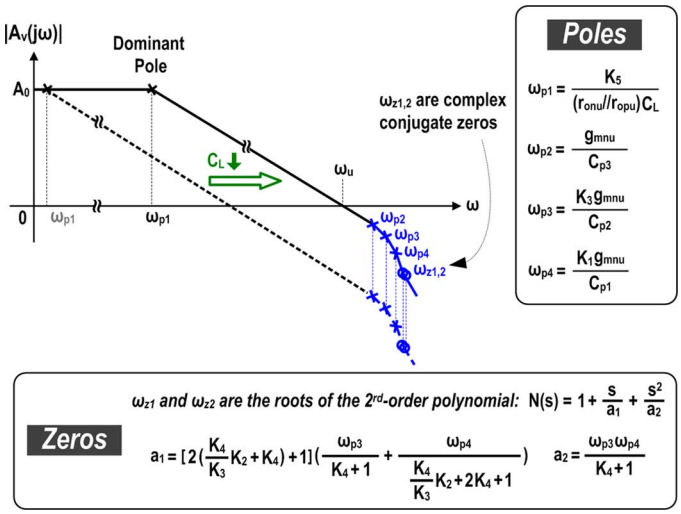


Fig. 9. The pole-zero distribution of the 3-step NCM amplifier.

Fig. 11 depicts the large-signal step responses of both 3-step and 4-step NCMs under 100× Monte-Carlo simulations. At 0.15 nF C_L, the worse rise/fall time at 1% precision of the 3-step (4-step) are 24.6 (19.3) and 23.0 (22.8) μs, respectively. Both results are relatively robust, especially for applications in which the settling time is dominated by the SR (i.e., only determined by the tail current and C_L, and therefore less susceptible to transistor mismatches).

For the small-signal metrics, such as DC gain and UGF, both are vulnerable to transistor mismatches if large mirror ratios and more mirror stages are assigned. This is due to the phenomena different from the traditional mismatch analysis [19]: the random current mismatches, particularly those in the 1st mirror and associated DP input transistors, are successively amplified by the NCM, thereby affecting the DC operation of the NCM amplifier by disabling the diode-connected transistors. The following two subsections study the robustness of 3-step and 4-step NCMs under transistor mismatches.

A. Three-Step NCM Amplifier Under Transistor Mismatches

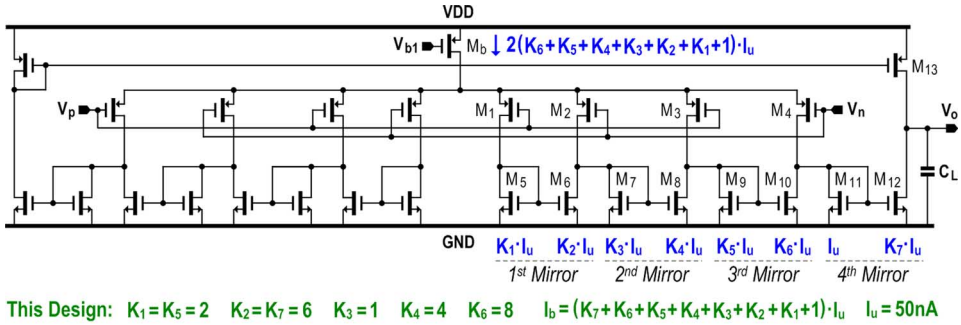
In the 3-step NCM amplifier, if the transistor mismatches are not well-controlled, the diode-connected transistor M_8 shows the highest possibility to exhibit no bias current, destroying the amplifier's DC operation and nullifying the performance enhancement. The impact of ΔV_{th} is first evaluated, which shows the ω of M_8's drain current can be expressed as

$$\sigma_{\mathrm{th,NCM3}}\left(\mathrm{I_{D,M8}}\right) = \sqrt{\left[\left(\frac{\mathrm{K_4}}{\mathrm{K_3}}\right)^2\left(\mathrm{K_3}+\mathrm{K_2}+\frac{\mathrm{K_2^2}}{\mathrm{K_1}}\right)+\mathrm{K_4}+1\right]\frac{(\mathrm{g_{mpu}A_{thp}})^2}{\mathrm{W_{up}L_{up}}}+\left[\left(\frac{\mathrm{K_4}}{\mathrm{K_3}}\right)^2\frac{\mathrm{K_2(K_2+K_1)}}{\mathrm{K_1}}+\frac{\mathrm{K_4(K_4+K_3)}}{\mathrm{K_3}}\right]\frac{(\mathrm{g_{mnu}A_{thn}})^2}{\mathrm{W_{un}L_{un}}}}. \tag{19}$$

Assume the transistors follow the square-law drain-current model, the drain-current σ of M_8 due to the current factors are calculated as in (20), shown at the bottom of the page, where β_{un} and β_{up} are the current factors of the unit-NMOS and PMOS transistors, respectively. Thus, the percentage of σ of the total M_8's drain-current mismatch α_{NCM3} is given by (21), also shown at the bottom of the page. α_{NCM3} is a key metric used to quantify the robustness of the 3-step NCM amplifier. As suggested by (21), with increased mirror factors K_4/K_3 and/or K_2/K_1, α goes up thereby degrading the yield of the amplifier. Also, α_{NCM3} is highly related to the transistors' operating points (g_{mnu}/I_u for NMOS and g_{mpu}/I_u for PMOS) and the sized area ($W_{un}\cdot L_{un}$ for each unit of NMOS, and $W_{up}\cdot L_{up}$ for each unit of PMOS). Similar derivation can be applied to the 4-step NCM to obtain α_{NCM4}. In addition to the most straightforward approach to reduce α_{NCM3} by increasing the device areas, there are several circuit- and layout-level techniques can be applied to the proposed NCM amplifier to

$$\sigma_{\beta,\mathrm{NCM3}}\left(\mathrm{I_{D,M8}}\right) = \frac{1}{2}\sqrt{\left[\left(\frac{\mathrm{K_4}}{\mathrm{K_3}}\right)^2\left(\mathrm{K_3}+\mathrm{K_2}+\frac{\mathrm{K_2^2}}{\mathrm{K_1}}\right)+\mathrm{K_4}+1\right]\beta_{up}^2(\mathrm{V_{GSp}}-\mathrm{V_{thp}})^4\frac{\mathrm{A_{\beta p}^2}}{\mathrm{W_{up}L_{up}}}+\left[\left(\frac{\mathrm{K_4}}{\mathrm{K_3}}\right)^2\frac{\mathrm{K_2(K_2+K_1)}}{\mathrm{K_1}}+\frac{\mathrm{K_4(K_4+K_3)}}{\mathrm{K_3}}\right]\beta_{un}^2(\mathrm{V_{GSn}}-\mathrm{V_{thn}})^4\frac{\mathrm{A_{\beta n}^2}}{\mathrm{W_{un}L_{un}}}} \tag{20}$$

$$\alpha_{\mathrm{NCM3}} = \frac{\sqrt{\sigma_{\mathrm{th,NCM3}}^2\left(\mathrm{I_{D,M8}}\right)+\sigma_{\beta,\mathrm{NCM3}}^2\left(\mathrm{I_{D,M8}}\right)}}{\mathrm{I_{D,M8}}} = \sqrt{\left[\left(\frac{\mathrm{K_4}}{\mathrm{K_3}}\right)^2\left(\mathrm{K_3}+\mathrm{K_2}+\frac{\mathrm{K_2^2}}{\mathrm{K_1}}\right)+\mathrm{K_4}+1\right]\left[\left(\frac{\mathrm{g_{mpu}}}{\mathrm{I_u}}\right)^2\frac{\mathrm{A_{thp}^2}}{\mathrm{W_{up}L_{up}}}+\frac{\mathrm{A_{\beta p}^2}}{\mathrm{W_{up}L_{up}}}\right]+\left[\left(\frac{\mathrm{K_4}}{\mathrm{K_3}}\right)^2\frac{\mathrm{K_2(K_2+K_1)}}{\mathrm{K_1}}+\frac{\mathrm{K_4(K_4+K_3)}}{\mathrm{K_3}}\right]\left[\left(\frac{\mathrm{g_{mnu}}}{\mathrm{I_u}}\right)^2\frac{\mathrm{A_{thn}^2}}{\mathrm{W_{up}L_{up}}}+\frac{\mathrm{A_{\beta n}^2}}{\mathrm{W_{up}L_{up}}}\right]}. \tag{21}$$



Device	Size(μm/μm)	Device	Size(μm/μm)	Device	Size(μm/μm)	Device	Size(μm/μm)
M_1	1/0.36 (x2)	M_5	0.4/0.5 (x2)	M_9	0.4/0.5 (x2)	M_{13}	1.2/0.4 (x2)
M_2	1/0.36 (x7)	M_6	0.4/0.5 (x6)	M_{10}	0.4/0.5 (x8)	M_b	4/1 (x6)
M_3	1/0.36 (x6)	M_7	0.4/0.5	M_{11}	0.4/0.5		
M_4	1/0.36 (x9)	M_8	0.4/0.5 (x4)	M_{12}	0.4/0.5 (x6)		

Fig. 10. The schematic of the 3-step NCM amplifier with the half-side device sizes and selected K_1-K_7 values.

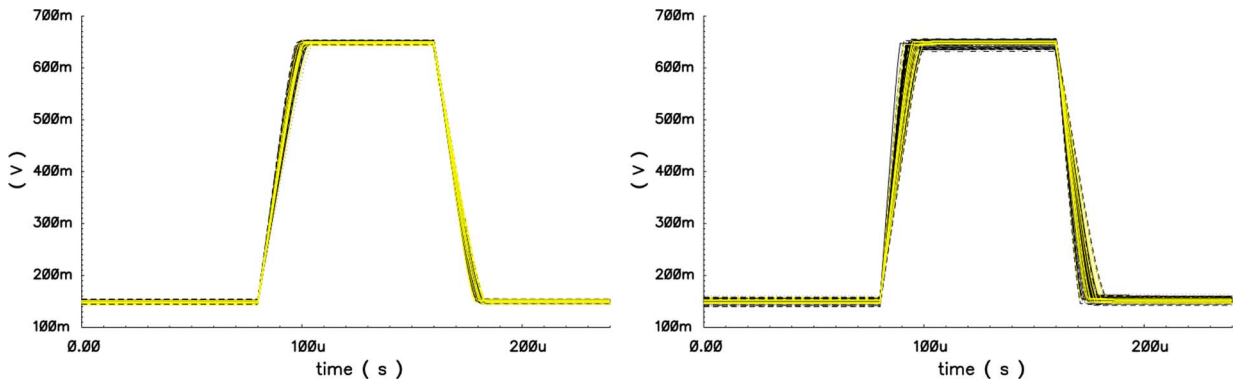


Fig. 11. Large-step (500 mV) responses at 0.15 nF C_L from Monte-Carlo simulations: (a) 3-step NCM; (b) 4-step NCM.

TABLE III
300-RUN MONTE-CARLO SIMULATION RESULTS OVER PROCESS VARIATIONS AND DEVICE MISMATCHES

	3-Step NCM Amplifier @ C_L = 0.15 nF					4-Step NCM Amplifier @ C_L = 0.15 nF				
Metrics	DC Gain (dB)	UGF (MHz)	PM (°)	Offset Voltage (mV)	$\Delta I_{D8}/I_{D8}$ (%)	DC Gain (dB)	UGF (MHz)	PM (°)	Offset Voltage (mV)	$\Delta I_{D11}/I_{D11}$ (%)
Mean	73.4	0.281	84.0	0.383	4	44.7	0.512	80.7	-0.122	200
σ	4.81	0.0026	2.37	2.01	47.4	29.0	0.627	11.0	4.07	240

minimize α_{NCM3}. For example, series-parallel current mirrors are utilized in [20] to realize large ratio current mirrors with reduced current mismatch while multi-dimension current mirror layout techniques are employed in [21] for substantial current mismatch reduction.

B. Three-Step NCM Versus Four-Step NCM

The 3-step NCM is compared with the aggressive 4-step NCM design to study the correlation of mismatches and robustness. From Section IV-A, α_{NCM3} should be downsized for better robustness, via selecting small mirror factors and enlarging the area of the unit-NMOS and PMOS transistors. In the 3-step NCM, the unit-NMOS is sized to be 2/0.8 μm while the unit-PMOS chooses an aspect ratio of 1.3/1.3 μm. They operate at the inversion levels corresponding to $g_{\mathrm{mnu}}/I_{\mathrm{u}} = 22.9\ \mathrm{V}^{-1}$ and $g_{\mathrm{mpu}}/I_{\mathrm{u}} = 22.1\ \mathrm{V}^{-1}$. For the 0.18 μm CMOS technology utilized, A_{thn} (A_{thp}) and $A_{\beta\mathrm{n}}$ ($A_{\beta\mathrm{p}}$) are 3.2 (4.8) mV/μm and $\sim 2(2)\% \cdot \mu$m, respectively. The calculated α_{NCM3} is $\sim 50\%$. The unit-NMOS and PMOS in the 4-step NCM are sized as 1/0.36 μm and 0.4/0.5 μm, respectively. $g_{\mathrm{mnu}}/I_{\mathrm{u}}$ and $g_{\mathrm{mpu}}/I_{\mathrm{u}}$ are designed to be 23.5 V^{-1} and 23.1 V^{-1}. α_{NCM4} for M_{11} is calculated as ~ 3, implying the 4-step NCM amplifier is highly sensitive to the transistor mismatches.

Three-hundred-run Monte-Carlo simulations (with process + mismatch) allow us to quantitatively compare the 3-step and 4-step NCM amplifiers. As shown inTable III, for the 3-step NCM, the mean of the DC gain is ~73 dB (σ <5 dB) while the mean value in the 4-step NCM is only 44 dB ($\sigma \approx 29$ dB). The latter is insufficient for the proposed application that entails >66 dB. Thus, the 3-step NCM is much more robustness

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON OF THE DP, 3-STEP NCM AND 4-STEP NCM AMPLIFIERS

	Typical DP Amplifier			Proposed 3-Step NCM Amplifier			Proposed 4-Step NCM Amplifier		
Load C_L (nF)	0.15	0.5	15	0.15	0.5	15	0.15	0.5	15
UGF (MHz)	0.0371	0.0116	0.00038	0.283	0.083	0.0027	1.24	0.396	0.013
Phase Margin (°)	91.7	92.5	92.9	86.4	88.9	90.2	62.4	81.4	90.2
Gain Margin (dB)	>60	>60	>60	31.5	41.9	>60	15.9	23.7	56.1
SR_{ave} (V/μs)	0.0166	0.0058	0.0002	0.0256	0.0077	0.00025	0.0314	0.0115	0.00037
1% $T_{s,ave}$ (μs)	40.1	109	3280	20.8	71.3	2149	17	47.1	1444
DC Gain (dB) (extrapolated)	43			72			84		
Input-Referred Noise (nV/√Hz)	310 @ 0.1kHz	120 @ 1kHz	80 @ 10kHz	430 @ 0.1kHz	170 @ 1kHz	110 @ 10kHz	1470 @ 0.1kHz	440 @ 1kHz	140 @ 10kHz
Power (μW) @ V_{DD} (V)	3.6 @ 1.2								
Chip Area (mm^2)	0.0013								
CMOS Technology	0.18μm								
FOM_1 [(MHz·pF)/μW/mm^2]	1,189	1,239	1,218	9,071	8,868	8,654	39,744	42,308	41,667
FOM_2 [(V/μs·pF)/μW/mm^2]	532	620	641	821	823	801	1,006	1,229	1,186

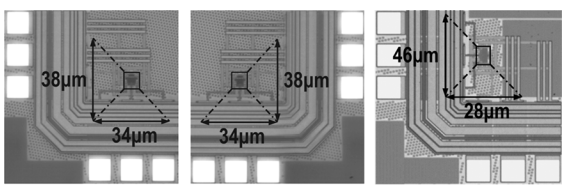


Fig. 12. Die photos: (a) DP amplifier; (b) 3-step NCM amplifier; (c) 4-step NCM amplifier.

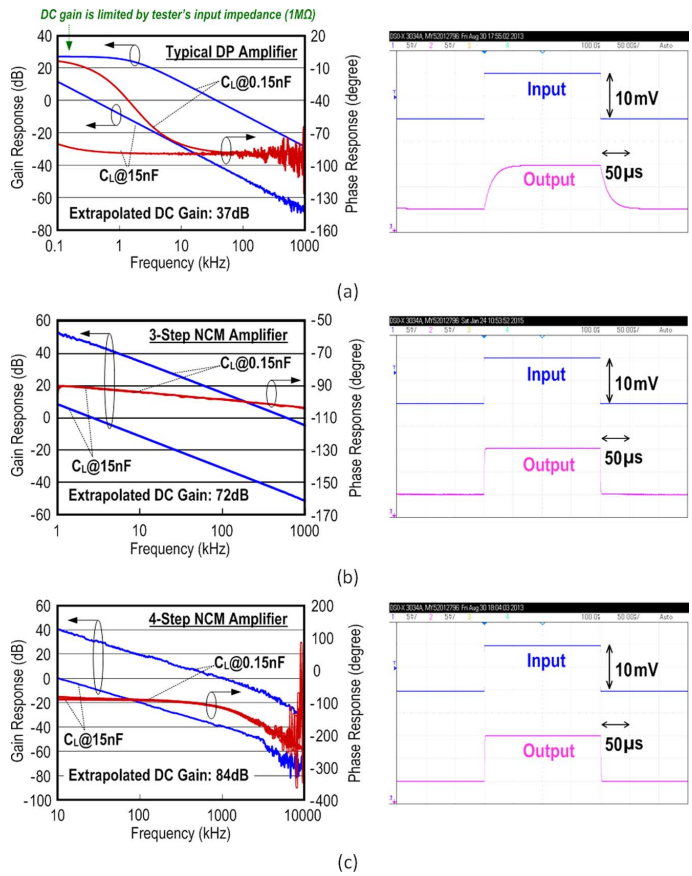


Fig. 13. Measured AC responses (at C_L = 0.15 and 15 nF) and small-step responses (at C_L = 0.15 nF): (a) DP amplifier; (b) 3-step NCM amplifier; (c) 4-step NCM amplifier.

in terms of DC gain. For the UGF, σ of the 3-step NCM is <10% of the mean, while for the 4-step NCM its σ is even > 1.2× of its mean. Moreover, roughly half of 300 runs achieve a UGF < 30 kHz. The PM of the 3-step NCM shows a small σ of 2.4°, but a very large spread for the 4-step NCM. For the offset voltage, the 3-step NCM has a small σ of 2 mV, but about 2 × larger offset spread for the 4-step NCM. It is obvious in Table III that the robustness factor α_{NCM3} is much smaller than α_{NCM4} consistent with the calculations, while validating the robustness of the 3-step NCM over the 4-step one.

V. EXPERIMENTAL RESULTS

The DP, 3-step and 4-step NCM amplifiers designed under the same power and area budgets were fabricated in 0.18 μm CMOS. Their die photos are shown in Fig. 12; all have a die size of 0.0013 mm^2. Their measured AC and small-step responses are plotted in Fig. 13. The 3-step NCM shows 0.0027–0.283 MHz UGF, linearly scalable with C_L from 15 down to 0.15 nF, which are > 7.5× to those of the DP (0.00038 to 0.037 MHz). The extrapolated DC gain (73 dB) of the 3-step NCM also compares favorably with that (43 dB) of the DP. Unlike those multi-stage designs [22]–[27] that have stringent stability limits on both small and large C_L sides, the stability of the NCM amplifiers are only bounded by the small-C_L side (i.e., 86.4° PM at 0.15 nF C_L for the 3-step NCM). The PM is still 82.4° when C_L is down to ∼ 0.075 nF that is the minimum C_L limited by the parasitics. In fact, the simulations indicate that the minimum C_L is 0.03 nF when targeting a PM of 65°. The 3-step NCM technique has a tradeoff on the

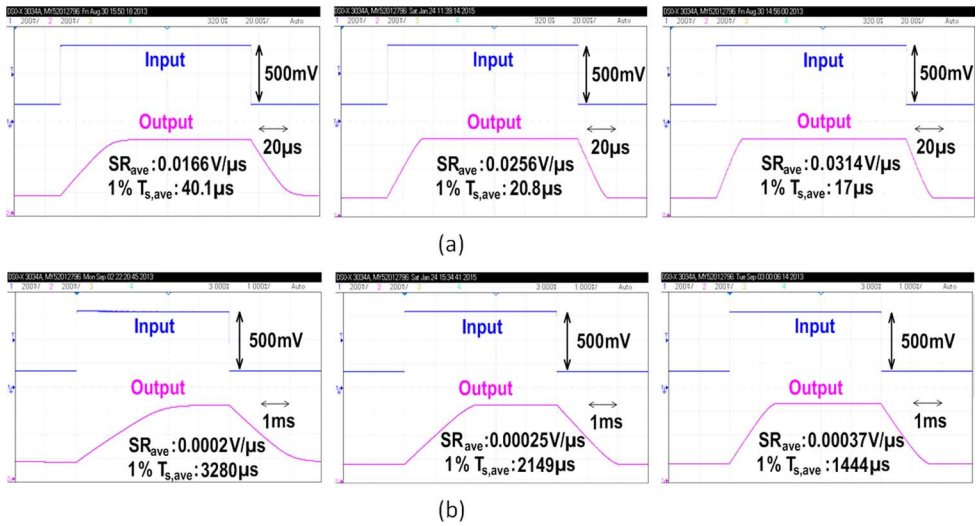


Fig. 14. Large-step responses of the DP (left), 3-step NCM (mid) and 4-step NCM (right) amplifiers at C_L: (a) 0.15 nF; (b) 15 nF.

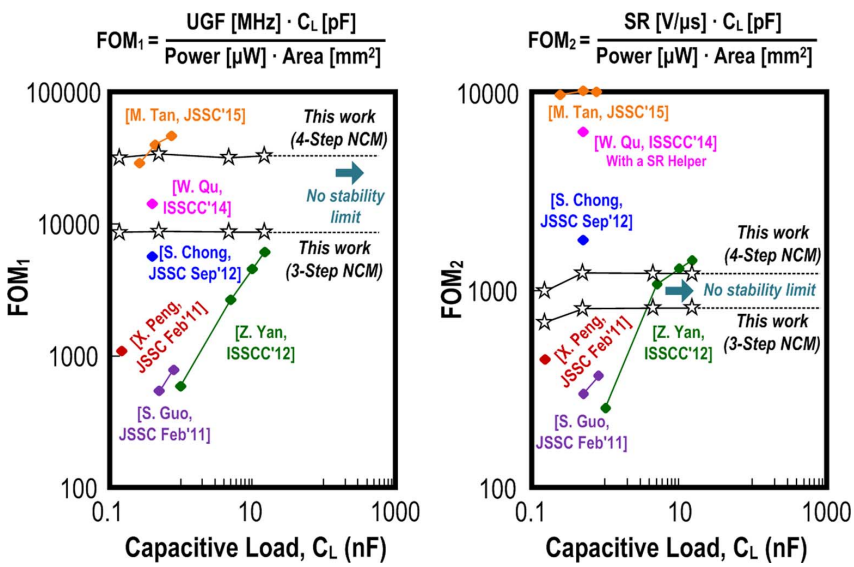


Fig. 15. Benchmark with the state-of-the-art three-stage amplifiers.

input-referred noise, 1.38× to 1.8× higher than the DP amplifier. The large-step responses are plotted in Fig. 14. At 0.15 and 15 nF C_L, the 3-step NCM amplifier improves constantly the average SR by $> 1.25\times$, and 1% settling time by $> 1.5\times$.

For the aggressive 4-step NCM design, Figs. 13 and 14 show that it could achieve further enhancement of both AC and transient performances over the DP amplifier (i.e., 84 dB DC gain, $>33\times$ larger UGF, 1.9× higher SR and 2.3 × 1% settling time reduction). Yet, the noise performance gets worse and the robustness degrades. In fact, only 9 out of 15 available samples measure similar performances as the theoretical prediction. On the contrary, all 15 samples of the 3-step NCM amplifier measure consistent improvements of those key metrics matched with the analysis (Section III-B). Particularly, the UGF exhibits a very small σ (0.0154 MHz) that is only 6% of the mean (0.275 MHz), and the σ of PM is only 1.31 ° for a mean of 86.1°. The performance summary is given in Table IV.

Unlike the multi-stage amplifiers, no bulky passives are entailed in our single-stage solutions. To allow a fair comparison with recent three-stage amplifiers [22]–[27], two figures-of-merit (FOMs) [5] that account for the impact of both power and area: $\mathrm{FOM}_1 = \mathrm{UGF} \cdot \mathrm{C_L}/(\mathrm{Power} \cdot \mathrm{Area})$ and $\mathrm{FOM}_2 = \mathrm{SR} \cdot \mathrm{C_L}/(\mathrm{Power} \cdot \mathrm{Area})$, are introduced. As summarized in Fig. 15, both the 3-step and 4-step NCM amplifiers achieve comparable FOM_1, and break the limit of large-C_L drivability. Before we apply any dynamic-biasing SR-enhancement technique [28], [29], the FOM_2 of the 4-step NCM amplifier is still 2.2 × higher than [22], but 1.2 ×, 1.47 ×, 5.8 × and 9.79 × lower than [24]–[27], respectively. [26] and [27] have better FOM_2 owing to the added SR helper and aggressively scaled compensation capacitors, respectively, whereas both have a limited C_L-drivability range. Detail comparison with the recently reported amplifiers is given in Table V.

TABLE V
PERFORMANCE COMPARISON OF THE 3-STEP NCM AND 4-STEP NCM AMPLIFIERS WITH RECENTLY REPORTED AMPLIFIERS

	[25] [Z. Yan, JSSC'13]		[26] [W. Qu, ISSCC'14]	[7] [K. H. Mak, TCAS-I'14]		[27] [M. Tan, JSSC'15]		Proposed 3-Step NCM Amplifier		Proposed 4-Step NCM Amplifier	
Load C_L (nF)	1	15	0.5	4.4	19	0.33	0.68	0.15	15	0.15	15
UGF (MHz)	1.37	0.95	1.34	1.08	0.289	4.21	3.37	0.283	0.0027	1.24	0.013
Phase Margin (°)	83.2	52.3	52.7	55.4	80.8	58	45	86.4	90.2	62.4	90.2
Gain Margin (dB)	9.8	18.1	--	17.7	36.3	--	--	31.5	>60	15.9	56.1
SR_{ave} (V/µs)	0.59	0.22	0.62	0.233	0.06	1.35	0.67	0.0256	0.00025	0.0314	0.00037
1% $T_{s,ave}$ (µs)	1.28	4.49	1.12	--	--	0.7	1.2	20.8	2149	17	1444
DC Gain (dB) (extrapolated)	>100		>100	>100		>100		72		84	
Input-Referred Noise (nV/√Hz)	172 @ 10kHz		--	--		--		430 @ 0.1kHz	110 @ 10kHz	1470 @ 0.1kHz	140 @ 10kHz
Power (µW) @ V_{DD} (V)	144 @ 2		6.3 @ 0.9	36.5 @ 1.8		12.7 @ 1.2		3.6 @ 1.2			
Chip Area (mm^2)	0.016		0.007	0.007		0.0032		0.0013			
CMOS Technology	0.35µm		0.18µm	0.18µm		0.13µm		0.18µm			
FOM_1 [(MHz·pF)/µW/mm^2]	595	6,185	15,119	18,599	21,491	34,186	56,388	9,071	8,654	39,744	41,667
FOM_2 [(V/µs·pF)/µW/mm^2]	256	1,432	7,030	4,013	4,462	1,0962	1,1211	821	801	1,006	1,186

VI. CONCLUSIONS

This paper introduced a NCM single-stage amplifier that has more design flexibilities (mirror steps and sub mirror ratios) to optimize the performance metrics (GBW, DC gain and SR), while preserving a rail-to-rail output swing, and wide C_L drivability without entailing any compensation capacitor or resistor. Both the performance limits and robustness of the NCM technique have been analytically explored, and the fabricated DP, 3-step and 4-step NCM amplifiers confirmed the theoretical study and performance claims.

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