Self-Reconfiguration Property of a Mixed Signal Controller for Improving Power Quality Compensation During Light Loading

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***Abstract*—This paper proposes a FPAA-FPGA/DSP-based mixed signal controller that achieves superior performance when compared with conventional digital controllers in power quality compensation. This includes adaptive signal conditioning and programmability on-the-fly, higher flexibility, parallel computation capability, and easy implementation. In practical applications, the power quality compensator may suffer from poor compensation performance, particularly during light loading. The adaptive signal gain and programmable on-the-fly functions of the mixed signal controller are intended to improve the system compensation performance, which cannot be achieved by using conventional digital controllers alone. In this study, an approximate total harmonic distortion (ATHD) is proposed to determine the total harmonic distortion value more quickly, reducing the evaluation time of the power quality compensation system performance. With hysteresis pulse width modulations, when the hysteresis error margin is designed, the ATHD can be determined instantaneously. Finally, representative simulation and experimental results of a three-phase four-wire center-split hybrid active power filter are presented. These verify the validity and effectiveness of the proposed mixed signal controller in improving current quality compensation performance during light load conditions, compared with a conventional digital controller.**

***Index Terms*—Converters, power conditioning, power quality, power system harmonics, reactive power.**

I. Introduction

In modern electric appliances, the loads are normally nonlinear, inductive, and unbalanced, which can cause power quality issues. These can increase transmission losses but are also harmful to electrical and electronic devices, affecting reliability, safety, and lifecycles. Power quality compensators have developed from capacitive banks, passive power filters (PPFs), and active power filters (APFs) into hybrid active power filters (HAPFs) to address these problems. Moreover, the development trend changes from static operations into dynamic responses, according to the change of system loading. Different control strategies have been proposed and developed; for example, from periodical root mean square (rms) values into instantaneous active and reactive power (pq) theories, from 2-D into 3-D pulse width modulations (PWMs), and from time-domain hysteresis controls into space-vector domain modulations. These algorithms have been proposed to improve the compensation performance of power quality compensators, by increasing response speed and reducing the total harmonic distortion (THD). The existing power quality compensators usually execute the compensation control algorithm using a digital controller. In this study, we propose to combine the control algorithm with the advantages of adaptive controller hardware supported by a mixed signal controller, to achieve better compensation performance. This cannot be achieved by using a digital controller alone. Currently, when compensator performance does not satisfy international standards, other PWMs can be selected, or the dc-link voltage can be increased. However, it may be the case that neither of these methods will improve compensator performance during light loading due to the low resolution of the input signals compared with the error signal and the PWM error margin. The design of digital controllers is usually based on a full loading situation. The full analog-to-digital conversion input signal range of a digital controller is, therefore, utilized to avoid analog signal saturation. In a light load situation, the digital controller may suffer from the problem of low resolution, which significantly affects its compensation performance. There is presently no achievable control strategy to deal with power quality compensation issues during light loading.

Table I summarizes the comparison and development timeline of traditional analog controllers, programmable logic controllers (PLC), microprocessors, digital signal processors (DSP), field programmable gate arrays (FPGA), and field programmable analog arrays (FPAA) [1]–[13]. The DSP/FPGA is shown to have superior performance with high computational ability and complexity, while FPAAs show remarkable improvements in

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TABLE I
COMPARISON OF DIFFERENT CONTROLLERS [1]–[13]

	Analog Controller	PLC	Micro processor	DSP	FPGA	FPAA
Development Timeline [1]–[6]	Before 1960s	1960s	1970s	1970s	1980s	1990s
Flexibility and Reconfiguration [7]–[10], [12], [13]	+	++	+++	++++	++++	++++
Computation Ability and Complexity [7]	+	++	+++	++++	+++	++
Parallelism [7]	+++	+	+	++	++++	++++
Quick and Easy Implementation [8], [9]	+	++	++	++	+++	++++
Programmability on-the-Fly [9], [11]	+	++	++	++	+++	++++
Bandwidth [7]	++++	+	++	+++	+++	++++
Accuracy [8], [9]	++++	+	++	+++	+++	++++
Electro-Magnetic Compatibility [8], [9]	+	++	+++	+++	+++	++++
High Speed	++++	+	++	+++	++++	++++
Low Power [9]–[11]	+	+	++	++	+++	++++

analog-related factors, such as better bandwidth, higher accuracy, on-the-fly programmability, and easier implementation. Recently, FPGAs have become more popular controllers than DSPs due to their parallelism properties and easy implementation [7]. However, the use of digital controllers alone is not sufficient to further improve system performance, such as the adaptive signal conditioning and on-the-fly programmability discussed here.

Based on the literature review, papers [14]–[18] are related to mixed signal controller researches. Girardey *et al.*, [14] focuses on control redundancy, with dynamic reconfiguration for system failure, and self-healing properties for safety concerns. In [15], the mixed signal controller combines three control loops: An analog nonlinear current loop, a digital linear voltage loop, and a digital frequency loop, to eliminate the sampling delay associated with conventional digital controllers and improve the transient response performance, whereas the fast nonlinear loop is built with simple analog hardware. In [16], the operation of the flyback-transformer-based buck converter is governed by a modified mixed signal controller, which provides minimum voltage deviation and seamless transitions between the modes. However, the mixed signal controllers in [15] and [16] do not address the advantages of using both analog and digital signal processing. In [17], a mixed-signal fixed frequency voltage-mode controller for dc–dc converters is proposed, where the derivative part of a proportional-integral-derivative (PID) regulator is maintained in the analog domain. Finally, the derivative action of the PID controller is inherently obtained by a combination of the analog front-end and the hard-wired digital logic, reducing sampling effects and control delays. This feature enables high dynamic performance, improving the bandwidth limitation of a conventional digital control solution. The development of alternative digital (or mixed signal) control architectures potentially enables simpler control architecture and faster dynamic response. In [18], a combined FPAA-FPGA/DSP platform is discussed, focusing on rapid prototyping and the need for stringent time-to-market constraints. In summary, the applications of the mixed signal controller at present are primarily for:

1) reducing the computation burden through a digital controller;
2) enhancing the parallelism property to increase the dynamic response; and
3) reducing the development time to market.

Several special features can be achieved by using a FPAA-FPGA/DSP mixed signal controller:

1) adaptive signal conditioning and programmability on-the-fly;
2) parallelism properties and higher redundancy;
3) higher accuracy, higher bandwidth, faster response time, and low power;
4) algorithm complexity and simplicity of implementation.

In this study, a FPAA-FPGA/DSP mixed signal controller for power quality compensation will be designed, and it is proposed that it will enhance compensator performance, which cannot be achieved by using either analog or digital controllers alone. This implies that the utilization of an integrated solution using both analog and digital controllers is advantageous. In Section II, the architecture of the proposed mixed signal controller will be presented. Based on this, certain characteristics of the mixed signal controller will be verified, using a three-phase four-wire HAPF system, in the subsequent sections. The main goal of this study is to apply the self-reconfiguration control strategy to improve compensator performance based on the benefits of the mixed signal controller and the proposed approximate THD (ATHD) index, in which the ATHD is deduced. This is discussed in Section III. The simulation and experimental verification of the improvements in the compensation performance of the proposed mixed controller application for a HAPF are presented in Section IV. The conclusions are given in Section V.

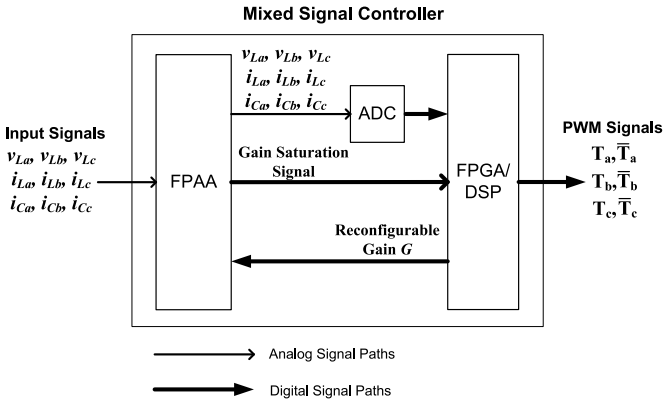

Fig. 1. Proposed mixed signal controller.

II. PROPOSED MIXED SIGNAL CONTROLLER ARCHITECTURE

To achieve the advantages of using analog and/or digital controllers, a mixed signal controller for power quality compensator is proposed in Fig. 1. The FPAA and FPGA are combined with an analog-to-digital converter (ADC), in which the input signals for the FPAA are analog signals from the power system

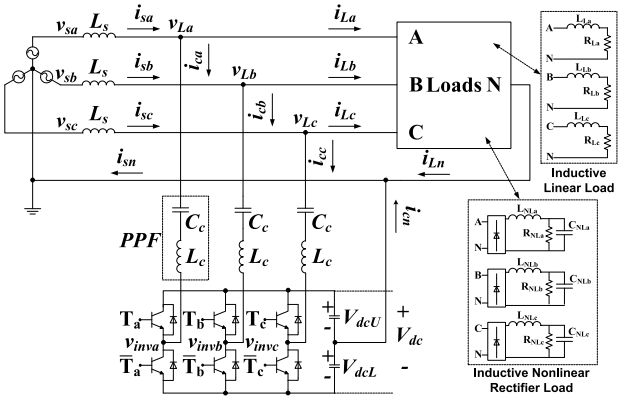

Fig. 2. Configuration of a three-phase four-wire HAPF.

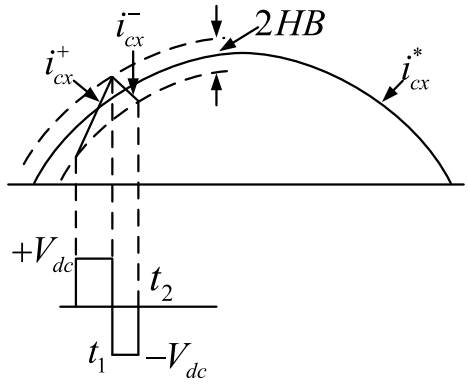

Fig. 3. Hysteresis PWM control method.

and the power quality compensator. The output digital signals of the FPGA/DSP are PWM trigger signals, which control the switching devices of the power quality compensator.

The FPAA can be operated as an adaptive signal conditioning unit that preconditions and filters, according to the optimization of system performance. The modified signals then pass to the digital unit for further processing, assisted by the ADC. The digital system, FPGA/DSP, can work with a "backer" subprogram to optimize the system operation by reconfiguring the control system automatically, or to carry out self-testing and self-repairing tasks. When it is necessary to reconfigure the analog part, the reprogramming data can be transferred directly through the digital path to the FPAA. Conversely, the FPAA can also send out control signals to the FPGA to modify the algorithm for protection, critical operations, etc. Finally, the mixed signal controller can send out digital signals for control purposes, as shown in Fig. 1.

The study focuses on the advantages of the mixed signal controller and highlights its superior performance for power quality compensation, compared with conventional digital controllers, in terms of its self-testing, self-repairing, and self-healing capabilities. The FPAA system used is the Anadigm third generation AN231E04 development board [19], and for the FPGA system, the Altera DE2-115 development board [20] is used. In the next section, an ATHD index for real-time performance evaluation is proposed and discussed. This evaluates whether the power quality compensation performance meets the requirement. If not, self-reconfiguration of the mixed signal controller will be carried out to improve system compensation performance.

III. Proposed ATHD Index for Real-Time Performance Evaluation and its Control

A three-phase four-wire HAPF (power quality compensator) system [21]–[23] is shown in Fig. 2. The subscript "x" denotes phases a, b, and c, n. v_{sx} is the system voltage, and i_{sx}, i_{Lx}, and i_{cx} are the system, load, and inverter currents for each phase, respectively. Based on this circuit, the self-reconfiguration control strategy for improving power quality compensator performance is illustrated as follows.

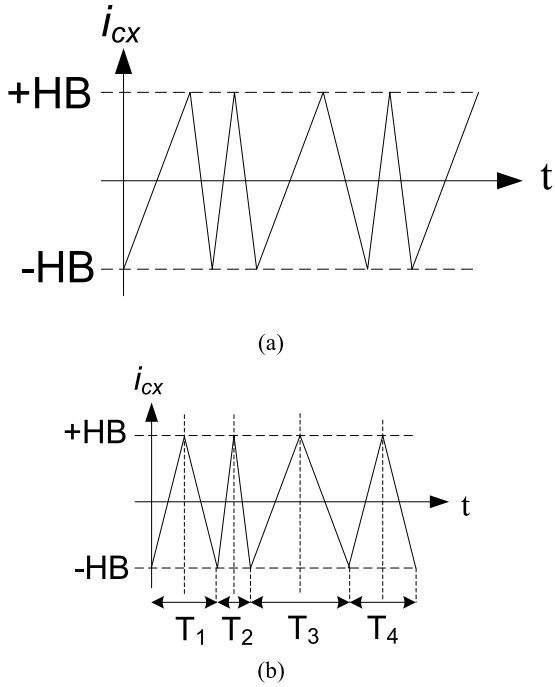

Fig. 4. Current error waveforms by hysteresis PWM: (a) Actual error waveform, (b) approximate error waveform.

A. ATHD Index

The THD of a signal is a measurement of the harmonic distortion, and is defined in (1) as the ratio of the sum of all harmonic components to the fundamental component. THD is used as an index to evaluate whether its power quality is acceptable or not. However, the fundamental frequency current and its related harmonic components are defined and computed under rms values. It takes at least a period cycle of time to sample data for computation; for example, a 50-Hz system needs 0.02 s. In this section, an ATHD index is proposed to have a fast determination of compensator performance, and to improve its performance during light loading, which cannot be implemented by a state-of-the-art digital controller alone

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1}. \tag{1}$$

TABLE II
THD AND ATHD WITH I_{1p} AND HB VARIATIONS, RESPECTIVELY, IN PU

HB (pu)		I_{1p} (pu)									
		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
0.1	THD (%)	82.39	41.95	27.14	20.25	16.08	14.10	11.48	10.08	8.99	8.170
	ATHD (%)	81.65	40.82	27.22	20.41	16.33	13.61	11.66	10.21	9.07	8.165
0.2	THD (%)	161.3	84.02	52.25	40.53	33.94	27.71	23.39	19.25	18.21	15.58
	ATHD (%)	163.3	81.65	54.43	40.82	32.66	27.22	23.33	20.41	18.14	16.33
0.3	THD (%)	220.8	126.8	87.51	60.48	46.32	39.50	36.43	30.90	27.32	23.35
	ATHD (%)	244.9	122.5	81.65	61.24	48.99	40.82	34.99	30.62	27.22	24.49
0.4	THD (%)	324.6	162.7	120.0	85.70	64.13	52.56	46.87	39.87	34.85	33.24
	ATHD (%)	326.6	163.3	108.9	81.65	65.32	54.43	46.66	40.82	36.29	32.66
0.5	THD (%)	416.4	221.5	119.4	103.5	79.23	69.22	60.97	50.14	42.63	40.59
	ATHD (%)	408.2	204.1	136.1	102.1	81.65	68.04	58.32	51.03	45.36	40.82
0.6	THD (%)	550.6	250.0	166.3	124.3	91.52	81.49	67.66	59.36	53.84	48.67
	ATHD (%)	489.9	244.9	163.3	122.5	97.98	81.65	69.99	61.24	54.43	48.99
0.7	THD (%)	561.8	276.2	203.8	124.8	119.4	105.1	80.54	67.53	62.84	57.06
	ATHD (%)	571.5	285.8	190.5	142.9	114.3	95.26	81.65	71.44	63.51	57.15
0.8	THD (%)	664.9	320.5	231.4	167.0	135.7	110.8	92.66	82.21	70.87	63.86
	ATHD (%)	653.2	326.6	217.7	163.3	130.6	108.9	93.31	81.65	72.58	65.32
0.9	THD (%)	775.4	375.7	259.4	166.6	155.6	117.3	114.2	92.36	80.30	71.26
	ATHD (%)	734.8	367.4	244.9	183.7	147.0	122.5	105.0	91.86	81.65	73.48
1.0	THD (%)	801.9	361.2	268.5	201.7	167.8	147.7	114.3	107.3	93.43	84.48
	ATHD (%)	816.5	408.2	272.2	204.1	163.3	136.1	116.6	102.1	90.72	81.65

TABLE III
ABSOLUTE% ERROR OF ATHD

HB (pu)	Average Δ_{ATHD}	I_{1p} (pu)									
		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
0.1	Δ_{ATHD} (%)	0.90	2.69	0.29	0.79	1.55	3.48	1.57	1.29	0.89	0.06
0.2	Δ_{ATHD} (%)	1.24	2.82	4.17	0.72	3.77	1.77	0.26	6.03	0.38	4.81
0.3	Δ_{ATHD} (%)	10.91	3.39	6.70	1.26	5.76	3.34	3.95	0.91	0.37	4.88
0.4	Δ_{ATHD} (%)	0.62	0.37	9.25	4.73	1.86	3.56	0.45	2.38	4.13	1.74
0.5	Δ_{ATHD} (%)	1.97	7.86	13.99	1.35	3.05	1.70	4.35	1.78	6.40	0.57
0.6	Δ_{ATHD} (%)	11.02	2.04	1.80	1.45	7.06	0.20	3.44	3.17	1.10	0.66
0.7	Δ_{ATHD} (%)	1.73	3.48	6.53	14.50	4.27	9.36	1.38	5.79	1.07	0.16
0.8	Δ_{ATHD} (%)	1.76	1.90	5.92	2.22	3.76	1.71	0.70	0.68	2.41	2.29
0.9	Δ_{ATHD} (%)	5.24	2.21	5.59	10.26	5.53	4.43	8.06	0.54	1.68	3.12
1.0	Δ_{ATHD} (%)	1.82	13.01	1.38	1.19	2.68	7.85	2.01	4.85	2.90	3.35

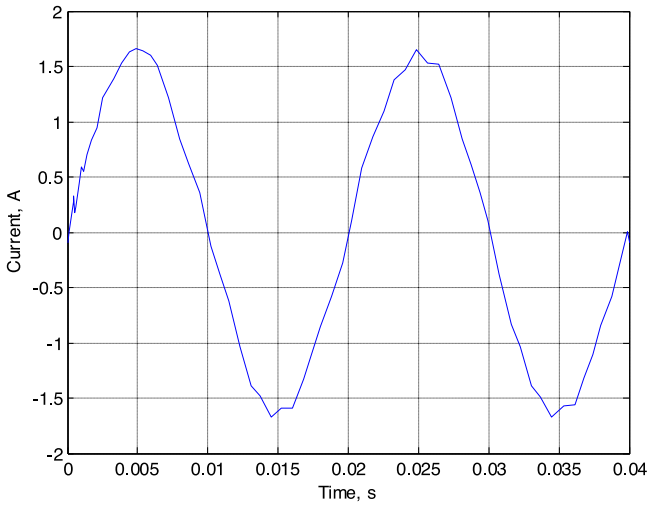

Fig. 5. Simulated current waveform when $I_{1p} = 1.6$ A, HB $= 0.1$ A, THD $= 4.92\%$, ATHD $= 5.1\%$, $|\Delta_{\mathrm{ATHD}}| = 3.72\%$.

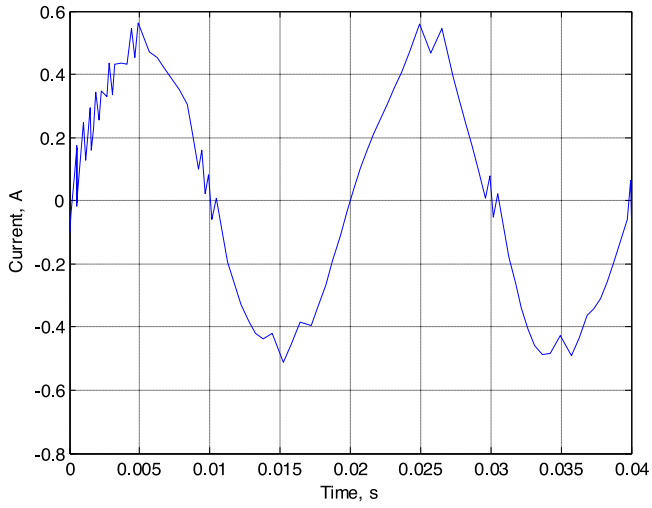

Fig. 6. Simulated current waveform when $I_{1p} = 0.5$ A, HB $= 0.1$ A, THD $= 16.08\%$, ATHD $= 16.33\%$, $|\Delta_{\mathrm{ATHD}}| = 1.55\%$.

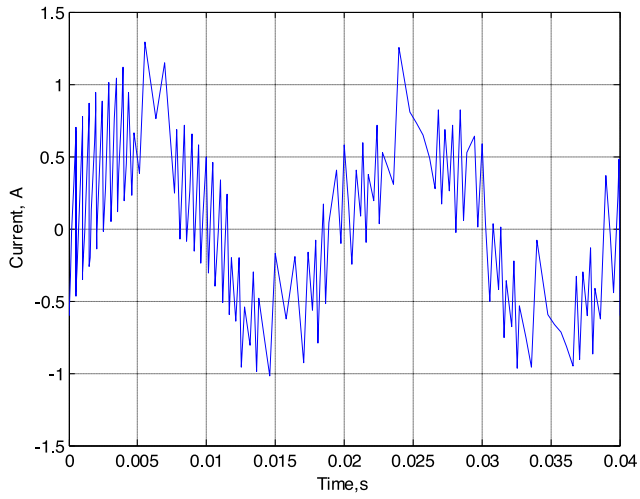

Fig. 7. Simulated current waveform when $I_{1p} = 0.7$ A, HB $= 0.6$ A, THD $= 67.56\%$, ATHD $= 69.99\%$, $|\Delta_{\mathrm{ATHD}}| = 3.44\%$.

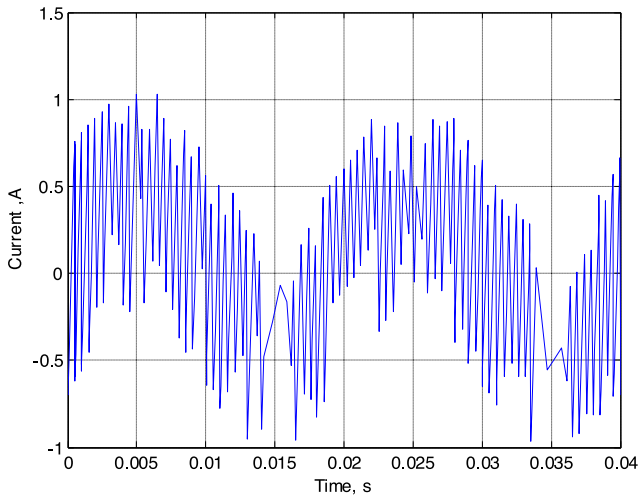

Fig. 8. Simulated current waveform when $I_{1p} = 0.4$ A, HB $= 0.7$ A, THD $= 124.8\%$, ATHD $= 142.9\%$, $|\Delta_{\mathrm{ATHD}}| = 14.5\%$.

Fig. 3 shows the hysteresis current control of a voltage source PWM inverter [24], in which the sinusoidal reference current i_{cx}^{*} is compared with the actual current, i_{cx}. When the actual current is greater (less) than the reference current by a hysteresis band (HB) value, the inverter leg is switched ON or OFF accordingly. Therefore, the HB specifies the maximum current ripple.

By superposition, the actual current can be decomposed into a sinusoidal current and an irregular triangular current waveform. An irregular triangular waveform is given in Fig. 4(a), in which the rate of change of current at any moment should be different, due to its different voltage amplitude at different times. Therefore, the triangular waveforms are actually not symmetrical.

Referring to (1), the ratio of the sum of all harmonic current components to the fundamental current component can be considered as the ratio of the rms value of the irregular triangular waveform, as shown in Fig. 4(a), to the fundamental sinusoidal waveform. However, by taking an approximation, the regular

TABLE IV
SIMULATED AND EXPERIMENTAL PARAMETERS FOR THE HAPF SYSTEM

System parameters	Physical values	
Source	V_{Lx}, L_s	110 V, 1 mH
Passive part	L_c, C_c	10 mH, 40 μF
	20% Testing Load	
Nonlinear rectifier load (Inductor, resistor, capacitor)	$L_{NLx}, R_{NLx}, C_{NLx}$	35 mH, 169 Ω, 373 uF
	50% Testing Load	
Nonlinear rectifier load (Inductor, resistor, capacitor)	$L_{NLx}, R_{NLx}, C_{NLx}$	35 mH, 55 Ω, 373 uF
	70% Testing Load	
Nonlinear rectifier load (Inductor, resistor, capacitor)	$L_{NLx}, R_{NLx}, C_{NLx}$	35 mH, 55 Ω, 373 uF
Linear load (Inductor, resistor)	L_{Lx}, R_{Lx}	0 mH, 100 Ω
	90% Testing Load	
Nonlinear rectifier load (Inductor, resistor, capacitor)	$L_{NLx}, R_{NLx}, C_{NLx}$	35 mH, 55 Ω, 373 uF
Linear load (Inductor, resistor)	L_{Lx}, R_{Lx}	0 mH, 50 Ω

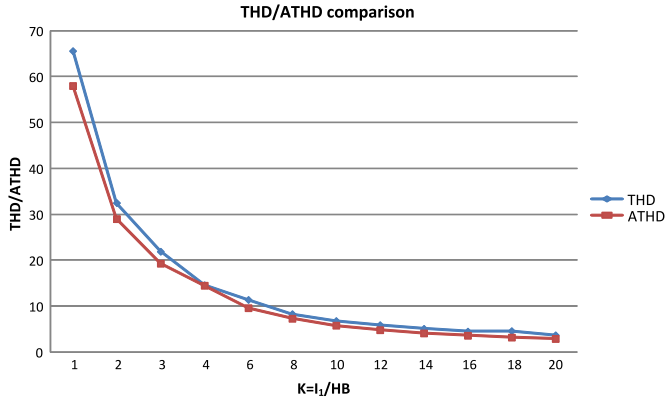

Fig. 9. THD versus ATHD.

triangular waveform, as shown in Fig. 4(b), is chosen instead of the irregular one. Fig. 4(b) shows that each period of the triangular waveform is different. Correspondingly, the rms value of a regular triangular waveform is given in (2). The rms value is shown to be independent of the period of the triangular waveform. Finally, the proposed ATHD index can be defined as (3)

$$I_h = \sqrt{\frac{1}{T}\int_0^T \left[\frac{8\cdot \mathrm{HB}}{\pi^2}\sum_{n=1}^{\infty}\left(\frac{1}{n}\cos n\omega t\right)\right]^2 dt} = \frac{\mathrm{HB}}{\sqrt{3}} \tag{2}$$

$$\mathrm{ATHD} = \frac{\mathrm{HB}}{\sqrt{3}I_1}. \tag{3}$$

According to the instantaneous power theory [25], the instantaneous fundamental active current peak value can be calculated by (4). It should be noted that (4) can be used when the three-phase voltage source is balanced and sinusoidal. However, unbalanced and nonsinusoidal voltage is out of this study's scope. More detail concerning the required compensation current under unbalanced and nonsinusoidal voltage can be computed by the method given in [28]. The ATHD is calculated during compensation, and as a result the fundamental reactive component

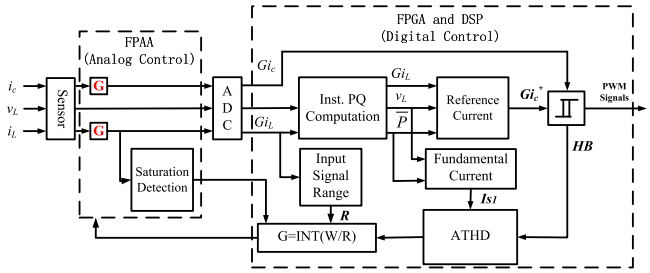

Fig. 10. Control block diagram for proposed mixed signal controller.

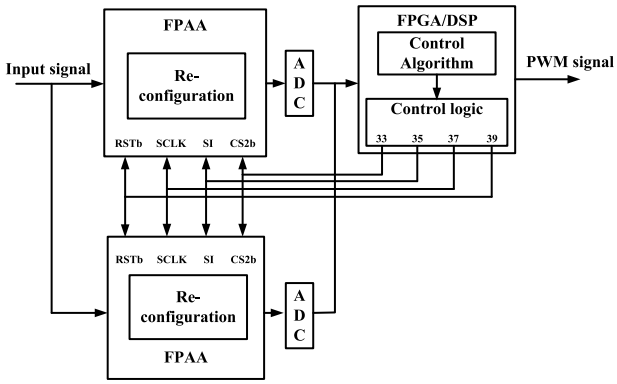

Fig. 11. Configuration connections between FPAAs and FPGA/DSP.

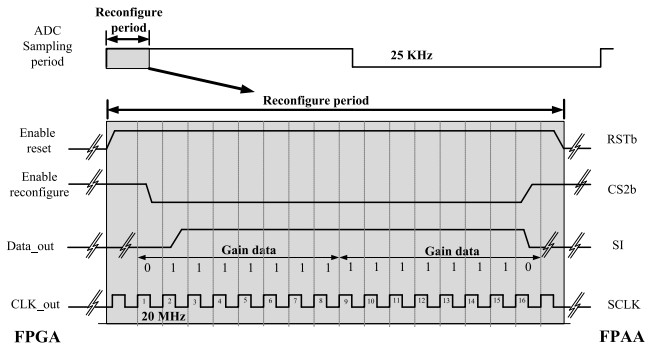

Fig. 12. Gain = 2, data streams between FPGA and FPAA.

is not considered in computing the ATHD value. The calculated ATHD would otherwise be smaller when the fundamental reactive current is included. In (3), I_1 is an rms value that has $\sqrt{2}$ difference with its peak value (I_{1p}), which can be calculated instantaneously, using the instantaneous power theory [25]

$$I_{1p} = \frac{\sqrt{2} \cdot \bar{p}}{\sqrt{3}\,\|\Delta\|} \tag{4}$$

where $\|\Delta\| = \sqrt{v_a^2 + v_b^2 + v_c^2}$ and

$$\bar{p} = \frac{1}{T}\int_0^T \vec{v} \cdot \vec{i} dt = \frac{1}{T}\int_0^T (v_a \cdot i_a + v_b \cdot i_b + v_c \cdot i_c) dt.$$

Then, finally

$$\text{ATHD} = \sqrt{\frac{2}{3}}\frac{\text{HB}}{I_{1p}}. \tag{5}$$

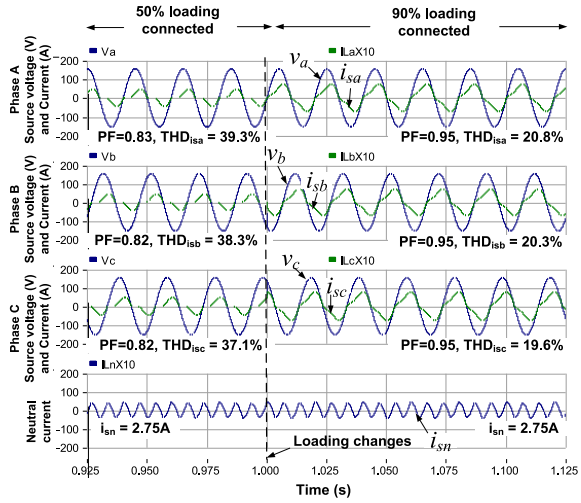

Fig. 13. Simulated system voltage and current before compensation.

ATHD is defined as (5), a fast evaluation index of compensation performance instead of THD, in which the HB of the ATHD can be determined according to hysteresis PWM, or the compensation error of space vector modulation.

B. THD and ATHD

A comparison between THD and ATHD is performed under two categories: With and without switching power quality compensations. The ATHD is an approximated method to evaluate the power quality compensator's performance during compensation. When there is no switching power quality compensator, the ATHD cannot be used to reflect the THD as there is no HB or error margin value for the ATHD computation. Here, capacitor banks and PPFs can perform steady compensation, with conventional THD as the performance evaluation index. The ATHD cannot be used under these circumstances.

When switching power quality compensators such as APFs and HAPFs are used, the proposed ATHD can be used to evaluate the power quality compensation performance. When the HB or error margin at a particular instant can be determined, the ATHD can be calculated using the instantaneous power theory [25].

Table II shows the simulated THD and ATHD values with respect to the different fundamental current peak I_{1p}, in per unit (pu), and HB in pu at sampling $\text{frequency} = 5$ KHz, and system $\text{frequency} = 50$ Hz. For example, when $I_{1p} = 0.5$ and $\text{HB} = 0.1$, its simulated THD is 16.08% and its ATHD is 16.33%.

Table III shows the simulated absolute percentage error of ATHD compared with THD through (6). However, the ATHD index is estimated to evaluate the compensation performance instantaneously. The absolute percentage error range of ATHD is shown to be from 0.06% to 14.5%, and its average percentage error is 3.44%.

Taking the IEEE Standard [27] with total demand distortion (TDD) for light rated loading ($I_{SC}/I_L > 1000$), and the Hong Kong Power Quality Standard [29] into consideration, at worst case, the nominal rate current is assumed to be equal to the fundamental load current with the result that $\text{THD} = \text{TDD}$.

TABLE V
EXPERIMENTAL RESULTS OF USING CONVENTIONAL AND PROPOSED CONTROLLERS

Different cases		Before compensation			After compensation					
					Conventional controller			Proposed controller		
		i_{sx} (A)	PF	THD_{isx} (%)	i_{sx} (A)	PF	THD_{isx} (%)	i_{sx} (A)	PF	THD_{isx} (%)
20% load	A	1.09	0.81	52.5	1.38	0.91	20.7	1.33	0.94	13.9
	B	1.08	0.81	51.9	1.46	0.93	21.1	1.38	0.94	15.8
	C	1.07	0.81	53.3	1.50	0.90	22.1	1.38	0.93	15.0
50% load	A	2.51	0.80	35.6	2.18	0.98	17.6	2.09	0.99	10.8
	B	2.47	0.80	35.5	2.16	0.98	17.1	2.13	0.99	11.9
	C	2.51	0.80	34.4	2.18	0.98	18.7	2.11	0.99	10.5
70% load	A	3.59	0.90	23.7	3.26	1.0	6.3	3.25	1.0	5.7
	B	3.49	0.90	23.7	3.30	0.99	7.7	3.28	1.0	6.1
	C	3.42	0.90	24.4	3.28	0.99	7.5	3.27	0.99	6.4
90% load	A	4.55	0.95	17.6	4.47	1.0	5.9	4.39	1.0	5.6
	B	4.47	0.95	17.4	4.41	1.0	7.1	4.39	1.0	6.7
	C	4.64	0.95	16.6	4.57	1.0	7.8	4.50	1.0	7.5

This study, therefore, focuses on a THD close to or below 20%. In Tables II and III, THD values which are close to or below 20% are highlighted underline. The average percentage error of ATHD within 20% THD is 2.089%.

To keep within the safety margin, it is suggested that an ATHD at 16% is chosen when THD at 20% is the compensation target to include this average percentage error of ATHD. However, the simulated results are estimated values and it should be noted that the values will be different in other circumstances

$$|\Delta_{\mathrm{ATHD}}| = \left|\frac{\mathrm{THD} - \mathrm{ATHD}}{\mathrm{THD}}\right| \times 100\%. \tag{6}$$

Several simulated current waveforms are given in Figs. 5, 6, 7, and 8 at THD = 5%, 16%, 68%, and 124%, respectively. Fig. 5 shows the waveform at THD ≈ 5% with $|\Delta_{\mathrm{ATHD}}| = 3.72\%$ corresponding to $I_{1p} = 1.6$ A and HB = 0.1 A. Fig. 6 shows the waveform at THD ≈ 16% with $|\Delta_{\mathrm{ATHD}}| = 1.55\%$ corresponding to $I_{1p} = 0.5$ A and HB = 0.1 A. Fig. 7 shows the waveform at THD ≈ 68% with average $|\Delta_{\mathrm{ATHD}}| = 3.44\%$ corresponding to $I_{1p} = 0.7$ A and HB = 0.6 A. Fig. 8 shows the waveform at THD ≈ 124% with the largest $|\Delta_{\mathrm{ATHD}}| = 14.5\%$ corresponding to $I_{1p} = 0.4$ A and HB = 0.7 A.

At THD ≈ 16%, based on Table II, the hysteresis error band HB should be set as one-fifth of the fundamental amplitude. Furthermore, a parameter $K = I_1/\mathrm{HB}$ is defined as a ratio of the fundamental rms current amplitude to the hysteresis error band value. When *K* is increased, the compensated current ripple relatively decreases. Taking the system parameters listed in Table IV under 50% loading compensation, Fig. 9 shows the simulated THD and calculated ATHD with respect to different *K*, and the difference between them is seen to be small. The THD standard of 20% is selected, as discussed, while the ATHD of 16% for the percentage error and safety margin considerations is selected. Fig. 9 shows that *K* is near to 3.8 at ATHD ≈ 16%. In Table II, this is the case with $I_{1p} = 0.5$ A, HB = 0.1 A, THD = 16.08%, in which I_{1p} is the fundamental current peak value. This means that the HB value or error margin of the hysteresis PWM control should not be less than 0.26 times the fundamental rms current amplitude. Otherwise, no matter how fast the power electronics switching device, the compensation performance of the power quality compensator will not be acceptable.

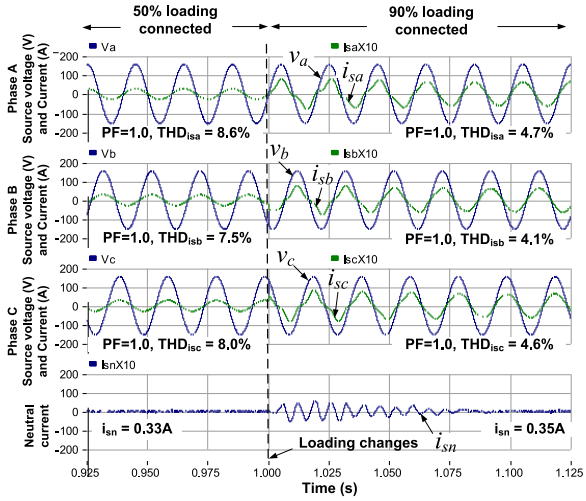

Fig. 14. Simulated system voltage and current after HAPF compensation.

An ATHD can be used to estimate the power quality compensation system performance, rapidly determining the THD value. The advantages of using an ATHD over THD are as follows:

1) It can simplify the computation without computation of the frequency spectrum.
2) The ATHD value can be obtained in real time.
3) Hardware implementation of ATHD can be easily obtained.

The ATHD is, however, an approximated performance index, unlike THD. It can only be calculated when the HB or error margin at a certain instant can be determined. An ATHD is suitable to be used with APFs and HAPFs for power quality compensation. Nevertheless, the dc-link voltage of the power quality compensators should be sufficient to successfully perform compensation [21], [22].

C. Self-Reconfiguration Control Strategy for Improving Power Quality Compensator Performance

In a traditional power quality compensating system, the system rating design is usually based on the defined nominal values

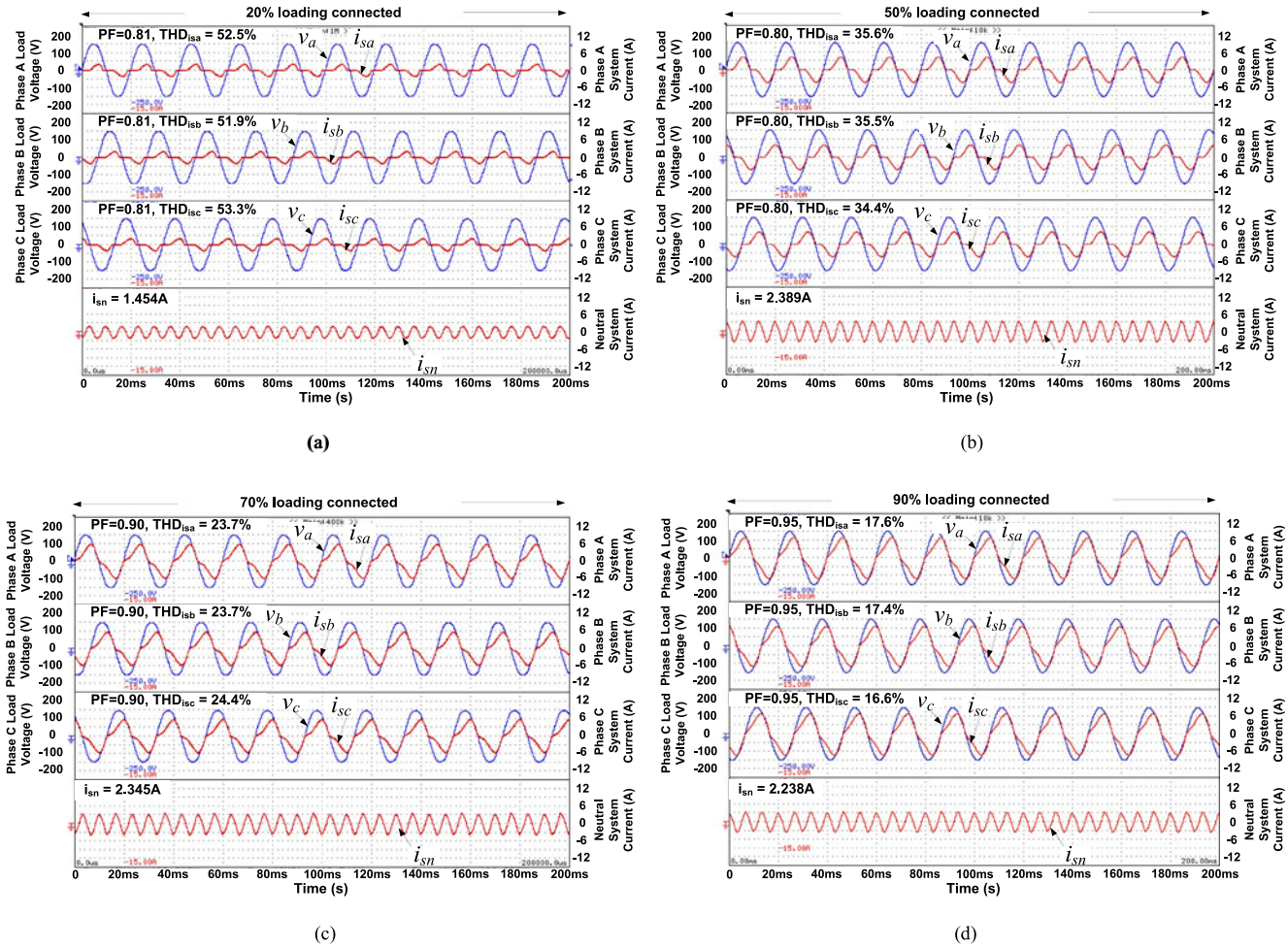

Fig. 15. Three-phase experimental system currents before compensation during: (a) 20% loading, (b) 50% loading, (c) 70% loading, and (d) 90% loading.

(full loading consideration). In practical operations, the system loading varies over time. The loading may be full or light. During a full loading situation, the system performance can be guaranteed, due to the nominal design. However, during a light loading situation, the power quality compensator performance cannot usually reach the standard requirement [27], [29]. The mixed signal controller proposed in this study has self-reconfiguration capabilities, which cannot be achieved using only a digital controller. The self-reconfiguration control strategy for improving power quality compensator performance is given as follows.

Using a simplified three-phase instantaneous pq theory [26], the reference compensating current for a HAPF shown in Fig. 2 can be determined by

$$i_{cx}^{*} = \left(i_{La} - \frac{\bar{p}}{v^2} v_{La}\right)\overrightarrow{n_a} + \left(i_{Lb} - \frac{\bar{p}}{v^2} v_{Lb}\right)\overrightarrow{n_b} + \left(i_{Lc} - \frac{\bar{p}}{v^2} v_{Lc}\right)\overrightarrow{n_c} \tag{7}$$

where $\{\overrightarrow{n_a}, \overrightarrow{n_b}, \overrightarrow{n_c}\}$ is the space basis in the a-b-c coordinate, $p = v_{La}i_{La} + v_{Lb}i_{Lb} + v_{Lc}i_{Lc}$, and $\bar{p}$ is the average value of instantaneous power p.

From Fig. 2, the actual i_{cx} should be the same as its reference i_{cx}^{*}, ($i_{cx}^{*} = i_{cx}$) under perfect compensation. The source current, composed of load and compensator currents, is defined by (8). By hysteresis PWM, the current error should be within the HB. As a result, (8) can be rewritten as (9)

$$i_{sx} = i_{Lx} + i_{cx}^{*} \equiv i_{sx1} \tag{8}$$

$$i_{sx1} \cong i_{Lx} + i_{cx} + \mathrm{HB}. \tag{9}$$

Considering the digital control system, the resolution of HB is limited by the available bits (B) of the ADC, and the amplitude width (W) of the input signal. The minimum HB value can be given as

$$\mathrm{HB}_{\min} = \frac{W}{2^{B+1}}. \tag{10}$$

This minimum HB cannot be further reduced due to the hardware limitations of the controller; this implies that the digital controller compensation performance may not be acceptable during a light load condition, particularly when the ATHD or the THD is around 16% and K ≈ 3.8, as shown in Fig. 9. From (9) and (11), when the amplitude of HB is relatively near to the amplitude of i_{Lx} and i_{cx}, the compensation performance is not acceptable. This is because the $\mathrm{HB}_{\min}$ cannot be further reduced, and a parameter gain G is attached to K. Finally, as G is an amplification gain, the K value can move to a larger value.

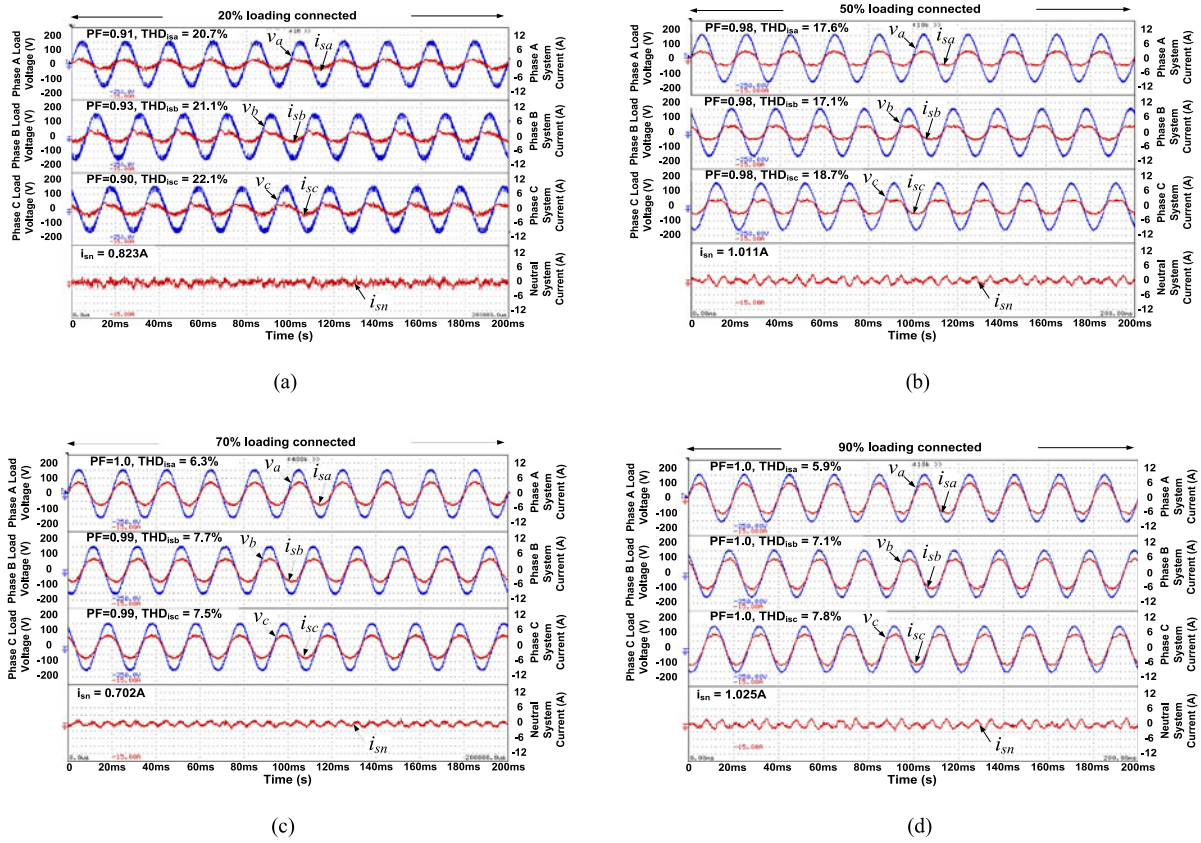

Fig. 16. Compensated three-phase experimental system currents by using the conventional digital controller during: (a) 20% loading, (b) 50% loading, (c) 70% loading, and (d) 90% loading.

The THD and the ATHD can, therefore, be improved

$$K = G \cdot \frac{i_{sx1}}{\mathrm{HB}} \cong G \cdot \left(1 + \frac{i_{Lx} + i_{cx}}{\mathrm{HB}}\right). \tag{11}$$

Fig. 10 shows a control block diagram for the proposed mixed signal controller. The gain G can be adjusted according to (12), where INT is an integer function that takes out all the fraction parts, W is the measured width (range) of the ADC, and R is the peak-to-peak input signal range for a given period, such as 1 min or several hours, to avoid system fluctuation during operations. The G is calculated by a digital controller such as DSP or FPGA, and then sent to FPAA for gain modification. During light loading, G can be an integer number larger than 1. To avoid analog signal saturation, a saturation detection function can be implemented in FPAA. $G = 1$ when saturation occurs

$$G = \mathrm{INT}\left(\frac{W}{R}\right). \tag{12}$$

Finally, the compensation error can be limited by (13)

$$\Delta i_{\mathrm{error}} = \mathrm{HB}_{\min} = G \cdot i_{cx}^{*} - G \cdot i_{cx}. \tag{13}$$

When the ATHD $\approx$ 16% and $G = 1$, $K \approx 3.8$. According to (11) and Fig. 9, when the ATHD $\approx$ 20%, $G = 2$, K is approximately 6. The ATHD and the THD can then be lowered to around 10%. The gain G can be seen to improve the compensation performance under the hysteresis PWM, without changing the coupling inductance and capacitance.

D. System Implementation and Communication

Fig. 11 shows the system implementation based on FPAAs and FPGA/DSP. FPGA/DSP is used for the digital parts and FPAA for the analog parts.

The basic idea of the self-reconfiguration characteristic is that a FPGA-based high-speed control logic block and a FPAA-based analog module are used to adjust the gain automatically and rapidly. Two FPAAs and one FPGA are used in the implementation. The FPAAs are under the control of the FPGA, and the inherent reconfigurable properties of FPAAs allow the analog modules to be dynamically reconfigured through a serial interface. In the system initialization, voltage and current signals are detected and amplified by the FPAA, digitized through an ADC, and fed into the FPGA for further processing. The gain of the gain limiter is controlled by the FPGA. The output voltage limit is 3 V, which is the maximum input voltage for the ADC. If the input signal amplified by the gain is saturated, the FPGA will reset the gain G to 1. Through various computations and comparisons, the corresponding gain value G for the FPGA will be obtained.

The configuration clock of FPAA and FPGA is 20 MHz. In the configuration process, shown in Fig. 12, every gain value needs 11 bytes of control logic data, defined by the configuration

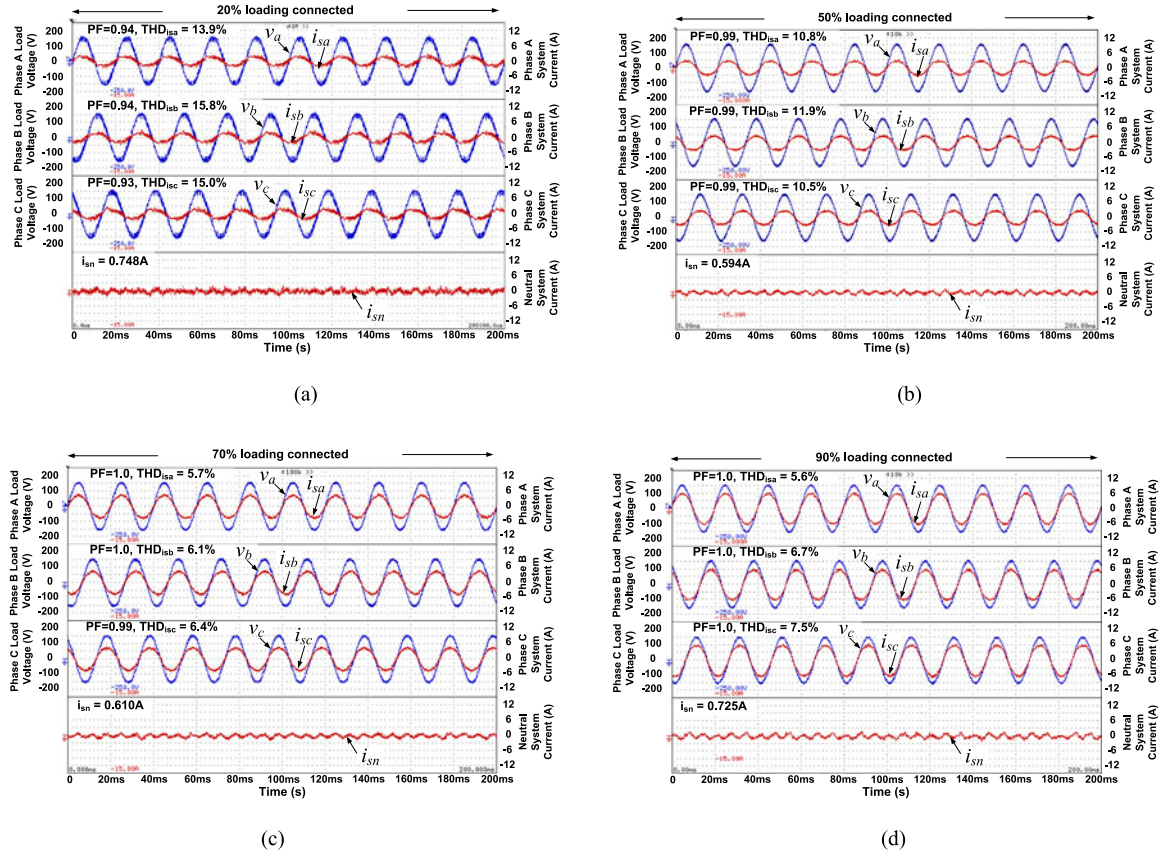

Fig. 17. Compensated three-phase experimental system currents by using the proposed mixed signal controller during: (a) 20% loading, (b) 50% loading, (c) 70% loading, and (d) 90% loading.

protocol in the FPAA. Each byte has one 8-bit address, which in total needs t_1 (s) to completely transmit. The AD sampling frequency of the whole controller is 25 kHz, so the controller outputs obtained in this period is 1/25 kHz (40 μs). In total, the control loop, including the AD conversion, pq theory, PWM techniques, and feedback loop, can be completed in one ADC sample period. Moreover, t_1, as given in (14), is much smaller than one ADC sampling cycle, which means the compensation control algorithm will not be affected by the on-the-fly FPAA reconfiguration

$$t_1 = 11 \times 8 \times \frac{1}{20 \times 10^6} = 4.4 \times 10^{-6} s \ll \frac{1}{25 \times 10^3} = 4 \times 10^{-5} \text{s}. \quad (14)$$

IV. Simulation and Experimental Results

In this section, the proposed mixed signal controller, for improving power quality compensator performance, will be verified by simulation and experiments. This is compared with a conventional digital controller, in which a three-phase four-wire HAPF system, shown in Fig. 2, is chosen as the testing power quality compensator. Table IV lists the simulated and experimental system parameters for the HAPF with different loadings. Table V summarizes the power quality parameters for different testing loads before compensation.

To show the advantage of the proposed mixed signal controller, four sets of loading parameters are chosen. To ensure the focus is on the ATHD and the mixed signal controller strategy, the simulated and experimental three-phase loadings are approximately balanced, shown in Fig. 2.

Simulation studies were carried out using PSCAD/EMTDC. Fig. 13 shows the simulated system voltages and currents before compensation. When 50% loading is connected, the three-phase simulated $\text{THD}_{i_{sx}}$ of system current are 39.3%, 38.3%, and 37.1%, with power factors $(\text{PF}) = 0.83$, 0.82, and 0.82, respectively. When 90% loading is connected (loading compensation, by applying the conventional digital changes), the three-phase simulated $\text{THD}_{i_{sx}}$ are 20.8%, 20.3%, and 19.6%, with PF = 0.95, 0.95, and 0.95, respectively. Before compensation, the simulated $\text{THD}_{i_{sx}}$ cannot satisfy the $\text{THD}_{i_{sx}} < 20\%$ requirement during both 50% and 90% loading conditions.

Fig. 14 shows the simulated system voltages and currents after HAPF compensation. After compensation, the simulated $\text{THD}_{i_{sx}}$ satisfies the $\text{THD}_{i_{sx}} < 20\%$ requirement during both 50% and 90% loading conditions. Moreover, the PF are improved to unity. In the PSCAD simulation, the signal resolution is infinite, as there is no AD conversion process, and the simulation process is not affected by EMI noise. Therefore, the HAPF compensation performance is satisfactory no matter whether the loading is light or full.

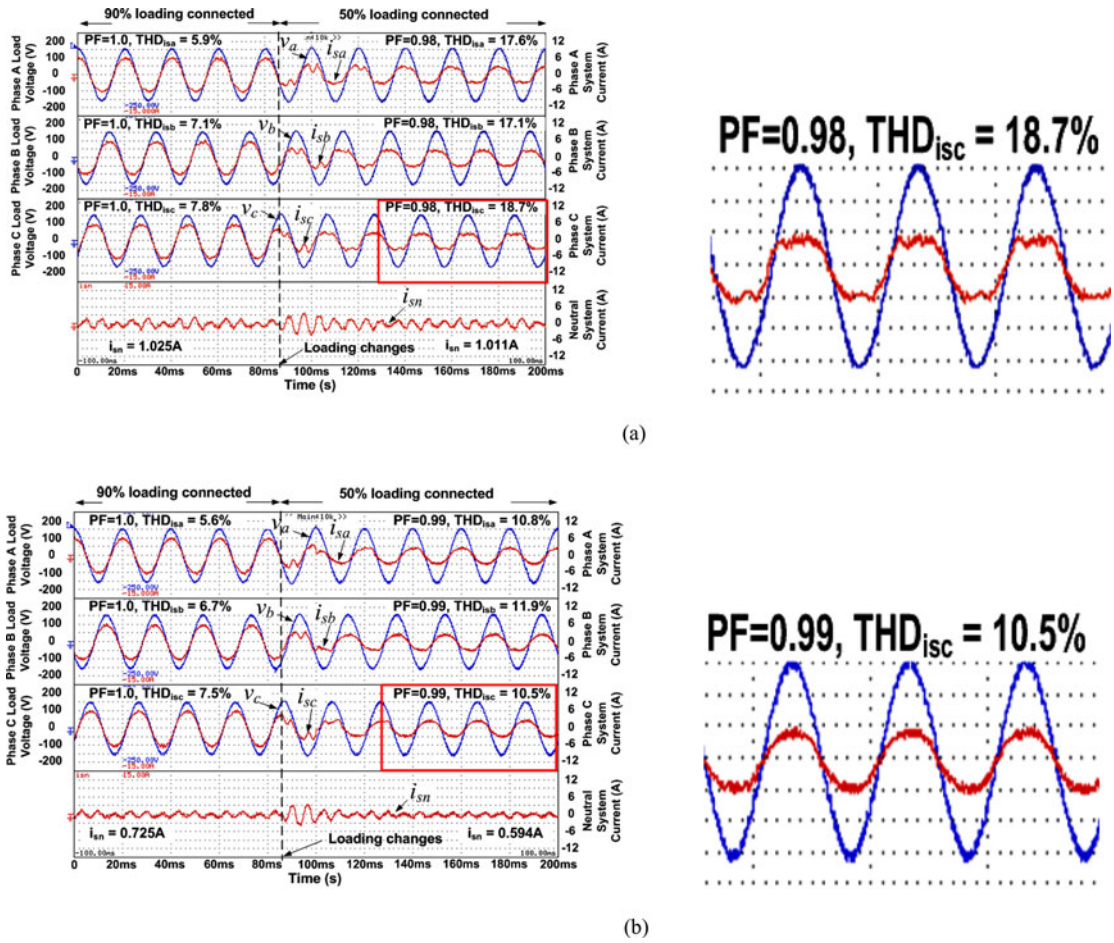

Fig. 18. Dynamic compensation performance during loading changes by using: (a) Conventional digital controller and (b) proposed mixed signal controller.

However, for the hardware experimental case, the signal resolution will greatly affect the HAPF compensation performance. Fig. 15 shows three-phase experimental system currents before compensation during 20%, 50%, 70%, and 90% loading conditions. Figs. 16 and 17 show the corresponding three-phase experimental system currents after HAPF controller and the proposed mixed signal controller, respectively.

Comparing Figs. 16 and 17, the proposed mixed signal controller can provide better compensation performance, particularly during light loading conditions. For example, the THD values in phase A are improved from 20.7% to 13.9%, 17.6% to 10.8%, 6.3% to 5.7%, and 5.9 to 5.6, for 20%, 50%, 70%, and 90% of the loading, respectively. Using a conventional digital controller, the $\mathrm{THD}_{i_{sx}}$ during 20% loading cannot satisfy the desired value ($\mathrm{THD}_{i_{sx}} < 20\%$), while the proposed mixed signal controller can. This verifies the effectiveness of the proposed controller in improving the HAPF compensation performance. Table V also summarizes the HAPF experimental compensation results using the conventional digital controller and the proposed mixed signal controller during different loading cases.

Fig. 18 shows the dynamic compensation performance during loading changes using the conventional and the proposed controllers. The dynamic response time of both controllers is less than two cycles, which verifies the fast dynamic response of the proposed controller and the function of on-the-fly mixed signal reconfiguration.

V. Conclusion

A mixed signal controller for power quality compensator improvement with adaptive gain and on-the-fly programmability and with a self-reconfiguration property in a three-phase four-wire HAPF system has been proposed in this study. It can achieve better performance than a conventional digital controller. To detect the compensation performance instantaneously, an ATHD index was deduced. From this, the corresponding gains can be calculated in the FPGA and transferred by feedback to the FPAA in a dynamic configuration process. The system implementation and communication between the analog and the digital controllers are discussed. Moreover, the viability and effectiveness of the proposed mixed signal controller for three-phase four-wire HAPF have been demonstrated with experimental results, which exhibit better compensation performance when compared with conventional digital controllers during light load conditions.

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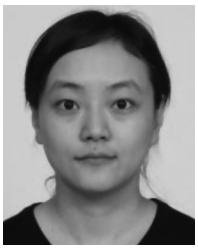
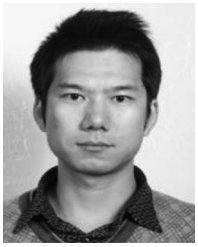
From 2012 to 2014, he was a Research Assistant in Power Electronics Laboratory, UM, where he is currently a Technician of Electric Power Engineering Laboratory. His research interests include power electronics applications and power quality compensation.

Mr. Choi received the Macao Scientific and Technological R&D Award for Postgraduates (M.Sc. level) in 2014.



Ning Yi Dai (S'05–M'08) was born in Jiangsu, China. She received the B.Sc. degree in electrical engineering from the Southeast University, Nanjing, China, in 2001, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the Faculty of Science and Technology, University of Macau, Macao, China, in 2004 and 2007, respectively.

She is currently an Assistant Professor in the Department of Electrical and Computer Engineering, University of Macau. She has published more than thirty technical journals and conference papers in the field of power system and power electronics. Her research interests include application of power electronics in power system, renewable energy integration, and pulse width modulation.



Yajie Wu was born in Xinjiang, China, in 1982. He received the B.S. degree in physics from Nanjing Normal University, Nanjing, China, in 2004, and the M.S. degree in electronic engineering from Southeast University, Nanjing, in 2007. He is currently working toward the Ph.D. degree at the integrated Power Electronics Controller Lab, University of Macau, Macao, China.

From 2007 to 2012, he was a Senior Digital Circuit Design Engineer at Actions-semi Corporation. His research interests include the field of digital integrated circuit design, video codec IP design, and mixed-signal integrated power electronics controller design.

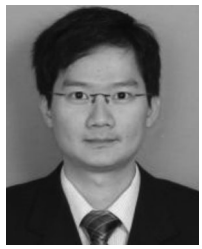
Chi-Kong Wong (M'91) was born in Macao in 1968. He received the B.Sc. and M.Sc. degrees in electrical and electronics engineering (EEE) from the University of Macau, Macao. China, in 1993 and 1997, respectively, and the Ph.D. degree in EEE from Tisnghua University, Beijing, China, in 2007.

He was recruited by the University of Macau as a Teaching Assistant for the Faculty of Science and Technology in 1993 and promoted to the post of a Lecturer and an Assistant Professor in 1997 and 2008, respectively. Since 1997, he has been teaching the fundamental courses for the Department of Electrical and Electronics Engineering and supervising the final year projects. In addition of the undergraduated teaching and supervision, he had also cotaught one masters' course and cosupervised three masters' research projects. From 1997 to 2007, he had conducted four University research projects and five external projects form CEM and organized one power system protection training course to CEM staffs. His research interests include voltage stability analysis, synchronized phasor measurement applications in power systems, wavelet transformation applications in power systems, renewable energy, and energy saving.

Sai-Weng Sin (S'98–M'06–SM'13) received the B.Sc., M.Sc., and Ph.D. degrees with the highest honor in electrical and electronics engineering from the University of Macau, Macao, China, in 2001, 2003, and 2008, respectively.

He is currently an Assistant Professor in the Faculty of Science and Technology, University of Macau, and is the Coordinator of the Data Conversion and Signal Processing Research Line in the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. He has published one book entitled *Generalized Low-Voltage Circuit Techniques for Very High-Speed Time-Interleaved Analog-to-Digital Converters* (New York, NY, USA: Springer), hold five U.S. patents, and more than 80 technical journals and conference papers in the field of high performance data converters and analog mixed-signal integrated circuits.

Dr. Sin is currently the Secretary of the IEEE Solid-State Circuit Society (SSCS) Macau Chapter and the IEEE Macau CAS/COM Joint Chapter. He received the 2012 IEEE SSCS World Chapter of the Year Award, the 2011 ISSCC Silk Road Award, the Student Design Contest Award in A-SSCC 2011, and the 2011 State Science and Technology Progress Award (second-class), China.



U-Fat Chio received the B.Sc. degree in electrical engineering and the M.Sc. degree in communications engineering from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2002 and 2004, respectively, and the Ph.D. degree from the University of Macau, Macao, China, in 2012.

From 2004 to 2005, he was with DenMOS Technology Inc., Hsinchu, Taiwan. He is currently a Postdoctoral Fellow with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. His research interests include high-speed analog-to-digital converters and power management circuit designs.

Seng-Pan U (S'94–M'00–SM'05) received the B.Sc. and M.Sc. degrees, in 1991 and 1997, respectively, and the joint Ph.D. degree from the University of Macau (UM), Macao, China, and the Instituto Superior Técnico (IST), Lisboa, Portugal, in 2002 with highest honor in the field of high-speed analog IC design.

In 2001, he cofounded the Chipidea Microelectronics (Macau), Ltd., and was an Engineering Director and since 2003, the corporate VP-IP Operations Asia Pacific for devoting in advanced analog and mixed-signal semiconductor IP product development. The company was acquired in 2009 by the world leading EDA and IP provider Synopsys Inc., currently as Synopsys Macau Limited. He is also the corporate Senior Analog Design Manager and Site General Manager. He has been with the Department of Electrical And Electronics Engineering, Faculty of Science and Technology, UM, since 1994, where he is currently a Professor and the Deputy Director of the State-Key Laboratory of Analog and Mixed-Signal VLSI, UM. During 1999–2001, he was also on leave from the Integrated CAS Group, Center of Microsystems in IST, as a Visiting Research Fellow. He has published more than 140 scientific papers in IEEE/IET journal and conferences, coholds nine U.S. patents, and coauthored four books in Springer and China Science Press in the area of VHF SC filters, analog baseband for multistandard wireless transceivers, and very high-speed TI ADCs.

Dr. U received ∼30 research and academic/teaching awards and is also the advisor for ∼30 various international student paper award recipients, e.g., the ISSCC Silk-Road Award, IEEE DAC/ISSCC Student Design Contest, A-SSCC Student Design Contest, ISCAS, MWSCAS, PRIME etc. He also received The 2012 IEEE SSCS Outstanding Chapter Award as the Macau Founding Chairman. Both at the first time from Macau, he received the Science and Technology (S&T) Innovation Award of Ho Leung Ho Lee Foundation in 2010, and also The State S&T Progress Award in 2011. He also received both the 2012 and 2014 Macau S&T Invention and Progress Awards. In recognition of his contribution in high-technology research and industrial development in Macau, he was awarded by Macau SAR government the Honorary Title of Value in 2010. He was also selected as the "Scientific Chinese of the Year 2012." He is currently the Industrial Relationship Officer of IEEE Macau Section, the Chairman of IEEE SSCS and CAS/COMM Macau Chapter. He is currently an IEEE SSCS Distinguished Lecturer for 2014–2015. He was A-SSCC 2013 Tutorial Speaker for Energy-Efficient SAR-Type ADCs and has also been with the technical review committee of various international scientific journals for many years, e.g. JSSC, TCAS, IEICE, etc. He was the Chairman of the Local Organization Committee of IEEJ AVLSIWS'04, the TPC Cochair of the IEEE APCCAS'08, ICICS'09, and PRIMEAsia'11. He is currently with the TPC of ISSCC, A-SSCC, RFIT, VLSI-DAT, and an Editorial Board Member of the Journal AICSP.

Rui P. Martins (M'88–SM'99–F'08) born in April 30, 1957. He received the Bachelors' (five years), Masters', and Ph.D. degrees, as well as the Habilitation for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering, IST, TU of Lisbon, since October 1980. Since 1992, he has been on leave from IST, TU of Lisbon (now the University of Lisbon since 2013), and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor since August 2013. In FST, he was the Dean of the Faculty from 1994 to 1997 and he has been a Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed in 2013 as a Vice-Rector (Research) until August 31, 2018. Within the scope of his teaching and research activities, he had taught 21 bachelors' and masters' courses and has supervised (or cosupervised) 35 theses, 15 of Ph.D., and 20 of Masters. He has coauthored five books and four book chapters (refereed); nine U.S. patents; 291 refereed papers, in scientific journals (70) and in conference proceedings (221); as well as other 47 academic works, in a total of 356 publications. He was a cofounder of Chipidea Microelectronics (Macao) [now Synopsys] in 2001/2002, and created the Analog and Mixed-Signal VLSI Research Laboratory of University of Macau, in 2003, elevated in January 2011 to the State Key Laboratory of China (the first in engineering in Macao), being its Founding Director.

Dr. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005, and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 [2009 World Chapter of the Year of the IEEE CASS]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on Circuits and Systems, and was the Vice-President for the Region 10 (Asia, Australia, the Pacific) of the IEEE CAS Society from 2009 to 2011. Since then, he was the Vice-President of (World) Regional Activities and a Member of the IEEE CAS Society from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2010 to 2013, and was nominated as the Best Associate Editor of T-CAS II for 2012 to 2013. Plus, he has been a Member of the IEEE CASS Fellow Evaluation Committee for Classes of 2013 and 2014, and he is the CAS Society Representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—Director of the IEEE. He received two government decorations: The Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences in Lisbon, being the only Portuguese Academician living in Asia.