A 0.02 mm^2 59.2 dB SFDR 4th-Order SC LPF With 0.5-to-10 MHz Bandwidth Scalability Exploiting a Recycling SC-Buffer Biquad

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***Abstract*—This paper reports a switched-capacitor (SC)-buffer Biquad that can be recycled efficiently as an ultra-compact low-pass filter (LPF) in nanoscale CMOS. It incorporates only passive-SC networks and open-loop unity-gain buffers; both are friendlier to technology downscaling than most conventional Biquads that use high-gain amplifiers and closed-loop negative feedback. Complex-pole pairs with independent Q factors are recursively realized in one clock period, while ensuring low crosstalk effect between the formations of each pole. Nonlinearity and parasitic effects are inherently low due to no internal gain. The fabricated 65 nm CMOS prototype is a 1x-recycling SC-buffer Biquad that is equivalent to a 4th-order Butterworth LPF with 75% buffer utilization. It occupies a die size of only 0.02 mm^2 and exhibits 20x bandwidth tunability (0.5 to 10 MHz), linear with the clock rate. At 10 MHz bandwidth, the in-band IIP3 is +17.6 dBm and input-referred noise is 19.5 nV/$\sqrt{}$Hz; they correspond to 59.2 dB SFDR and 0.013 fJ figure-of-merit which are favorably comparable with the recent art. The 1 dB compression point (P_{1dB}) conforms to the out-of-band blocker profile of the LTE standard at a 20 dB front-end gain.**

***Index Terms*—1 dB compression point ($P_{1\,dB}$), Butterworth, clock generator, CMOS, channel selection, clock-rate-defined bandwidth (BW), die area, figure-of-merit (FOM), low-pass filter (LPF), long-term evolution (LTE), operational transconductance amplifier (OTA), recycling, switched capacitor (SC), wireless radios.**

I. Introduction

In response to the ever-increasing demand for higher data rates, long-term evolution (LTE) and wireless local-area network (WLAN) radios have introduced the carrier aggregation (CA) and multiple-input multiple-output (MIMO) techniques to enhance their throughput [1], [2]. Yet, each CA or MIMO channel calls for a separate radio front-end, pressuring the area budget of each analog function. In fact, merely the numerous channel-selection low-pass filters (LPFs) occupy a substantial area of the radio, e.g., ~11% in [2]. For common LPF topologies like active-RC and g_m-C that hinge on passives to define the time constant, the die area can be relatively large because of bandwidth (BW) tuning and kT/C requirement. Also, to resist the process variations and allow BW scaling, spare capacitor banks are unavoidable [3]–[5]. Although the recent ring-oscillator-based LPF [6] has improved area and power efficiencies (0.073 mm^2 and 0.73 mW per complex pole), the BW could only be tuned by the supply voltage. This undertaking couples the BW scalability with other performance metrics, while entailing a precision voltage regulator to avoid drifting of BW against PVT. The active-RC LPF in [7] benefits from a switched-mode operational amplifier (SMOA) for rail-to-rail signal handling well-suited for low-voltage (0.6 V) and wide-BW (70 MHz) applications. However, the achieved area and power efficiencies (0.095 mm^2 and 6.55 mW per complex pole) are inferior to [6], and spare passive elements are still entailed for BW scaling or correction similar to other active-RC LPFs.

In fact, downscaling of CMOS has enabled faster switches, less parasitics and better capacitor matching. All rekindle the interest on switched-capacitor (SC) LPFs, especially for multi-standard radios demand high BW flexibility. Although an anti-aliasing filter (AAF) is required (normally embedded into the mixer's RC load), SC solutions are competitive to reject the close-in adjacent/alternate channels. A real-pole SC LPF implementation [8] shows very low power (1.96 mW) and noise (2.85 nV/$\sqrt{}$Hz), being an attractive analog approach to partition the channel selection to the digital domain for power and area savings [9]. Regrettably, despite the used 7th-order, the lack of complex poles worsens the roll-off around the -3 dB BW. Also, large spread (i.e., 256) of capacitors limits its area efficiency (0.06 mm^2 per real pole). For a typical active-SC LPF that can offer complex poles, operational transconductance amplifiers (OTAs) should be employed [10], [11], but are harder to be efficiently realized in modern CMOS. This fact renders the active-SC LPF not as common as its active-RC and g_m-C counterparts in recent years. Other techniques have also been reported to alleviate such an issue for SC circuits, such as the gain regulation [12] and charge assisting [13]. The former entails an additional control loop to precisely set the gain, while the latter requires extra buffers and clock phases for the assisting circuit.

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This work aims at an ultra-compact calibration-free SC LPF with a clock-rate-defined BW suitable for ultra-scaled CMOS. Unlike the traditional non-OTA SC Biquads that use bilinear SC integrators [14], [15], our *recycling SC-buffer Biquad* involves only passive-SC networks and open-loop unity-gain buffers. Recycling such a Biquad once is equivalent to a 4th-order Butterworth LPF. The prototype fabricated in 65 nm CMOS achieves 4.7x wider BW tunability, 8x higher area efficiency and 1.52x better figure-of-merit (FOM) than the recent art. Also, since the Biquad features no internal gain, low parasitic effects and high linearity are inherently assured albeit there is no virtual ground.

Section II presents the real-pole SC LPF. The proposed recycling SC-buffer Biquad is described in Section III, and its circuit non-idealities are analyzed in Section IV. The prototype sizing and optimization are detailed in Section V, followed by the experimental results given in Section VI. The conclusions are drawn in Section VII.

II. Real-Pole SC LPF

A 1st-order SC LPF can be as simple as a passive-SC network as shown in Fig. 1(a). Driven by a 2-phase 50% clock (Φ_1 and Φ_2), the switches and sampling capacitor C_s emulate a parasitic-insensitive SC-based resistor controlling the signal current that goes into the integrating capacitor C_i. When V_{out} is taken out at the end of Φ_2, the z-domain transfer function of this LPF is given by

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{(\alpha-1)z^{-\frac{1}{2}}}{1-\alpha z^{-1}} \tag{1}$$

where $\alpha = (C_i)/(C_s + C_i)$. The unity-gain buffer decouples the passive-SC network from the load facilitating filter-order extension. This SC LPF gives rise to a real pole with tunable time constant by adjusting the clock (f_{clk}), and the capacitive ratio of C_i and C_s can be accurately defined in fabrication ($< 1\%$ error). As such, the cutoff frequency of this SC LPF is intrinsically accurate, and widely tunable without any calibration loop or spare elements. The buffer can be an open-loop single-stage amplifier that has no parasitic pole, being a more prospective choice for high-speed operation than the OTA-based SC integrator that involves closed-loop charging/discharging a feedback capacitor.

To further save area and power, the buffer can be recycled to build more poles by sub-dividing the clock period ($T_c = 1/f_{clk}$). For instance, two real poles can be built with one buffer [Fig. 1(b)] under a 3-phase 33% clock, yielding a multiplicative transfer function of two independent real poles as given by

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{(\alpha_1-1)z^{-\frac{2}{3}}}{1-\alpha_1 z^{-1}} \cdot \frac{(\alpha_2-1)z^{-\frac{1}{3}}}{1-\alpha_2 z^{-1}} \tag{2}$$

where $\alpha_1 = (C_{i1})/(C_{s1} + C_{i1})$ and $\alpha_2 = (C_{i2})/(C_{s2} + C_{i2})$. Obviously, one buffer is saved (so as the static power), but the buffer has to be 1.5x faster for the same settling accuracy as that of Fig. 1(a). The buffer utilization is improved from 50% (i.e., one pole in 2 phases) to 66.7% (i.e., two poles in 3 phases). Both the filter order and buffer utilization can be extended by recycling more often the buffer, but the response is restricted to only real poles. For instance, when recycling the LPF by 4x (Fig. 2), the -3 dB BW drops from 10 to 4 MHz, and the roll-off

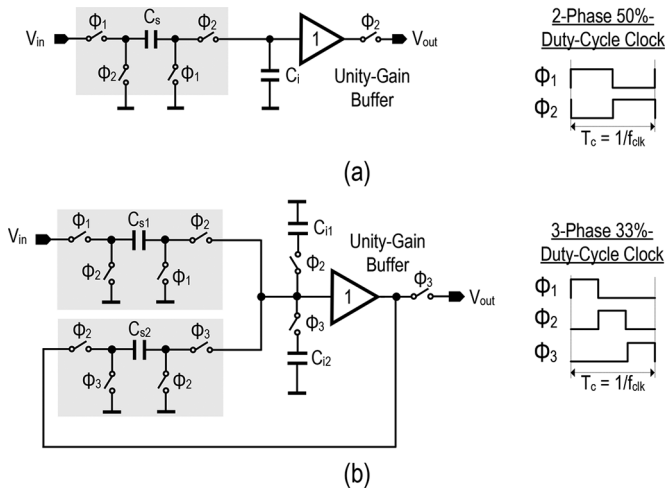


Fig. 1. (a) 1st-order SC-Buffer LPF. The buffer utilization is 50% under a 2-phase 50% clock. (b) 2nd-order SC-Buffer LPF by recycling the buffer. The buffer utilization is 66.7% under a 3-phase 33% clock. Both realize only real pole(s).

is much smoother than the typical Butterworth LPF. Driven by this fact, this work investigates a recycling Biquad that can offer complex poles with the Q factors controllable in each phase, as presented next.

III. SC-Buffer Biquad

A. Basic Topology

With unity gain buffers it is possible to design SC integrators and, subsequently, filters with complex poles [14], [15]. The Biquad scheme of Fig. 3 is simpler than using the SC integrators of [14], [15]. It employs two cascaded 1st-order passive-SC networks with the output of the second passive-SC network fed back to C_{i1} to build the complex poles. The AC-coupling established by C_{i1} opens the loop at low frequencies and speeds up the operation. Both V_{outa} and V_{outb} can serve as the outputs. Assuming all capacitors are fully charged during each clock phase, the z-domain transfer function of V_{outa} and V_{outb} can be expressed as

$$\frac{V_{outa,b}(z)}{V_{in}(z)} = \frac{\alpha_1\alpha_2 z^{-2}}{(\alpha_1-1)z^{-2} + (2-\alpha_1-\alpha_1\alpha_2)z^{-1} - 1} \tag{3}$$

where α_1 and α_2 are the same as (2). The transfer function in the s-domain (assuming $\omega \ll 1/T_c$) is given by

$$\frac{V_{outa,b}(s)}{V_{in}(s)} = \frac{1}{\frac{C_{i1}C_{i2}}{C_{s1}C_{s2}}T_C^2 s^2 - \frac{C_{i2}}{C_{s2}}T_C s + 1}. \tag{4}$$

From (4), $\omega_n = (f_{clk})/\sqrt{(C_{i1}C_{i2})/(C_{s1}C_{s2})}$, $Q = \sqrt{(C_{s2}C_{i1})/(C_{s1}C_{i2})}$, and $C_{s1} = C_{s2}$ can be handily chosen. Complex poles are formed if $Q > 0.5$. For simplicity, (4) neglects the buffer's output resistances (R_{on1} and R_{on2}) as they mainly affect the stopband profile that will be analyzed in Section IV. The tunability of BW and Q is illustrated in Fig. 4.

The two buffers isolate the two passive-SC networks and help to reduce the capacitor spread when compared with the Sallen-Key SC Biquad that uses a single buffer. For instance, in

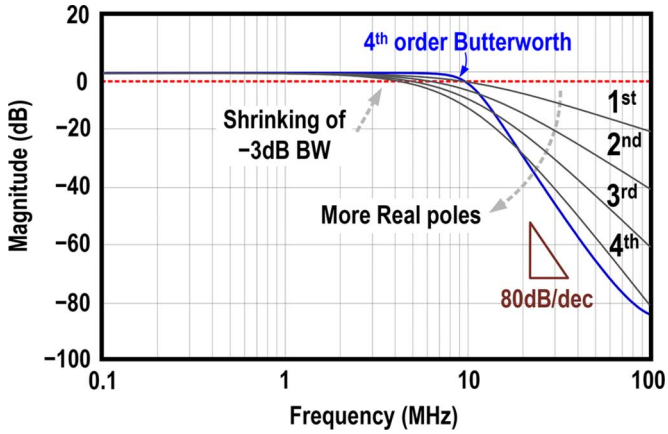


Fig. 2. Comparing the gain response from a 1st-order to a 4th-order real-pole-only LPF to a typical 4th-order Butterworth LPF. The former suffers from the shrinking of −3 dB BW, and has a weaker roll-off due to the non-existence of complex poles.

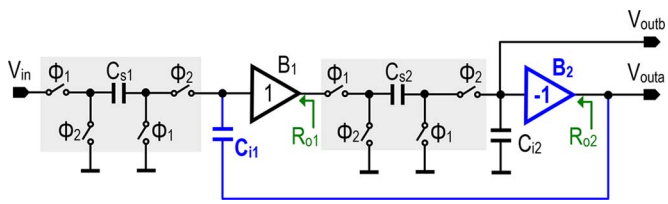


Fig. 3. Proposed SC-buffer Biquad.

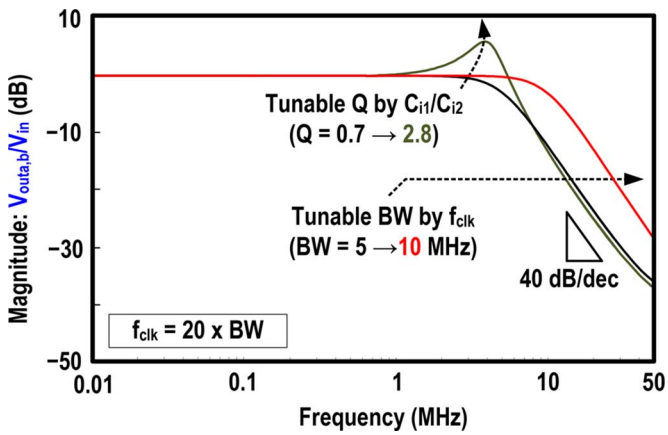


Fig. 4. Tunability of BW and Q of the proposed SC-buffer Biquad.

a differential implementation, the Sallen-Key SC Biquad with $Q = 1.93$ entails a capacitor spread of 14.8, while it is just 5.7 in the proposed SC Biquad, improving area efficiency and matching accuracy.

Conventionally, a high-order LPF (e.g., 4th-order Butterworth) is realized by cascading Biquads with different Q. In this work, a high-order SC LPF is obtained by recycling the Biquad and altering its Q on-the-fly. The circuit diagram is conceptualized in Fig. 5. Driven by an n-phase clock, the BW and Q of the Biquad can be switched to different values in different phases, recycling the buffers, and parts of the capacitor and switch elements. Empirically, starting from Φ_1, the input signal is sampled into the Biquad, which chooses one set of capacitor ratio to define the BW_x and Q_x. Its output is

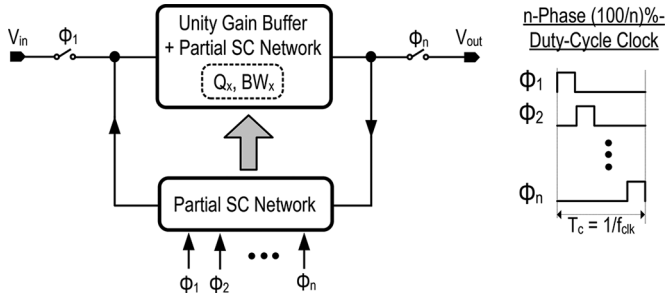


Fig. 5. Conceptual diagram of a recycling SC-buffer Biquad for higher-order filtering.

then fed back to its input for another round of filtering under different BW_x and Q_x before final outputting the signal at Φ_n. The overall operation is equivalent to an nth-order LPF with $(n-1)/n \times 100\%$ buffer utilization.

B. RC Settling Accuracy and Speed Tradeoff

The tradeoff between RC settling accuracy and speed of a recycling SC LPF is highly related to the technologies (65 nm CMOS here). We study it by analyzing the recycling SC-buffer Biquad as shown in Fig. 6, which offers 4th-order filtering. The simulated on-resistance and parasitic capacitance of a transmission-gate switch are plotted in Fig. 7. For a channel width of 8 μm, the switch's on-resistance is $\sim$70 Ω and parasitic capacitor is just $\sim$8 fF. Thus, the time constant τ is 0.22 ns for a 1.5 pF sampling capacitor (C_{s1-3}), and, even if 99.6% settling accuracy (i.e., 5.45τ) is required, f_{clk} can be as high as 200 MHz.

Ideally the Biquad can be recycled several times to rise up the filter-order, but the physical constraint must be considered. As n-time recycling leads to n-time duty-cycle reduction of the clock, the size of the switches and speed of the clock generator must be increased to achieve the same RC settling accuracy. Yet, using bigger switches also introduces more parasitics, degrading the accuracy of the LPF's AC response. To this point, we assess it using the switch's characteristic (Fig. 7). Fig. 8 shows the tradeoff between the RC settling accuracy and gain loss for 2nd- to 8th-order SC LPFs. As expected, more recycling can penalize the RC settling accuracy and passband gain. As an example, the 6th-order LPF shows $\sim$4 dB (2 dB) gain loss for a RC settling accuracy of 99% (95%). In this work, a 4th-order LPF is implemented by one-time recycling, at a switch's width of 8 μm.

C. Crosstalk Effect

When the SC-buffer Biquad is recycled, the parasitic capacitors can induce crosstalk (memory) effect [16] in each duty cycle. As marked in Fig. 6, the critical parasitic capacitors are $C_{p1,2}$ at the buffer's input, and $C_{p4,5}$ induced between the integrating capacitors $C_{i1,3}(C_{i2,4})$. C_{p3} is ignorable as it is associated with the buffer's output. Fig. 9 plots the simulated gain response of Fig. 6, in which $C_{p1,2}$ vary from 0 to 250 fF. As the buffer has no internal gain, and there is no feedback capacitor between the buffer's input and output, $C_{p1,2}$ mainly induces gain loss in the passband, which varies almost linearly with the values of $C_{p1,2}$. For $C_{p1,2} = 40$ fF in this work, the gain loss is $\sim$2 dB. Also, due to the charge sharing between $C_{i1,3}$ $(C_{i2,4})$, a

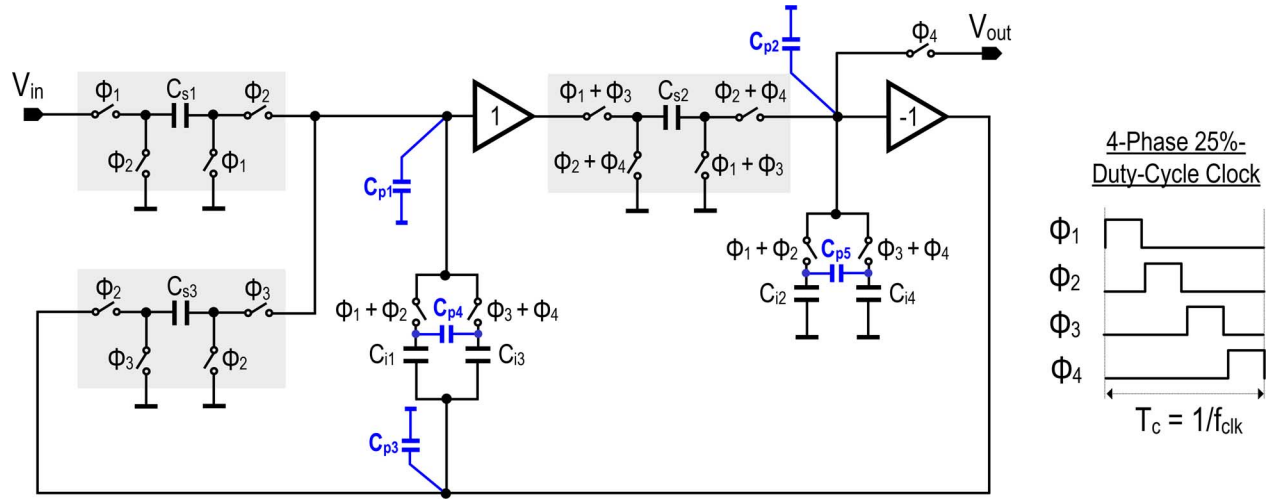


Fig. 6. Proposed recycling SC-buffer Biquad as a 4th-order SC LPF. The major parasitic capacitors C_{p1-3} are explicitly shown.

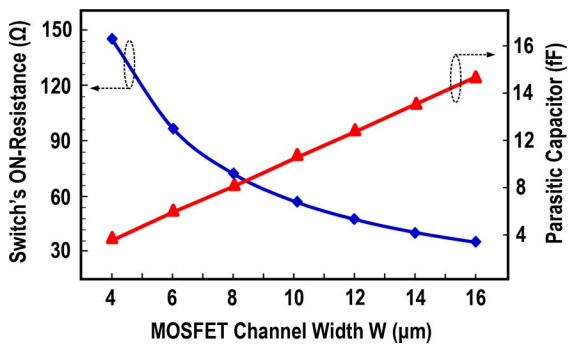


Fig. 7. On-resistance and parasitic capacitor of a transmission-gate CMOS switch against the MOSFET channel width (W).

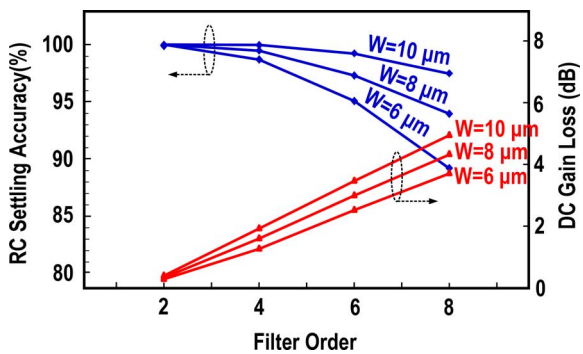


Fig. 8. Tradeoff between the RC settling accuracy and gain loss for different filter order and MOSFET channel width (W).

large parasitic capacitor can cause a gain peak nearby the cutoff frequency. Thus, it is essential to choose a large C_{i1-4} while minimizing the size of the switches. Both verify a tradeoff between area, power and RC settling accuracy. The signal loss due to the crosstalk effect induced by C_{p4} (similar for C_{p5}) in each duty cycle can be estimated as: $(C_{p4}\|C_{i,n})/(C_{p4}+C_{p4}\|C_{i,n})$, where $n = 1$ for the 1st cycle, and $n = 3$ for the 2nd cycle. The extracted $C_{p4,5}$, is <30 fF for a pF-range MOM capacitor that has a 1.6% parasitic effect. From simulations, this effect degrades the stopband attenuation by 1.5 dB.

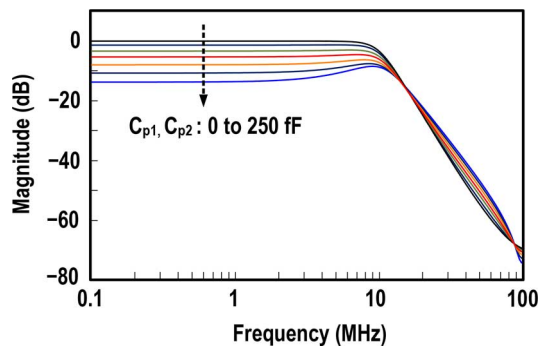


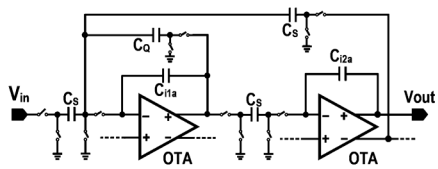
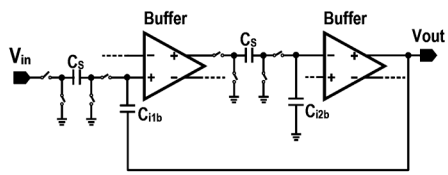
Fig. 9. Frequency responses of the 4th-order SC LPF in Fig. 6 with different sizes of $C_{p1,2}$.

D. Comparison With the SC-OTA Biquad

The proposed SC-buffer Biquad can be compared with its SC-OTA counterpart. A differential Tow-Thomas SC-OTA Biquad is chosen for feature comparison in Table I. For the same parameters (DC gain, cutoff frequency and Q), their area and power efficiencies can be analyzed. Regarding noise performance, the sample-and-hold noise [17] is dominant and $\propto 1/C_S$. Detailed noise analysis is given in the Appendix. Here, we set the same C_S for fair comparison of area and power between the two Biquads. For the SC-buffer Biquad, its DC gain is directly defined by the buffers, whereas the Q and cutoff frequency are set by four capacitor ratios showed in (4). For the SC-OTA Biquad, it involves six capacitor ratios [18] to define those parameters that can impact the device matching and area. Also, the grounded C_{i2} and C_{i4} of the SC-Buffer Biquad can be halved in a differential termination to save area. To exemplify this, in Table I, we choose a 4th-order Butterworth LPF with a unity DC gain and BW $= f_{clk}/20$. Half of the total capacitor can be saved for the proposed design. Indeed, the die area of the fabricated LPF is dominated by the capacitors. To this point, the Sallen-Key SC Biquad becomes very area hungry for high Q realization due to its large capacitor spread.

The BW of the buffer and OTA are strongly related to their circuit topologies. In this work, the buffer is a simple

TABLE I
PARAMETERS COMPARISON OF CONVENTIONAL SC-OTA LPF AND PROPOSED SC-BUFFER LPF

Schematic (Only Biquads are shown)				
Parameters	OTA-based LPFs (Differential)		**SC-Buffer-based LPFs (differential)**	
	2nd order Butterworth	4th order Butterworth (By recycling Biquad)	**2nd order Butterworth**	**4th order Butterworth (By recycling Biquad)**
Total Capacitor [1]	$21.5C_s$	$40.7C_s$	$\mathbf{10.75C_s}$	$\mathbf{21.9C_s}$
Acitve Elements [2]	2 OTAs	2 OTAs	**2 Buffers**	**2 Buffers**
Settling Speed [3]	$(\frac{2I_{total}}{V_{OV}})/2C_s$	$(\frac{2I_{total}}{V_{OV}})/2C_s$	$\mathbf{\left(\frac{2I_{total}}{V_{OV}}\right)/C_s}$	$\mathbf{(\frac{2I_{total}}{V_{OV}})/C_s}$
Noise PSD [4]	$\propto 4kT/f_{clk}C_s$	$\propto 8\beta kT/f_{clk}C_s$	$\mathbf{\propto 4kT/f_{clk}C_s}$	$\mathbf{\propto 8\beta kT/f_{clk}C_s}$

1: $\mathbf{C_s}$ dominates the noise performance.
2 : Assumed a folded-cascode OTA (The speed will be doubled for a telescopic OTA, but at the cost reduced output swing).
3 : $\mathbf{I_{total}}$ is the total bias current, and $\mathbf{V_{ov}}$ is the input transistor overdrive voltage.
4 : $\boldsymbol{\beta}$ is up to 1.2 (from simulations) due to the reduced $\mathbf{f_{clk}}$ duty cycle from 50% to 25%.

differential pair with an active load (Section V), featuring no internal gain node and parasitic poles. It is compared with a folded-cascode OTA for its balanced DC gain, output swing and GBW. Under the same total current (I_{total}), the SC-buffer Biquad has a settling speed doubled than that of the SC-OTA Biquad, because half of the OTA's bias current in the folded branch is consumed to provide the gain. In practice, realizing a high-speed buffer is also easier than a high-speed high-gain OTA in nanoscale CMOS.

IV. ANALYSIS OF CIRCUIT NON-IDEALITIES

A. Stopband Zeros Induced by the Buffer's Output Resistance

Assuming that C_{s1} and C_{s2} in Fig. 3 are fully charged during every clock phase, V_{outa} and V_{outb} have the same z-domain transfer function. Yet, the output resistance of the buffers will affect the stopband profile for both V_{outa} and V_{outb}. Since V_{outa} and V_{outb} serve as outputs of the first and second Biquads, respectively, in a recycling 4th-order LPF as stated above, it is important to study their stopband behavior. V_{outa} can drive the capacitor load as it is connected at the buffer's output. The transfer function of V_{outa} in the s-domain can be rewritten by taking the R_{o1} and R_{o2} into account, as shown in (5) at the bottom of the page.

The two zeros in the numerator can be approximated by $\omega_z \approx 1/(\sqrt{C_{i1}C_{i2}R_{o1}(\frac{T_C}{C_{s2}}+R_{o2})})$. In practice, $T_C/C_{s1}, T_C/C_{s2} \gg R_{o1}, R_{o2}$, and we have $\omega_n \approx 1/\sqrt{\frac{C_{i1}C_{i2}T_C^2}{C_{s1}C_{s2}}} < \omega_z$. The stopband rejection at high frequency from (5) can be estimated by $\frac{R_{o1}(\frac{T_C}{C_{s2}}+R_{o2})}{\frac{T_C^2}{C_{s1}C_{s2}}+R_{o2}(\frac{T_C}{C_{s1}}+R_{o1})+R_{o1}\frac{T_C}{C_{s2}}}$ indicating that one way of improving the high frequency rejection is to reduce the buffer output resistance but it will lead to more power consumption. Similarly, if V_{outb} serves as the output, the corresponding s-domain transfer function can be obtained as shown in (6) at the bottom of the page. Compared with (5), (6) only contains one real zero at high frequency. Thus, the stopband rejection of the second Biquad is better than the first. Obviously, V_{outb} has better stopband rejection when compared with V_{outa} as shown in Fig. 10.

$$\frac{V_{outa}(s)}{V_{in}(s)} = \frac{s^2C_{i1}C_{i2}R_{o1}\left(\frac{T_C}{C_{s2}}+R_{o2}\right)+sC_{i1}R_{o1}+1}{s^2C_{i1}C_{i2}\left(\frac{T_C^2}{C_{s1}C_{s2}}+R_{o2}\left(\frac{T_C}{C_{s1}}+R_{o1}\right)+R_{o1}\frac{T_C}{C_{s2}}\right)+s\left(C_{i1}R_{o1}-C_{i2}\left(\frac{T_C}{C_{s2}}-R_{o2}\right)\right)+1} \quad (5)$$

$$\frac{V_{outb}(s)}{V_{in}(s)} = \frac{sC_{i1}R_{o1}+1}{s^2C_{i1}C_{i2}\left(\frac{T_C^2}{C_{s1}C_{s2}}+R_{o2}\left(\frac{T_C}{C_{s1}}+R_{o1}\right)+R_{o1}\frac{T_C}{C_{s2}}\right)+s\left(C_{i1}R_{o1}-C_{i2}\left(\frac{T_C}{C_{s2}}-R_{o2}\right)\right)+1} \quad (6)$$

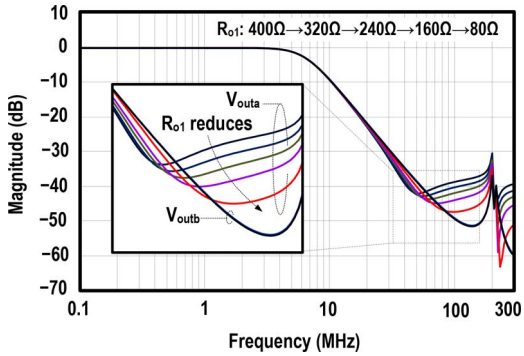


Fig. 10. Comparison of stopband rejection between V_{outa} and V_{outb} under different R_{o1}.

B. Sensitivity to Process Variations

Here the gain sensitivity of the LPF is studied against process variations. The effect of buffer B_1 (with a gain of A_0) in Fig. 3 is analyzed first. By ignoring R_{o1} and R_{o2}, the s-domain transfer function can be simplified as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A_0}{s^2 C_{i1}C_{i2}\frac{T_C^2}{C_{s1}C_{s2}} + s\left(C_{i1}\frac{T_C}{C_{s1}} + C_{i2}\frac{T_C}{C_{s2}} - A_0 \cdot C_{i1}\frac{T_C}{C_{s1}}\right) + 1} \quad (7)$$

with $\omega_n = 1/\sqrt{\frac{C_{i1}C_{i2}T_C^2}{C_{s1}C_{s2}}}$, $Q = \frac{\sqrt{\frac{C_{i1}C_{i2}T_C^2}{C_{s1}C_{s2}}}}{C_{i2}\frac{T_C}{C_{s2}} + C_{i1}\frac{T_C}{C_{s1}}(1-A_0)}$, DC gain $= A_0$. From (7), Q and DC gain of the Biquad are related directly with the buffer's gain, while the dependence with the cutoff frequency is irrelevant. Thus, we have $\frac{dQ}{dA_0} = \frac{\sqrt{\frac{C_{i1}C_{i2}T_C^2}{C_{s1}C_{s2}}}C_{i1}\frac{T_C}{C_{s1}}}{\left[C_{i2}\frac{T_C}{C_{s2}} + C_{i1}\frac{T_C}{C_{s1}}(1-A_0)\right]^2}$ and hence $\frac{dQ}{Q} = \frac{C_{i1}\frac{T_C}{C_{s1}}dA_0}{C_{i2}\frac{T_C}{C_{s2}} + C_{i1}\frac{T_C}{C_{s1}}(1-A_0)}$. Supposing that Q is 0.54 and 1.31 for the two Biquads composing a 4th-order Butterworth response, we can plot their relationships with the buffer's gain as shown in Fig. 11(a).

Variations of threshold voltage and carrier mobility will impact the buffer's performance. Monte-Carlo simulations (process + mismatch) were conducted to assess the gain variation. Since when the gain changes from 0.9 to 1.1, $\Delta Q/Q$ has a variation of 0.2 for $Q = 1.31$, and 0.036 for $Q = 0.54$, the simulation results in Fig. 11(b) reveal that the mean value of the DC gain only has 0.33% deviation with $\sigma = 0.028$. For the buffer B_2, a similar transfer function can be obtained, and the Q has the same expression as stated above.

V. Prototype Sizing and Optimization

The recycling SC-buffer Biquad is equivalent to a 4th-order Butterworth SC LPF (Fig. 12). Differential implementation allows the use of C_{i2} (3.75 pF) and C_{i4} (1.125 pF), differentially, to save chip area. C_{s1-3} (1.5 pF) are equal, such that C_{s2} can be shared by both Biquads. Due to the lack of virtual ground, the parasitic capacitances that are worth to consider are C_{p1-3}. $C_{p4,5}$ are the coupling capacitors within C_{i1-4}. Downsizing the switches while enlarging C_{s1-3} and C_{i1-4} can reduce the parasitic effects, but the time constant associated with the capacitors and switches' on-resistance are limited by f_{clk}.

The nonlinearity is originated mainly by the buffer. Meanwhile the LPF's cutoff frequency also depends on the buffer's BW. The schematic of the buffer is shown in Fig. 12 (right), where the input voltage is converted into current through the input differential pair $M_{1,2}: i = g_1V_1 + g_2V_1^2 + g_3V_1^3$ and they are loaded by $M_{3,4}$ for returning the current back to voltage: $V_o = k_1 i + k_2 i^2 + k_3 i^3$. This process can be treated as two nonlinear conversions in cascade. Volterra Operators [19] are employed for distortion calculation. The third-intermodulation term (IM_3) of the output node can be written as $IM_3 = \frac{3V_{in}^2}{4} \cdot \frac{H_3}{H_1}$, and H_3 is the third-order Volterra Operator of the buffer that can be given by

$$\begin{aligned} H_3(s_1,s_2,s_3) = {} & G_1(s_1)G_1(s_2)G_1(s_3)K_3(s_1,s_2,s_3) \\ & + G_3(s_1,s_2,s_3)K_1(s_1+s_2+s_3) \\ & + \frac{2}{3}[G_1(s_1)G_2(s_2,s_3)K_2(s_1,s_2{+}s_3) \\ & + G_1(s_2)G_2(s_1,s_3)K_2(s_2,s_1{+}s_3) \\ & + G_1(s_2)G_2(s_1,s_3)K_2(s_2,s_1{+}s_3)] \end{aligned} \quad (8)$$

where G_n and K_n are nth Volterra operators of the first and second nonlinear conversions, respectively. Supposing that G_n and K_n are frequency independent variables, the following values to nullify the third-order term of the buffer can be chosen: $k_1 = \frac{1}{g_1}$, $k_2 = -\frac{g_2}{g_1^3}$, and $k_3 = \frac{1}{g_1^4}(-g_3 + 2\frac{g_2^2}{g_1})$. These parameters can be modified by tuning the bias voltage V_b. The linearity is also strongly related with the overdrive voltage (V_{ov}) of $M_{1,2}$ that affects g_1, g_2 and g_3. Two closely spaced tones around 2 MHz with 200-mV amplitude were used to characterize the buffer's linearity. Meanwhile the buffer's BW is $\propto 1/V_{OV}$, as plotted in Fig. 13 together with the IM_3. As expected, a small V_{OV} benefits the BW at the expense of linearity. Here, for the LPF to achieve a 10 MHz BW under a 200 MHz f_{clk}, $V_{ov} = \sim$100 mV was chosen. The buffer has a simulated BW of 460 MHz, which can provide 97.3% settling accuracy (3.6τ). Further increasing f_{clk} will lead to gain peaking around the band edge, owing to the excessive phase shift of the integrator's frequency response, caused by incomplete settling, and setting off the Q enhancement effect [10], [12]. The IIP_3 of the buffer is 23.5 dBm achieving an IM_3 of 68 dB. The variation of the bias voltage should be <20 mV for not degrading the IM_3 by 10 dB. Accordingly, the IIP_3 of the 4th-order LPF is 19.23 dBm by using the cascade formula:

$$\frac{1}{A_{IIP3}^2} \approx \frac{1}{A_{IIP3,1}^2} + \frac{1}{A_{IIP3,2}^2} + \frac{1}{A_{IIP3,3}^2}.$$

Through the bilinear transformation $s = \frac{2}{T}\frac{z-1}{z+1}$, a rational transfer function in the s-domain can be converted into the

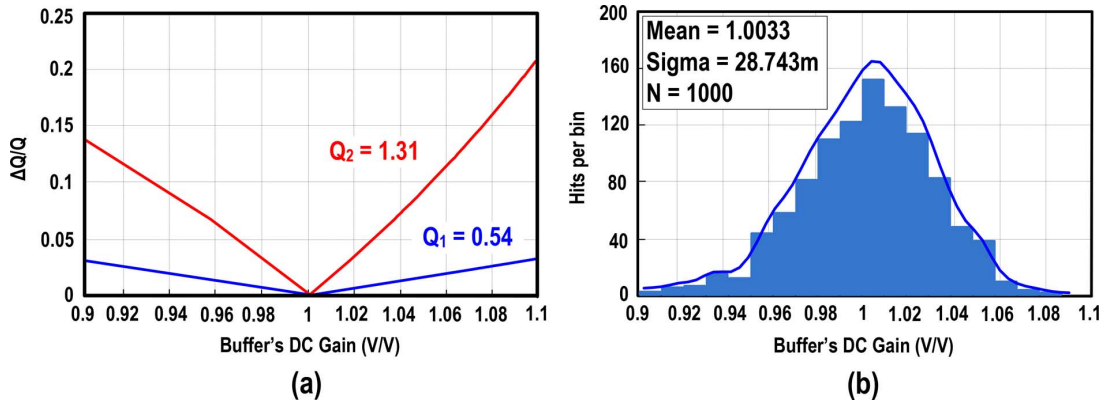


Fig. 11. (a) Q-factor variation with under different buffer's DC gain. (b) Buffer's DC gain distribution in Monte-Carlo simulations.

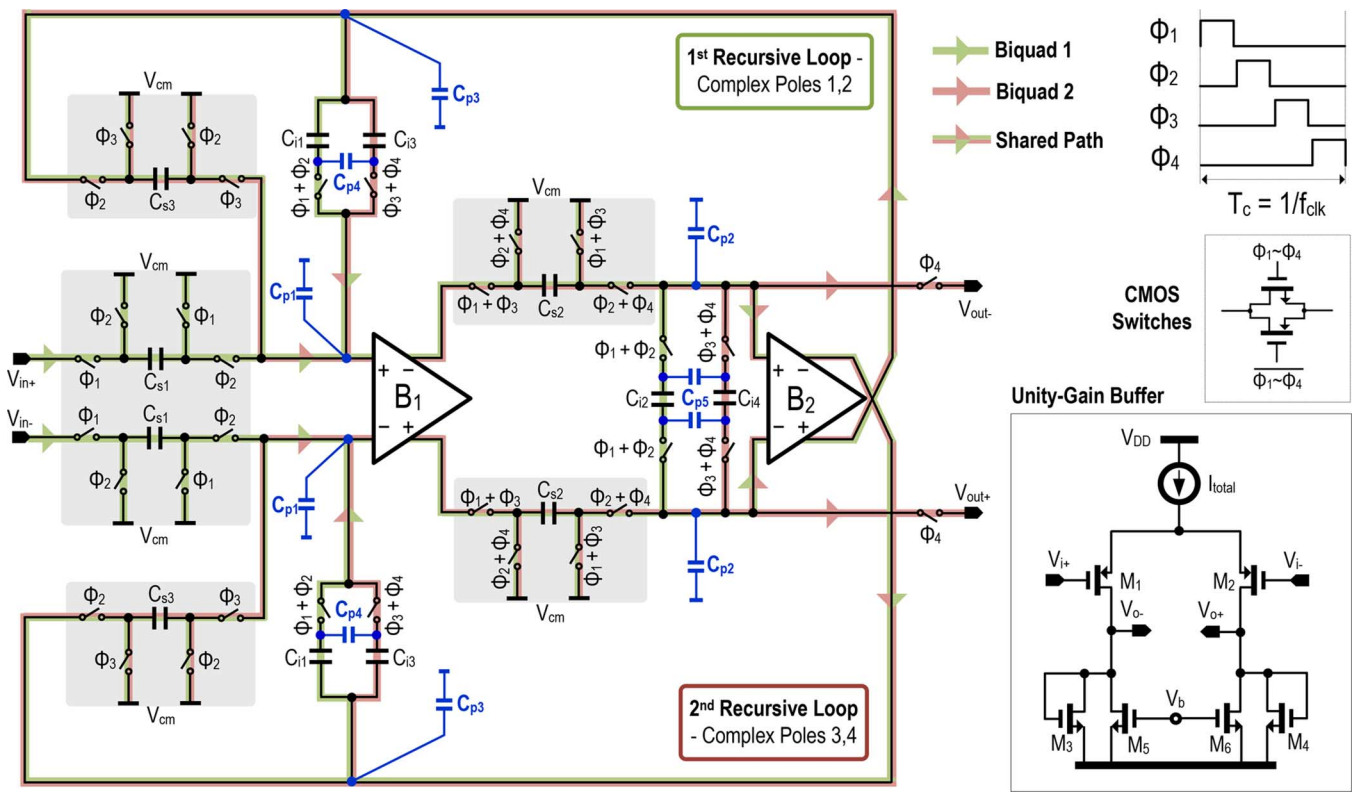


Fig. 12. Implemented differential 4th-order Butterworth SC LPF using the proposed recycling SC-buffer Biquad.

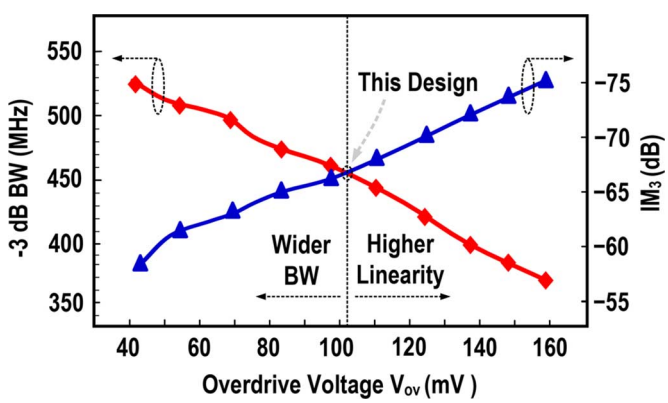


Fig. 13. Tradeoff between BW and linearity under different overdrive voltage V_{OV} for the buffer.

z-domain [18]. For the first Biquad with Q = 0.54, the normalized capacitor ratio is summarized as follows: C_{s1}: C_{s2} : C_{i1} : C_{i2} = 1 : 1 : 1.33 : 2.5. The second Biquad only differs in Q (1.31) with C_{s3} : C_{s2} : C_{i3} : C_{i4} = 1 : 1 : 3.58 : 0.75. These values will vary slightly after layout that takes into account the parasitics. The optimized unit capacitor value is 1518 fF (MOM capacitor cell with 253 fF × 6), which balances the layout effort with the required matching accuracy. The transmission-gate switches have equally-sized NMOS and PMOS to cancel the clock feedthrough and charge injection.

Each buffer consumes a total bias current of 800 μA. Compared with the inverter-based amplifier [8] that entails a common-mode feedback circuit (CMFB) and is sensitive to supply noise, our buffer does not need CMFB and has a

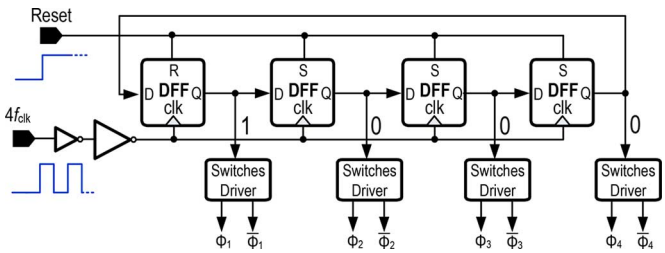


Fig. 14. Clock generator using 4 transmission-gate DFFs.

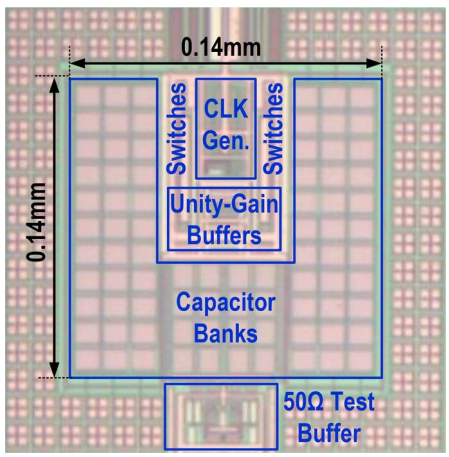


Fig. 15. Chip micrograph of the implemented SC LPF.

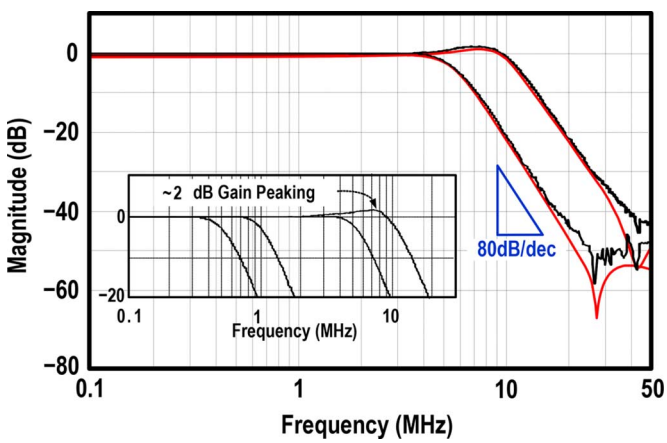


Fig. 16. Measured transfer function of the LPF with f_{clk} swept from 10 to 200 MHz.

simulated PSRR of 48 dB up to 400 MHz (if 1% mismatch between the differential pair). The simulated -3 dB BW at 1.5 pF load is $\sim$580 MHz/mA.

A power-efficient div-by-4 circuit generates the 4-phase 25%-duty-cycle clock by using the transmission-gate D flip-flops (DFFs), as shown in Fig. 14. At power-on, four DFFs are set to "1000". Code "1" is rotated to the next bit at each successive clock cycle. From simulations, the power efficiency is $\sim$1.05 μA/MHz up to a 1 GHz input. The 4-phase f_{clk} at 200 MHz has a rise/fall time $\sim$12.4 ps, which implies $<$1% duty cycle.

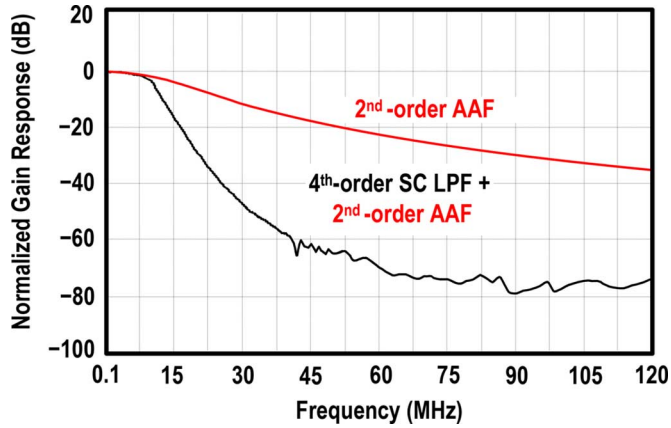


Fig. 17. Combined gain response when the 4th-order SC LPF (at 10 MHz BW) is preceded by a 2nd-order AAF (at 18 MHz BW).

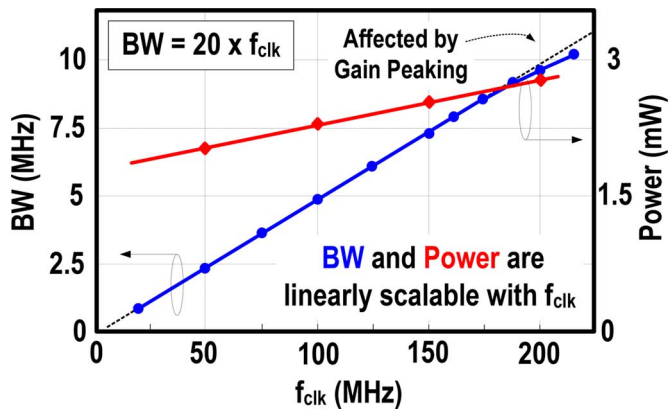


Fig. 18. Measured BW and power are linear scalable with f_{clk}.

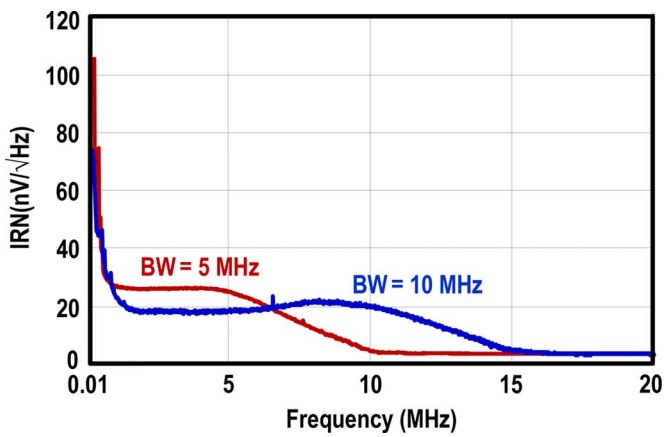


Fig. 19. Measured IRN voltages of at BW $=$ 5 and 10 MHz.

VI. Experimental Results

A. Area, Power and AC Response

The LPF fabricated in 65 nm CMOS occupies 0.02 mm^2 (Fig. 15), in which 77% is the typical MOM capacitor with a density of $\sim$2 fF/μm^2. Fig. 16 plots the measured gain responses. The -3 dB BW is scalable from 0.5 to 10 MHz by raising f_{clk} from 10 to 200 MHz. At 200 MHz f_{clk}, the power consumption is 2.75 mW at 1.2 V excluding the test buffers. The lowest operation frequency is limited by the startup of the clock

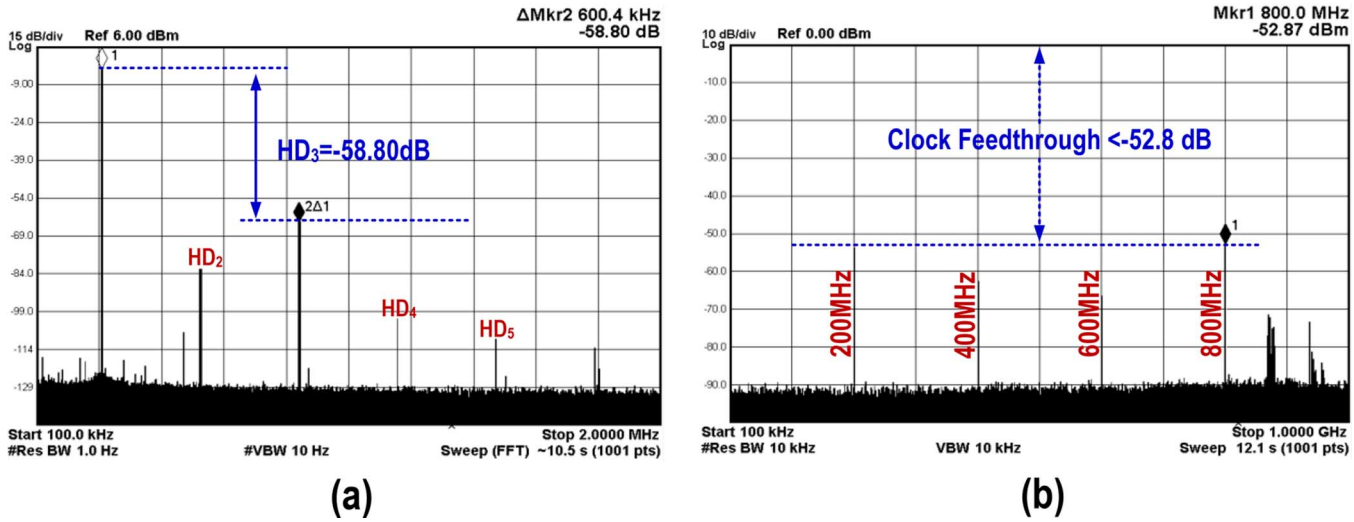


Fig. 20. Measured (a) in-band output spectrum under a 300-kHz input. (b) Far-out spectrum (100 kHz to 1 GHz) showing the clock feedthrough.

generator, whereas the highest value is decided by the buffer's GBW. The gain peaking ($\sim$2 dB) at 10 MHz BW is due to the finite buffer's GBW, and can be utilized to flatten the passband when applying the AAF. The stopband profile (80 dB/dec) is consistent in all cases. The limited stopband rejection is mainly originated by the finite output resistance of the buffers, as analyzed before. Measurement results match well with the simulations especially at low frequency. The notch in the stopband is due to the zeros induced by the buffer's output resistance as analyzed before.

In a receiver, the signal before channel selection by the SC LPF, can be pre-selected by an AAF which is normally embedded into the mixer's RC load. A 1st- or 2nd-order AAF and a high f_{clk} can suppress the amount of aliasing and those image bands. Supposing two 1st-order AAFs in cascade with BW $=$ 18 MHz, the overall transfer function of the 4th-order SC LPF at a 10 MHz BW can be obtained as shown in Fig. 17. Fig. 18 shows that the BW and power are linearly scalable with the frequency. The deviation of the theoretical linear BW at high f_{clk} is due to the Q-enhancement effect caused by the limited buffer's GBW. The clock generator measures a high energy efficiency of 1.18 μA/MHz, which can be further improved with the technology downscaling.

B. Noise

The measured output PSD noises at BWs of 5 and 10 MHz are shown in Fig. 19. The noise peaking below 1 MHz is due to the flicker noise caused by the unity-gain buffers. Noise above 1 MHz is the thermal noise after the sample-and-hold, and shaped by the LPF's transfer function. The noise performance varies with f_{clk} (and thus BW). The input-referred noise (IRN) density measures 28 nV/$\sqrt{}$Hz at 5 MHz BW, and 19.5 nV/$\sqrt{}$Hz at 10 MHz BW; and both match well with the theoretical predictions given in the Appendix.

C. One-Tone and Two-Tone Tests

For the single-tone test, the measured filter in-band output spectrum with 300 kHz input of 2.3 dBm is shown in Fig. 20(a).

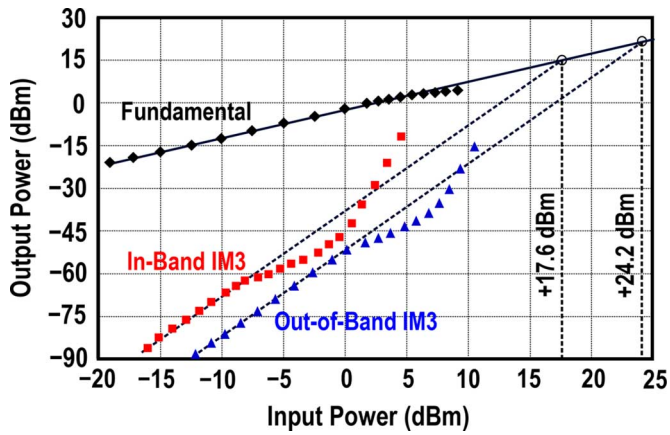


Fig. 21. Measured in-band and out-of-band IIP3.

The plot shows that the in-band spur is dominated by the 3rd-order term and the largest in-band spur is 58.8 dB below the fundamental, mainly due to the high linearity of the buffers. For the out-of-band spectrum purity, there are spurs caused by the clock feedthrough. The largest spur is -52.87 dB at $f_{clk} =$ 800 MHz, as shown in Fig. 20(b).

To evaluate the LPF's linearity, two in-band tones (1.9 and 2 MHz) are injected to the LPF at a 10 MHz BW. The in-band IIP3 is obtained by raising the input power from -16 to 5 dBm. The out-of-band IIP3 is obtained using the same way by injecting the two tones at 20 and 39 MHz. The measured P_{1dB} is 6.2 dBm, and the in-band and out-of-band IIP3 are 17.6 and 24.2 dBm, respectively (Fig. 21). If the effect of the AAF is taken into account, the out-of-band IIP3 can be further enhanced. If an active-RC LPF is loaded to the mixer as the AAF, the in-band linearity will not be affected. For instance, with two 18 MHz passive-RC poles applied at the front, the 20 and 39 MHz tones can be suppressed by $>$6 dB. Another test involves the setting of a 100-kHz-spaced signal to a fixed amplitude equal to 317 mV_{pp}, and sweeping the frequency from 0.2xBW to 1.8xBW to observe IM_3, as shown in Fig. 22.

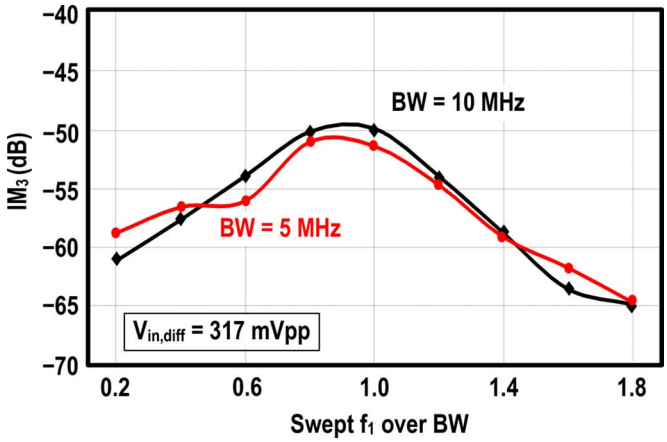


Fig. 22. Measured IM3 profiles at BW = 5 and 10 MHz.

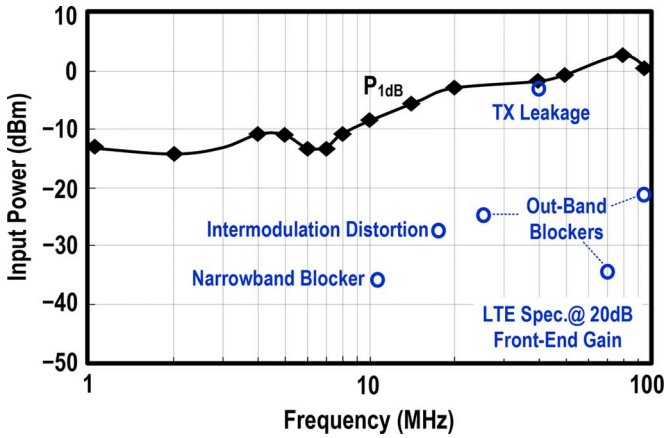


Fig. 23. Measured P_{1dB} profile. It meets the blocker profile of the LTE standard at a typical 20 dB front-end gain.

D. Out-of-Band Blocker Tolerability

Another important parameter for wireless applications is the out-of-band blocker tolerability. For this test, the in-band noise is measured against continuous-wave (CW) blockers. The P_{1dB} is defined as the blocker power for which the in-band noise rises by 1 dB compared to its zero-input level. As shown in Fig. 23, the LPF meets the OB blocker profile of the LTE standard at a typical 20 dB front-end gain [20]. The toughest spot is the TX leakage at 41 MHz offset, which already accounts 54 dB duplexer attenuation and an additional value of 5 dB peak-to-average ratio higher than the CW blocker [20].

E. Performance Comparison

The comparison between discrete-time and continuous-time LPFs at different technologies is not straightforward, because they may have different supply voltages, transfer functions and tunable ranges. Here, the following FOM [4], [21] is selected to evaluate the overall performance,

$$\mathrm{FOM} = \frac{\mathrm{P_C/N}}{\mathrm{BW} \cdot (\mathrm{SFDR} \cdot \mathrm{N}^{4/3})} \tag{9}$$

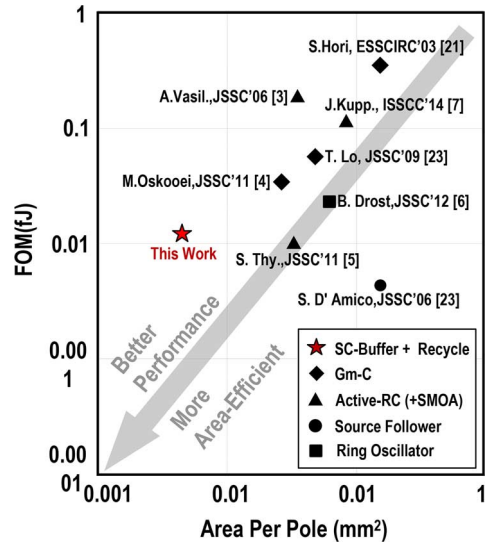


Fig. 24. Performance benchmark with the state-of-the-art.

where N is the number of poles and P_C/N is the normalized power consumption. The spurious-free dynamic range is given by $\mathrm{SFDR_{dB}} = 10\log(\frac{\mathrm{IIP3}}{\mathrm{P_N}})^{(2/3)}$, where P_N is the IRN power.

A comparison of FOM and area-per-pole efficiency with prior art is plotted in Fig. 24. The other LPFs are classified as shown in the inset. Benchmarking with the state-of-the-art Butterworth LPFs [4], [6], [7] is illustrated in Table II, this work achieves 4.7× wider BW tunability, 8× higher area efficiency and 1.5× better FOM. It is important to highlight that in [7] the BW is higher and supply voltage is lower, but the high OB spurs degrade the spectrum purity.

VII. Conclusion

High-speed nanoscale CMOS technologies have stimulated the use of switches and low-gain active elements to rebuild the analog blocks for better scalability, area and power efficiencies. Together with the improved accuracy of capacitor ratioing, this paper introduced a SC-buffer Biquad that can be recycled to build a compact and power-efficient high-order SC LPF. The generated complex poles have independent Qs in each cycle and have low crosstalk. The speed-to-power efficiency, in-/out-of-band linearity and P_{1dB} are inherently high, as no high gain node is involved. Recycling the Biquad once corresponds to a 4th-order Butterworth LPF with 75% buffer utilization, which occupies just 0.02 mm^2 in 65 nm CMOS and exhibits 20x BW tunability (0.5 to 10 MHz) solely tuned by the clock rate (10 to 200 MHz). The achieved FOM at 10 MHz BW is 0.013 fJ.

Appendix

The noise analysis is derived from the basic 1st-order passive-SC LPF as shown in Fig. 25(a). The buffer can be combined with the noise source of the next switch's on-resistance. Supposing that this on-resistance is R_{on1} (R_{on2}) during Φ_1 (Φ_2), the noise equivalent circuits can be obtained, as presented in Fig. 25(b). Since R_{on1} and R_{on2} are independent, the total output noise PSD is the summation of the noises due to R_{on1} and R_{on2}. R_{on1} is never directly connected to the output

TABLE II
BENCHMARK WITH THE STATE-OF-THE-ART BUTTERWORTH LPFS

Parameters	This Work	J. Kuppambatti et al. [7] ISSCC'14	B. Drost et al. [6] JSSC'12	M.S. Oskooei et al. [4] JSSC Jul'11
Technology	65-nm CMOS	65-nm CMOS	90-nm CMOS	90-nm CMOS
Filter Order, Type	4th, Butterworth	4th, Butterworth	4th, Butterworth	6th, Butterworth
Architecture and Key Technique	SC-Buffer Biquad + Recycling	Active-RC + Switched-Mode OTA	Ring-Oscillator Integrator	Continuous-Time Gm-C
BW Range (MHz) and Tunability	0.5 to 10 (20x) (clock rate)	70 (1x) (no tuning)	7 to 30 (4.28x) (supply voltage)	8.1 to 13.5 (1.67x) (capacitor & current)
	@ 10MHz BW	@ 70MHz BW	@ 7MHz BW [1]	@ 10MHz BW *
In-Band IIP3 (dBm) (2-Tone Test @ ~2MHz)	+17.6	+21	+17.7	+22.1
Power Per Pole (mW)	0.68 @ 1.2V	6.55 @ 0.6V	0.73 @ 0.55V	0.73 @ 1V
SFDR (dB)	59.2	51.1	59.16	54.4
IRN (nV/√Hz)	19.5**	43.6	23.6	75
Area Per Pole (mm²)	0.005	0.095	0.073	0.04
FOM (fJ) **	0.013	0.114	0.0198	0.0246
Out-Band Spurs at Full-Scale Input (dB)	<-52.8 (clock feedthrough)	<-32.8 (OTA phase mismatch)	<-65 (PWM phase mismatch)	No

*: Data at maximum BW is not available. **: IRN $\propto 1/\sqrt{f_{\rm clk}}$.

in both phases. Thus, only the sample-and-hold noise will be presented at the output. In the sampling phase [Fig. 25(b), left], the noise PSD due to the on-resistance is $4kT(2\mathrm{R_{on1}})$. The noise charge on $\mathrm{C_S}$ moves to the output in the next transferring phase and this noise is filtered by the RC LPF. As a result, the total noise power on the capacitor $\mathrm{C_S}$ is $kT/\mathrm{C_S}$. The noise on $\mathrm{C_s}$ is under-sampled, and the noise spectrum is folded back from 0 to $f_{\rm clk}$ due to the switch effect resulting in "white" noise. Consequently, the PSD of the output narrow-band noise due to $\mathrm{R_{on1}}$ is equal to the total power divided by $\mathrm{f_{clk}}$ which becomes $\mathrm{S_{R1\_N}}(f) = 2kT/f_{\rm clk}\mathrm{C_s}$.

For the noise originated by $\mathrm{R_{on2}}$, the same procedure can be applied. $\mathrm{R_{on2}}$ is directly connected to the output in the transferring phase, thus the output noise due to it is different in the two phases. The voltage at the input of $\mathrm{C_S}$ in the transferring phase will be settled and hold on $\mathrm{C_i}$ in the sampling phase. Thus, the output noise PSD during the sampling phase is given by $2kT/f_{\rm clk}\mathrm{C_{eq}}$ ($\mathrm{C_{eq}} = \dfrac{\mathrm{C_S C_i}}{\mathrm{C_S + C_i}}$). The output noise in the transferring phase can be divided into two parts: narrow-band sampled noise and continuous direct noise. For the sampled noise, the sampled voltage on $\mathrm{C_i}$ will be shared with $\mathrm{C_S}$ during the transferring phase. As a result, we can get

$$\mathrm{S_{R2T\_N}}(f) = \frac{2kT}{f_{\rm clk}\mathrm{C_{eq}}}\left(\frac{\mathrm{C_i}}{\mathrm{C_S + C_i}}\right)^2. \tag{10}$$

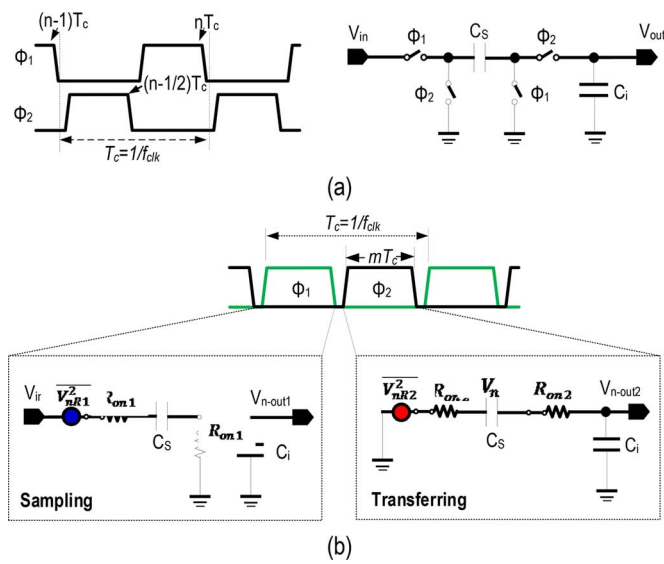


Fig. 25. (a) 1st-order passive-SC LPF without buffer. (b) Noise source in both phases.

Another continuous direct noise is given by

$$\mathrm{S_{R2C\_N}}(f) = 4kT(2\mathrm{R_{on2}})\left|\frac{1}{1+\mathrm{s}\,(2\mathrm{R_{on2}C_{eq}})}\right|^2\left(\frac{\mathrm{C_S}}{\mathrm{C_S+C_i}}\right)^2. \tag{11}$$

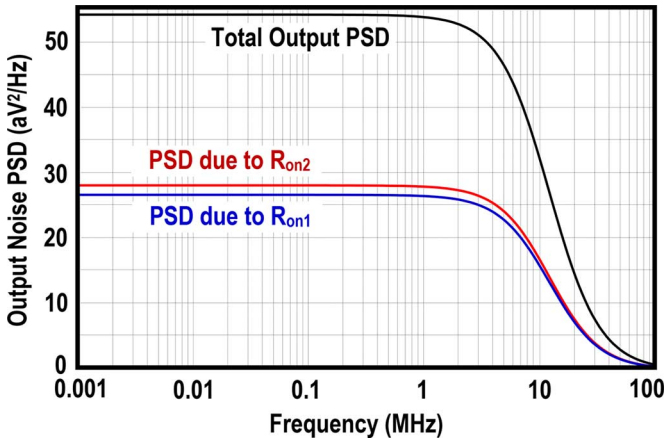


Fig. 26. Simulated output noise PSD of a 1st-order passive-SC LPF.

Recalling that Φ_2 lasts $m\mathrm{T_c}$ $(0 < m < 0.5)$, the noise in the corresponding phase should be multiplied by this factor. Thus, the sampled noise after multiplying by the power transfer function of the filter is given by

$$|H_1(j\omega)|^2 = \left| \frac{1-\mathrm{e}^{-j\omega \mathrm{T}}}{j\omega \mathrm{T}} \frac{\dfrac{\mathrm{C_S}}{\mathrm{C_S}+\mathrm{C_i}}\mathrm{e}^{-j\omega \mathrm{T}/2}}{1-\dfrac{\mathrm{C_i}}{\mathrm{C_S}+\mathrm{C_i}}\mathrm{e}^{-j\omega \mathrm{T}}} \right|^2. \quad (12)$$

The total output thermal-noise PSD $\mathrm{S_{Total\_N}}(f)$ of a 1st-order passive-SC LPF can be obtained by adding the uncorrelated PSDs together:

$$\mathrm{S_{Total\_N}}(f) = [\mathrm{S_{R1\_N}}(f) + (1-m)\mathrm{S_{R2S\_N}}(f) + m\mathrm{S_{R2T\_N}}(f)] \cdot |H(j\omega)|^2 + (1-m)\mathrm{S_{R2C\_N}}(f). \quad (13)$$

From (13), only the last term is related to the switch's on-resistance, which is the minor contributor of the total output noise. The dominated noise is the narrow-band sample-and-hold noise. The output noise PSD is dominated by $\mathrm{C_S}$ from (13) for $\mathrm{C_i} > \mathrm{C_S}$ (in most of the cases). Supposing that $f_{\mathrm{clk}} = 200$ MHz is selected, $\Phi_1 = \Phi_2 = 0.45\mathrm{T_c}$ and BW $= 10$ MHz, $\mathrm{C_S}$ and $\mathrm{C_i}$ can be chosen as 1.5 and 4 pF, respectively. The calculated output noise power is 57.5 aV^2/Hz, at low frequency, shaped by the filter's transfer function and matching well the simulation (Fig. 26).

To extend the noise analysis to the proposed SC-buffer Biquad, Fig. 3 is recalled. The output resistance $\mathrm{R_{o1}}$ of the buffer can be treated as part of the switch's on-resistance, and the flicker noise induced by the buffer $\mathrm{B_2}$ only crams at low frequency. If $\mathrm{V_{outb}}$ serves as the output of the Biquad, the flicker noise and the low frequency thermal noise induced by $\mathrm{B_2}$ will be filtered out by $\mathrm{C_{i1}}$ in the proposed architecture. By applying the same procedure, the output noise PSD $(\mathrm{V_{outb}})$ of this Biquad can be obtained,

$$\mathrm{S_{T\_B}}(f) = [\mathrm{S_{T1}}(f) + \mathrm{S_{T2}}(f)]|H_2(\mathrm{e}^{j\omega})|^2|\mathrm{H_{ZOH}}(j\omega)|^2 + (1-m)\mathrm{S_{R2C2\_N}}(f) \quad (14)$$

where $H_2(\mathrm{e}^{j\omega})$ is the transfer function of the Biquad as stated in (3). $\mathrm{H_{ZOH}}(j\omega)$ is the transfer function of the zero-order hold, and $\mathrm{S_{R2C2\_N}}(f)$ is the continuous output noise PSD caused by the switch's on-resistance linked to $\mathrm{C_{S2}}$ when Φ_2 is high. $\mathrm{S_{T1}}(f)$ and $\mathrm{S_{T2}}(f)$ are the noise PSDs introduced by the first and second SC branches, respectively:

$$\mathrm{S_{T1}}(f) = \mathrm{S_{R1\_N1}}(f) + (1-m)\mathrm{S_{R2S\_N1}}(f) + m\mathrm{S_{R2T\_N1}}(f) \quad (15)$$

$$\mathrm{S_{T2}}(f) = \mathrm{S_{R1\_N2}}(f) + (1-m)\mathrm{S_{R2S\_N2}}(f) + m\mathrm{S_{R2T\_N2}}(f) + \mathrm{S_{flicker}}(f) \quad (16)$$

where $\mathrm{S_{flicker}}(f)$ is the flicker noise caused by the buffer $\mathrm{B_2}$. If the Biquad is recycled to build a higher order LPF, the above noise analysis is still valid with modification of $0 < m < 0.25$ because $\Phi_1, \Phi_2, \Phi_3, \Phi_4$ is a 25%-duty-cycle clock. The increase of the output noise PSD is minor if (14) is used. For instance, for the Biquad, the simulated output-noise PSD caused by $\mathrm{R_{on2}}$ will be raised from 28.6 to 31.3 aV^2/Hz, if the clock is reduced from 50% to 25% duty cycle.

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