Resolution-enhanced sturdy MASH delta–sigma modulator for wideband low-voltage applications

Liang Qi, Sai-Weng Sin✉, Seng-Pan U and Rui Paulo Martins

A resolution-enhanced sturdy multi-stage noise shaping (MASH) delta–sigma modulator is presented. By employing the Leslie-Singh architecture in the first stage and an appropriate second stage digital filtering, the proposed structure could achieve much higher resolution [>80 dB signal-to-quantisation noise ratio] when compared with a traditional sturdy MASH, at a lower oversampling ratio (e.g. 8X). Interestingly, the mismatch between digital and analogue transfer functions is inherently shaped so that the structure is not sensitive to opamp finite gain error. Both these properties make the proposed structure suitable for wideband low-voltage applications. Behavioural simulations are presented to demonstrate the effectiveness of the proposed structure when compared with the prior art of its high performance delta–sigma counterparts.

Introduction: The increasing demand of faster data rates for modern standards of wireless communication systems translates into higher bandwidth requirements for analogue-to-digital converters. Multi-stage noise shaping (MASH) type delta–sigma modulators (DSMs) are suitable candidates for high resolution wideband applications. When compared with the single-loop DSM, the MASH structure avoids the stability problems associated with high-order noise shaping. However, MASH structures are sensitive to the mismatch between analogue and digital filters, leading to quantisation noise leakage. To suppress the leakage, high-gain opamps are always necessary (and often implemented as a 2-stage opamp), which implies stringent stability–power–bandwidth trade-offs in nanometre CMOS designs.

A sturdy MASH (SMASH) structure completely avoids the noise leakage by removing the digital filter, thus alleviating the need for high-gain opamps [1]. Fig. 1 depicts the block diagram of the traditional SMASH structure. The final output of this structure is given by

$$Y_{\mathrm{SMASH}} = \mathrm{STF}_1 X + \mathrm{NTF}_1(1-\mathrm{STF}_2)E_1 - \mathrm{NTF}_1\mathrm{NTF}_2 E_2 \quad (1)$$

where STF_i, NTF_i and E_i represent the signal transfer function, noise transfer function and quantisation error of the ith loop, respectively. Through choosing $\mathrm{STF}_2 = 1 - \mathrm{NTF}_2$, E_1 could be shaped with the same order of E_2 (instead of fully cancelled as in a normal MASH). With the same number of bits for both quantisers, this would increase the noise power at the final output by 3 dB when compared with the normal MASH (assuming E_1 and E_2 are uncorrelated).

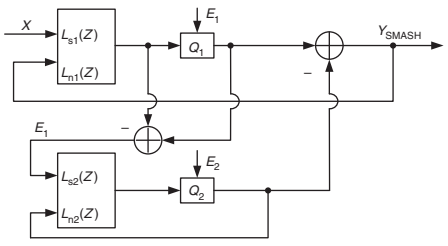

Fig. 1 *Block diagram of traditional SMASH structure*

However, the above general design for the SMASH is difficult regarding achieving high resolution with higher bandwidth, since the overall performance is limited by both quantisation errors. Further suppression for E_2 may be obtained by adding an inter-stage gain or utilising noise coupling techniques (without affecting the original STF_2) [2], but the performance would still be limited by the quantisation error E_1.

Proposed SMASH structure: This Letter presents a resolution-enhanced SMASH structure intended for wideband, low-voltage applications, which explores the underlying ability of the SMASH structure to achieve higher resolution at a lower oversampling ratio (OSR). Since both E_1 and E_2 exist in the overall output, E_1 and E_2 must be suppressed together to further boost the overall signal-to-quantisation noise ratio (SQNR). As illustrated in Fig. 2, the proposed SMASH structure is modified from the basis of the traditional SMASH structure. In the first loop, by employing the Leslie-Singh architecture [3], the outputs of the M-bit high resolution quantiser are divided into MSB segments (M_{MSB}-bits) and LSB segments (M_{LSB}-bits). The MSBs are directly fed back to the modulator input and the LSBs are digitally post-processed. Ideally, E_1 would be further suppressed by the extended bits (M_{LSB}-bits) even if it is not fed back. However, the normal digital post-processing in the Leslie-Singh structure (denoted by H_1 in Fig. 2) cannot be directly applied due to the different transfer function characteristic in the SMASH structure. To cater for this change, here we propose to add an extra digital filter H_2. Meanwhile, in the second loop, E_2 would be further suppressed by employing the noise coupling technique and inserting an appropriate inter-stage gain G.

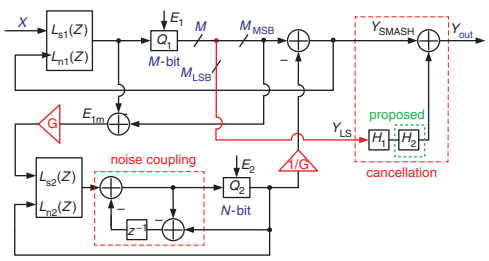

Fig. 2 *Block diagram of proposed SMASH structure*

The final output could be deduced as follows:

$$Y_{\mathrm{SMASH}} = \mathrm{STF}_1 X + \mathrm{NTF}_1(1-\mathrm{STF}_2)E_{1m} - \mathrm{NTF}_1\mathrm{NTF}_2 E_2 \quad (2)$$

$$Y_{\mathrm{LS}} = -E_{1m} + E_1 \quad (3)$$

$$Y_{\mathrm{out}} = Y_{\mathrm{SMASH}} + Y_{\mathrm{LS}} H_1 H_2, \quad \text{where } H_1 = \mathrm{NTF}_1, \; H_2 = 1 - \mathrm{STF}_2 \quad (4)$$

Here E_{1m} is the quantisation noise with respect to the M_{MSB}-bits and E_1 is the quantisation noise with respect to the full M bits. Since the LSB segments are an extended quantisation of its MSB counterpart's quantisation error E_{1m} and given by (3), the amplitude of E_{1m} is much larger than E_1. Fortunately, with a proposed extra digital filter H_2, E_{1m} could be completely cancelled in the final output. Also, as mentioned before, in traditional SMASH structures, $1-\mathrm{STF}_2$ is generally selected to be NTF_2 (typically, $1-\mathrm{STF}_2 = (1-z^{-1})^2$). However, in the proposed structure, with the help of the noise coupling technique, NTF_2 would be immediately increased by one more order while $1-\mathrm{STF}_2$ is not affected. Thus, NTF_2 could be expressed as $(1-\mathrm{STF}_2)(1-z^{-1})$. Then, with an ideal matching between the analogue and digital filters, the final output Y_{out} is given by

$$\begin{aligned} Y_{\mathrm{out}} &= \mathrm{STF}_1 X + \mathrm{NTF}_1(1-\mathrm{STF}_2)E_1 - (1/G)\mathrm{NTF}_1\mathrm{NTF}_2 E_2 \\ &= \mathrm{STF}_1 X + \mathrm{NTF}_1(1-\mathrm{STF}_2)E_1 - (1/G)\mathrm{NTF}_1(1-\mathrm{STF}_2)(1-z^{-1})E_2 \end{aligned} \quad (5)$$

As illustrated in (5), in terms of the whole transfer function and quantisation bits for both E_1 and E_2, E_2 would be further suppressed as a result of one extra order from the noise coupling and scaling gain $1/G$ while E_1 would be further suppressed by the extra number of bits ($M_{\mathrm{MSB}} + M_{\mathrm{LSB}} - N$). Assuming L is the shaped order of E_1's coefficient NTF_1 $(1-\mathrm{STF}_2)$ in (5), then E_2 has the corresponding shaped order of $L+1$ due to the noise coupling mechanism. Hence, with further reduction for both and to keep them still similar, the following equation should be satisfied

$$\begin{aligned} &10\lg\left[\frac{(2L+1)\mathrm{OSR}^{2L+1}}{\pi^{2L}}\right] + 6.02(M_{\mathrm{MSB}} + M_{\mathrm{LSB}}) + 1.76 \\ &= 10\lg\left[\frac{(2(L+1)+1)\mathrm{OSR}^{2(L+1)+1}}{\pi^{2(L+1)}}\right] + 10\lg G^2 + 6.02N + 1.76 \end{aligned} \quad (6)$$

Then, (6) could be further simplified to be

$$10\lg\left[\frac{\mathrm{OSR}^2(2L+3)G^2}{\pi^2(2L+1)}\right] = 6.02(M_{\mathrm{MSB}} + M_{\mathrm{LSB}} - N) \quad (7)$$

Consequently, in order to achieve a target SQNR in a specific wideband application, it is important to choose appropriate values for various parameters in (7), while considering the corresponding trade-offs for implementing these values at the circuitry level.

Transfer function mismatch analysis: The structure of Fig. 2 can be challenged because by introducing the digital cancelling mechanism H_1 and H_2 to eliminate E_{1m} it would completely destroy the advantages of the traditional SMASH due to the mismatch. Interestingly, such mismatch is also shaped in the proposed structure, making the implementation very robust. Owing to the mismatch between analogue and digital functions, the E_{1m} with larger amplitude would not be completely eliminated in the final output. As a result, the actual Y_{out} can be given by

$$Y_{\text{out}} = \text{STF}_{1a}X + \text{NTF}_{1d}(1 - \text{STF}_{2d})E_1 - (1/G)\text{NTF}_{1a}\text{NTF}_{2a}E_2 - [\text{NTF}_{1d}(1 - \text{STF}_{2d}) - \text{NTF}_{1a}(1 - \text{STF}_{2a})]E_{1m} \quad (8)$$

where the subscripts 'a' and 'd' denote analogue and digital transfer functions, respectively. As shown in (8), the last term corresponds to the E_{1m} leakage, and, interestingly, it can be transformed as follows:

$$\begin{aligned}&[\text{NTF}_{1d}(1 - \text{STF}_{2d}) - \text{NTF}_{1a}(1 - \text{STF}_{2a})]E_{1m}\\ &= \text{NTF}_{1d}(1 - \text{STF}_{2d})E_{1m} - \text{NTF}_{1a}(1 - \text{STF}_{2d} + \text{STF}_{2d} - \text{STF}_{2a})E_{1m}\\ &= (1 - \text{STF}_{2d})(\text{NTF}_{1d} - \text{NTF}_{1a})E_{1m} - \text{NTF}_{1a}(\text{STF}_{2d} - \text{STF}_{2a})E_{1m}\\ &= (1 - \text{STF}_{2d})L_{\text{N}} - \text{NTF}_{1a}L_{\text{S}} \quad (9)\end{aligned}$$

Here L_{N} denotes $(\text{NTF}_{1d} - \text{NTF}_{1a})\ E_{1m}$, which is the portion of E_{1m} leakage caused by the mismatch between NTF_{1d} and NTF_{1a}. L_{S} denotes $(\text{STF}_{2d} - \text{STF}_{2a})\ E_{1m}$, which is the other portion of the E_{1m} leakage caused by the mismatch between STF_{2d} and STF_{2a}. Obviously, as stated in (9), the noise leakages L_{N} and L_{S} are now shaped by $(1 - \text{STF}_{2d})$ and NTF_{1a}, respectively. This significantly mitigates the matching requirements between the analogue and digital filters, thus further relaxing the open-loop DC gain requirement for the opamps.

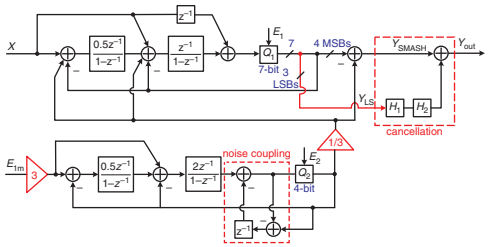

Fig. 3 *Implementation of proposed SMASH structure*

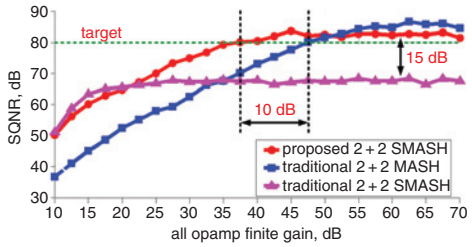

Fig. 4 *SQNR against all opamp finite gain*

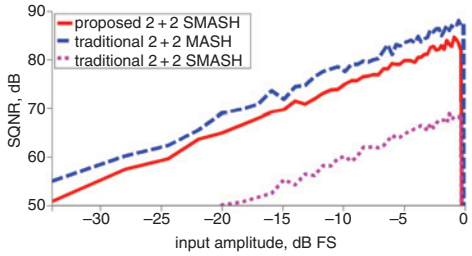

Fig. 5 *SQNR against input amplitude*

Simulation results: A typical implementation of the proposed SMASH modified by a traditional 2 + 2 SMASH [4] is shown in Fig. 3. The poles of NTF_1 are not located at zero for better stability [4], but this does not affect the theoretical analysis presented in this Letter. With the guideline from (7), to achieve 80 dB SQNR with OSR = 8, an M = 7b quantiser with M_{MSB} = 4b DAC feedback and M_{LSB} = 3b are used, while in the second stage an N = 4b quantiser is utilised. The inter-stage gain is set as G = 3. An input signal with −2 dB FS was applied and a reference of [−1 1] was used. The sensitivity of the proposed structure to finite opamp gain errors (for all the integrators) was analysed with MATLAB and compared with the traditional 2 + 2 MASH (with both 4b quantisers), as well as traditional 2 + 2 SMASH (with both 4b quantisers). Note that the inter-stage gain G = 3 was also applied in the other two structures, as well as the noise coupling technique. Fig. 4 illustrates SQNR against the all opamps DC gain. Obviously, the proposed SMASH structure is much more robust against the finite gain errors of the opamps while achieving at least 80 dB SQNR. Moreover, Fig. 5 shows the achieved SQNR against the input amplitude with 80 dB opamp DC gain. The proposed 2 + 2 SMASH structure saturates a little earlier when compared with the traditional 2 + 2 MASH. This is caused by the direct feedback from the output of the second loop to the input of the first loop.

Conclusion: An improved topology of the SMASH architecture is proposed. Combining the Leslie-Singh architecture and the traditional SMASH topology with the extra proposed digital filtering, larger SQNR could be achieved with lower OSR, which is suitable for medium-resolution wideband applications. Moreover, the overall output is inherently insensitive to mismatch between the analogue and digital transfer functions. This can significantly relax the opamp gain requirements, thus allowing lower-power, lower-voltage implementation. Simulation results demonstrate its effectiveness and robustness to the variation of opamp DC gain, while achieving at least 80 dB SQNR with 8X-OSR.

Acknowledgments: This work was financially supported by the Research Committee of the University of Macau and the Macao Science & Technology Development Fund (FDCT) under FDCT/055/2011/A2.

Submitted: *13 May 2015* E-first: *25 June 2015*
doi: 10.1049/el.2015.1655
One or more of the Figures in this Letter are available in colour online.

Liang Qi, Sai-Weng Sin, Seng-Pan U and Rui Paulo Martins (*State-Key Laboratory of Analog and Mixed-Signal VLSI and Department of ECE, FST, University of Macau, Macao, People's Republic of China*)

✉ E-mail: terryssw@umac.mo

Seng-Pan U: Also with Synopsys Macau Ltd, Macao, China

Rui Paulo Martins: On leave from Instituto Superior Técnico (IST)/Universidade de Lisboa, Lisboa, Portugal

References

1 Maghari, N., Kwon, S., Temes, G.C., and Moon, U.: 'Sturdy MASH ΔΣ modulator', *Electron. Lett.*, 2006, **42**, pp. 1269–1270
2 Lee, K., Bonu, M., and Temes, G.: 'Noise-coupled ΔΣ ADCs', *Electron. Lett.*, 2006, **42**, p. 1381
3 Lee, C.C., Alpman, E., Weaver, S., Lu, C.-Y., and Rizk, J.: 'A 66 dB SNDR 15 MHz BW SAR assisted ΔΣ ADC in 22 nm tri-gate CMOS'. Proc. of Symp. on VLSI Circuits, Dig. Tech. Pap., Kyoto, Japan, June 2013, pp. C64–C65
4 Maghari, N., Kwon, S., and Moon, U.-K.: '74 dB SNDR multi-loop sturdy-mash delta–sigma modulator using 35 dB open-loop opamp gain', *IEEE J. Solid-State Circuits*, 2009, **44**, (8), pp. 2212–2221