

# 0.0045 mm<sup>2</sup> 15.8 μW three-stage amplifier driving 10x-wide (0.15–1.5 nF) capacitive loads with >50° phase margin

Zushu Yan, Pui-In Mak<sup>✉</sup>, Man-Kay Law and Rui Paulo Martins

A three-stage amplifier employing embedded capacitor-multiplier compensation (ECMC) and active parallel compensation (APC) to enhance the area efficiency when driving nF-range capacitive loads ( $C_L$ ) is presented. Unlike the conventional current-buffer Miller compensation, ECMC applied to the dominant compensation path saves substantial power and area, while securing a large gain-bandwidth product. The created left-half-plane zero also benefits the phase margin (PM). For the APC, unlike the traditional passive parallel compensation, this work benefits from the Miller effect to avoid the area-consuming resistor, and reduces the entailed capacitances without lowering the parasitic pole position. A multi-path  $G_m$ -boosting second stage enhances the effective transconductance and DC gain. With 0.0045 mm<sup>2</sup> of area and 15.8 μW of power, the 0.18 μm CMOS three-stage amplifier measures 1.13 MHz unity-gain frequency, 0.41 V/μs average slew rate and 56.2° PM at 1 nF  $C_L$ . Stable responses with >50° PM are attained for a  $10 \times$  range of  $C_L$  from 0.15 to 1.5 nF. The achieved figure-of-merit accounting for both die area and power compares favourably with the state of the art.

**Introduction:** For flat-panel-display applications that demand thousands of buffer amplifiers [1], three-stage amplifiers have been continuously evolved for better small-/large-signal performances, area efficiency and  $C_L$  drivability [2, 3]. However, they suffer from inherent drawbacks. The amplifier in [2] is managed to balance power efficiency and  $C_L$  drivability, but area-hungry passive components are entailed to boost the current buffer's transconductance and generate the desired left-right-plane (LHP) zero. The design in [3] relies on an extra local feedback loop (LFL) [2] to move up the parasitic poles in the LHP zero circuit, but the LFL stability becomes very sensitive to the parasitics, and passive components are still unavoidable.

This Letter describes the techniques to realise an ultra-area-efficient nF- $C_L$  three-stage amplifier. It benefits from the combinatorial effects of embedded capacitor-multiplier compensation (ECMC), active-parallel compensation (APC) and multi-path  $G_m$  boosting technique to optimise the performance.

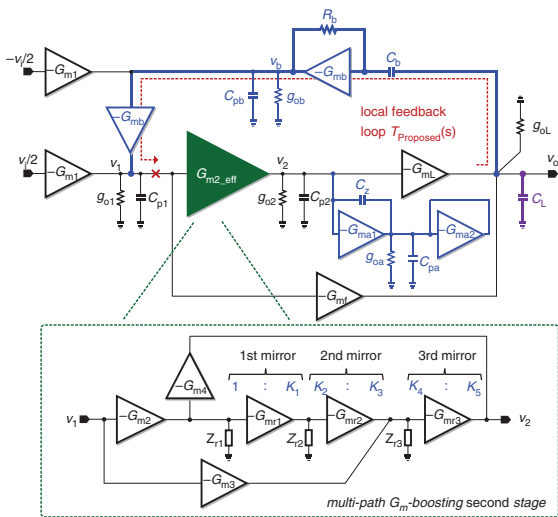


Fig. 1 Proposed three-stage amplifier

**Topology:** The proposed three-stage amplifier is depicted in Fig. 1. The CBMC in the dominant LFL [2] is replaced by an embeddable CM to realise ECMC; its small-signal behaviour is characterised by  $R_b$ ,  $C_b$ , and two  $G_{mb}$  stages, whereas  $g_{ob}$  and  $C_{pb}$  are the output conductance and parasitic capacitance, respectively. The two  $G_{m1}$  stages represent the differential inputs. Part of the  $-v_i/2$  input signal travelling through the above  $G_{m1}$  leaks to  $v_o$  via  $R_b$  and  $C_b$  which is in-phase with the other  $-v_i/2$  and  $v_i/2$  signals passing the main gain stages. The in-phase sum of these signals creates a useful LHP zero. The second stage is non-

inverting characterised by  $G_{m2\_eff}$ . It is a new multi-path  $G_m$ -boosting structure to enhance the transconductance and DC gain with high power efficiency. The feedforward stage  $G_{mf}$  with  $G_{mL}$  forms a push-pull output stage to improve the large-signal behaviour. The APC is attached at  $v_2$ . Alternatively, it can be positioned at  $v_1$ , but practical considerations for pushing up the parasitic pole created by the APC renders the connection of APC at  $v_2$  better. Note that when locating APC at  $v_1$ , the  $(G_{ma1} + G_{ma2})/(C_{p1} + C_{pa})$  pole is lower than  $(G_{ma1} + G_{ma2})/(C_{p2} + C_{pa})$  if located at  $v_2$  because  $C_{p1} > C_{p2}$ :  $G_{m1}$  is loaded by  $G_{m2\_eff}$  and  $G_{mf}$  while  $G_{m2\_eff}$  is only loaded by  $G_{mL}$ ;  $G_{mL}$  ( $G_{mf}$ ) is typically implemented by an NMOS (PMOS) device.

**LFL analysis and transfer functions:** LFL analysis is an insightful method guiding the pole-zero placements [2]. With the assumptions: (i) the DC gain of all the stages is  $\gg 1$ ; (ii)  $C_{p1,2}$ ,  $C_{pa,b} \ll C_{b,z} \ll C_L$ ; (iii)  $g_{ob} \ll 1/R_b < G_{mb}$ , the LFL transfer function of the amplifier is given by

$$T_{Proposed}(s) \simeq \frac{-sG_{m2\_eff}G_{mL}(G_{mb}R_b - 1)C_b}{g_{o1}g_{o2}g_{oL}(1 + (s/\omega_{p1}))(1 + (s/\omega_{p2}))} \times \left[ 1 + 2\zeta_{CM} \left( \frac{s}{\omega_{p3}} \right) + \left( \frac{s}{\omega_{p3}} \right)^2 \right] \left( 1 + \frac{s}{\omega_{p4}} \right) \quad (1)$$

where  $\omega_{p1}$  is  $g_{oL}/C_L$ .  $\omega_{p2}$  and  $\omega_{p4}$  associated with ACP are  $(G_{ma2}g_{o2})/[(G_{ma1} + G_{ma2})C_z]$  and  $(G_{ma1} + G_{ma2})/(C_{p2} + C_{pa})$ , respectively.  $\zeta_{CM}$  and  $\omega_{p3}$  correspond to the damping factor and natural frequency of the complex poles that are attributed to the embeddable CM. During the derivation, the influence of  $G_{mf}$  is negligible though it slightly shifts the position of the  $G_{ma2}/C_z$  zero and introduces another very high-frequency LHP zero; the  $G_{ma2}/C_z$  zero has been employed to cancel the  $g_{o1}/C_{p1}$  pole. Consequently, the UGF of the LFL,  $\omega_{\mu,Proposed}$ , is obtained in Fig. 2.

Since  $\omega_{\mu,Proposed}$  constitutes the first non-dominant pole of the overall transfer function [2], it should be placed at the highest possible frequency while managing to save power. The proposed topology can achieve a large  $\omega_{\mu,Proposed}$  in two power-efficient ways: (i) an extra boosting factor  $(G_{mb1}R_b - 1)C_b/C_{p1}$  is introduced when compared with that in [3], reducing the required  $G_{mL}$ ; (ii) the multi-path second-stage  $G_{m2\_eff}$  concurrently reduces the power budget of itself and  $G_{mL}$  while allowing a relatively large  $G_{ma1}$  to preserve the LFL stability. As the  $g_{o1}/C_{p1}$  pole is higher than its counterpart in [3], the pole-zero cancellation in the LFL appears at a higher frequency and permits shrinking  $C_z$  for area savings. The variability of  $C_L$  can be assessed by evaluating the LFL gain responses. As illustrated in Fig. 2,  $\omega_{p1}$  decreases when  $C_L$  is increased, while all other poles remain fixed. Since the mid-band LFL gain (LG) is also reduced,  $\omega_{\mu,Proposed}$  follows. Thus, a large  $C_L$  benefits the LFL stability, but deteriorating the amplifier's PM (i.e. the upper bound of  $C_L$ ). When  $C_L$  is reduced,  $\omega_{\mu,Proposed}$  approaches  $\omega_{p3}$  and  $\omega_{p4}$  degrading the PM of the LFL. Thus, the lower bound of the  $C_L$  is limited by the LFLs PM. The proposed amplifier employs the embeddable CM and APC that can locate their parasitic poles higher than those based on current buffers and/or conventional PC at equal power [2, 3]. The  $C_L$  drivability is therefore extended to smaller values. The transfer function of the amplifier is given by

$$A_{Proposed}(s) \simeq \frac{A_0(1 + (s/\omega_{z1}))}{(1 + (s/\omega_{pd}))(1 + (s/\omega_{\mu,Proposed}))} \times \left[ 1 + 2\zeta_{CM} \left( \frac{s}{\omega_{p3}} \right) + \left( \frac{s}{\omega_{p3}} \right)^2 \right] \left( 1 + \frac{s}{\omega_{p4}} \right) \quad (2)$$

where  $A_0$  and the dominant pole  $\omega_{pd}$  correspond to  $G_{m1}G_{m2\_eff}G_{mL}/(g_{o1}g_{o2}g_{oL})$  and  $g_{o1}g_{o2}g_{oL}/[G_{m2\_eff}G_{mL}(G_{mb}R_b - 1)C_b]$ , respectively. The GBW is given by  $G_{m1}/(G_{mb}R_b - 1)C_b$ . The LHP zero  $\omega_{z1} = 2G_{mb}/[(G_{mb}R_b + 1)C_b]$  counteracts the negative phase shift from the non-dominant poles of  $A_{Proposed}(s)$ , extending the large  $C_L$  drivability.

**Multi-path  $G_m$ -boosting second stage:** Two power-saving ideas are involved to enhance  $G_{m2\_eff}$  and its output resistance: (i) it cascades multiple wideband amplifiers that are realised by small-ratio current mirrors to attain significant transconductance enhancement and (ii) it recycles the current that biases the current mirrors to form a multi-path structure contributing to  $G_{m2\_eff}$ . Unlike the typical single-current-mirror realisation [2, 3], the output resistance of  $G_{m2\_eff}$  here is naturally increased,

as much less current is distributed to the last mirror. Fig. 1 shows the block-diagram model of  $G_{m2\_eff}$  that exploits three-cascaded current mirrors and two feedforward paths. The boosted  $G_{m2\_eff}$  is

$$G_{m2\_eff} = \left( \frac{K_5 K_3}{K_4 K_2} K_1 + K_5 \right) G_{m2} + \frac{K_5}{K_4} G_{m3} \quad (3)$$

where  $K_5$  is the ratio of  $G_{m4}$  to the conductance part of  $Z_{r1}$  that models the input impedance of the first mirror. Although the noise of the current mirrors is also raised by transconductance amplification, the amplifier's noise performance is almost unaffected since the multi-path  $G_m$ -boosting is enforced in the second stage.

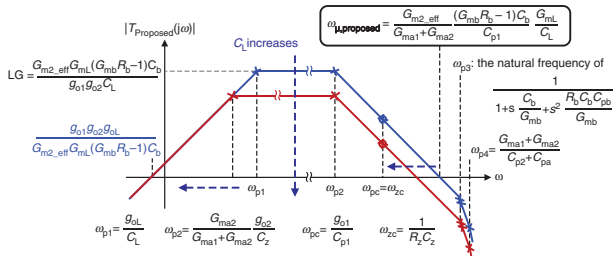


Fig. 2 Magnitude responses of LFL  $T_{Proposed}(s)$

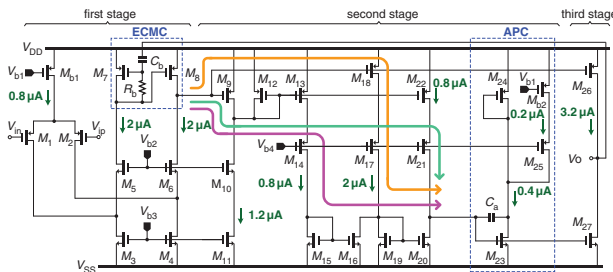


Fig. 3 Schematic of proposed three-stage amplifier

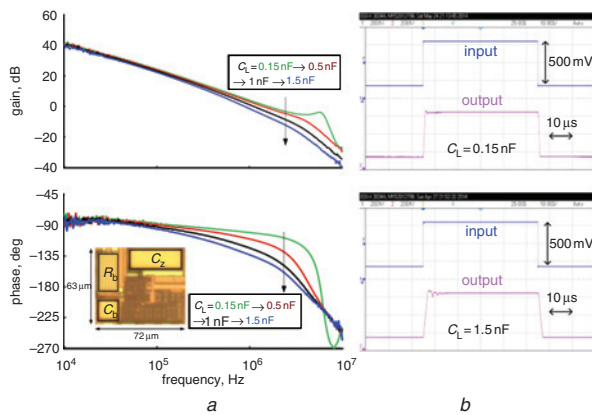


Fig. 4 Measured performance of 0.18  $\mu\text{m}$  CMOS amplifier (inset)  
a AC responses at  $C_L = 0.15, 0.5, 1$  and  $1.5$  nF  
b 500 mV-step responses at  $C_L = 0.15$  and  $1.5$  nF

**Schematic:** The schematic of the amplifier is shown in Fig. 3. The input stage,  $G_{m1}$ , is realised with a folded cascode transconductor ( $M_1$ – $M_8$  and  $M_{b1}$ ). Together with  $R_b$  and  $C_b$ ,  $M_{7-8}$  implement the two  $G_{mb}$  stages constituting the embeddable CM.  $M_9$ – $M_{22}$  form the multi-path  $G_m$ -boosting stage to implement  $G_{m2\_eff}$ . Highlighted in Fig. 3 are the three signal paths that contribute to  $G_{m2\_eff}$ : (i)  $M_9$  ( $G_{m2}$ ), the PMOS current mirror ( $M_{12-13}$ ) with  $M_{13}$  realising  $G_{mr1}$ ; (ii)  $M_{18}$  ( $G_{m3}$ ) and the mirror ( $M_{19-20}$ ) with  $M_{20}$  being  $G_{mr3}$ , and the two NMOS mirrors ( $M_{15-16}$  and  $M_{19-20}$ ) with  $M_{16}$  implementing  $G_{mr2}$ ; (iii)  $M_9$ , the mirror ( $M_{12-22}$ ) with  $M_{22}$  ( $G_{m4}$ ) recycling  $M_{20}$ 's current. APC is composed of  $M_{23}$ – $M_{25}$ ,  $M_{b2}$  and  $C_z$ .  $M_{23}$  acts as  $G_{ma1}$  and  $M_{24}$  plays the role of  $G_{ma2}$ .  $M_{24}$  is bypassed by the cascode current source formed by  $M_{b2}$  and  $M_{25}$ , easing the sizing of  $M_{24}$  to obtain large active resistance  $1/G_{ma2}$  and minimising the parasitic  $C_{pa}$ .  $M_{26}$  serves as  $G_{mf}$  while the output stage  $G_{mL}$  is realised by  $M_{27}$ .

**Experimental results:** The amplifier was fabricated in 0.18  $\mu\text{m}$  CMOS (Fig. 4a). At the typical  $C_L = 1$  nF, the amplifier shows a 1.13 MHz UGF at 56.2° PM. When  $C_L$  is reduced to 0.15 nF, both UGF and PM are increased to 1.6 MHz and 76.7°, respectively. When  $C_L$  is enlarged to 1.5 nF, the UGF is still 0.89 MHz with PM = 50°. Within  $C_L = 0.15$ – $1.5$  nF, the average SR reduces from 0.76 to 0.28 V/ $\mu\text{s}$ , while the 1% settling time is increased from 2.12 to 5.35  $\mu\text{s}$  (Fig. 4b). Table 1 gives the chip summary and benchmarks it with a recent work [3]. This work shows comparable UGF and SR while succeeding in reducing the die area.

Table 1: Performance summary and comparison

	[3] ISSCC'14	This work		
Load $C_L$ , nF	0.5	0.15	1	1.5
UGF, MHz	1.34	1.60	1.13	0.89
Phase margin, deg	52.7	76.7	56.2	50.0
Gain margin, dB	N/A	4.04	15.2	17.4
Average SR, V/ $\mu\text{s}$	0.62	0.76	0.41	0.28
Average $T_S$ , $\mu\text{s}$	0.62	2.16	3.87	5.34
DC gain, dB (extrapolated)	>100	>100		
Power, $\mu\text{W}$ at $V_{DD}$ , V	6.3 at 0.9	15.8 at 1.2		
Total capacitance $C_t$ and resistance $R_t$ , pF, M $\Omega$	0.87, 0.253	1, 0.125		
Chip area, $\text{mm}^2$	0.007	0.0045		
CMOS technology, $\mu\text{m}$	0.18	0.18		
FOM <sub>S</sub> [(MHz·pF)/( $\mu\text{W}\cdot\text{mm}^2$ )]	15 193	3376	15 893	18 776
FOM <sub>L</sub> [(V/ $\mu\text{s}\cdot\text{pF})/(\mu\text{W}\cdot\text{mm}^2)$ ]	7029	1603	5767	5907
IFOM <sub>S</sub> [(MHz·pF)/( $\mu\text{A}\cdot\text{mm}^2$ )]	13 673	4051	19 702	22 532
IFOM <sub>L</sub> [(V/ $\mu\text{s}\cdot\text{pF})/(\mu\text{A}\cdot\text{mm}^2)$ ]	6327	1924	6920	7089

Note: FOM<sub>S</sub> = (UGF· $C_L$ )/(power·area); FOM<sub>L</sub> = (SR· $C_L$ )/(power·area); IFOM<sub>S</sub> = (UGF· $C_L$ )/(static current·area); IFOM<sub>L</sub> = (SR· $C_L$ )/(static current·area).

**Conclusion:** This Letter has proposed ECMC, APC and multi-path  $G_m$ -boosting techniques to realise a novel ultra-compact  $10\times$ -wide nF- $C_L$  three-stage amplifier suitable for flat-panel-display applications. ECMC applied to the dominant compensation path saves substantial power and area, while securing a large GBW. The LHP zero also benefits the PM. For the APC, it benefits from the Miller effect to avoid the area-consuming resistor, and reduces the entailed capacitances without lowering the parasitic pole position.

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