

An RF-to-BB-Current-Reuse Wideband Receiver With Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF

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Abstract—N-path passive-mixer-first receivers suffer from a tight tradeoff between noise figure (NF), linearity and power due to no RF gain. This paper describes an extensively-current-reuse wideband receiver exploiting parallel N-path active/passive mixers. The key features are: 1) a *stacked RF-to-BB front-end* with an 8-path active mixer realizing RF amplification, harmonic-recombination (HR) downconversion and BB filtering in the current domain for better linearity and power efficiency; 2) a *feedforward 8-path passive mixer* enabling LO-defined input impedance matching without external components, while offering frequency-translated bandpass filtering and noise cancelling; 3) a *single-MOS pole-zero low-pass filter (LPF)* permitting both RF and BB filtering at low voltage headroom consumption, while easing the tradeoff between the in-/out-of-band linearity, and 4) a *BB-only two-stage HR amplifier* boosting the third and fifth harmonic rejection ratios (HRR_{3,5}) with low hardware intricacy. Measurements over the TV bands (0.15 to 0.85 GHz) manifest favorable NF (4.6 ± 0.9 dB) and out-of-band IIP2/IIP3 (+61/+17.4 dBm) at small power (10.6 to 16.2 mW) and area (0.55 mm²). The HRR_{2,6} are > 51 dB without any calibration or tuning. The ultimate out-of-band P_{-1dB} is > +2.5 dBm. The BB stopband rejection is > 86 dB at 150 MHz offset.

Index Terms—Active mixer, bandpass filtering, baseband (BB), biasing, current-reuse, frequency-translation, harmonic rejection ratio, harmonic-recombination, linearity, noise cancelling, noise figure, N-path, out-of-band linearity, passive mixer, pole-zero low-pass filter, power dissipation, radio frequency (RF), receiver.

I. INTRODUCTION

FREQUENCY-FLEXIBLE radios are low-cost platforms for multi-band multi-standard wireless communications. To eliminate (or minimize) the number of

surface-acoustic-wave (SAW) filters, wideband receivers [1]–[4] mostly favor the N-path passive mixer for downconversion, due to its high linearity and bidirectional response-translational property. Depending on the first baseband (BB) node of the receiver that can be a *virtual ground* or a *low-pass-RC*, the N-path passive mixer can be classified into current-mode [1], [2] or voltage-mode [3], [4] operation, respectively. For the former, the BB virtual ground is frequency-translated to RF, absorbing both the in-band signal and out-of-band interferers. As such, the signal amplification and channel selection can be delayed to BB. For the latter, the low-pass-RC at BB can be shifted to RF, offering a tunable bandpass response (also called N-path bandpass filter) that helps suppressing the out-of-band interferers [5]–[7].

An example of the virtual-ground approach is the passive-mixer-first receiver [2] [Fig. 1(a)]. The 8-path passive mixer reduces the noise/harmonic folding and harmonic reradiation at the RF port when compared with its 4-path counterpart. Input impedance matching is achieved with zero external components and is tunable by the BB circuitry. Expectedly, due to no RF gain the out-of-band IIP3 is high (+25 dBm), but demanding low-noise mixer, LO and BB circuitry. They together bottleneck the power (37 to 70 mW over 0.1 to 2.4 GHz) for an affordable noise figure (NF) of 4 ± 1 dB.

The power has been significantly cut down to 10 to 12 mW in [4], by operating the passive mixer in the voltage mode (i.e., no virtual ground at BB and RF), and using resonant multi-phase LO and current-reuse harmonic rejection at BB. Due to the limited tuning range of the resonant LO, the RF bandwidth is narrowed (0.7 to 3.2 GHz), while the NF (10.5 ± 2.5 dB) and out-of-band IIP3 (+10 dBm) are both penalized as a tradeoff with the power. This compromise holds in advanced 28 nm CMOS wideband receiver [8]; it features a wideband LNA followed by an 8-path voltage-mode passive mixer plus G_m-C BB circuitry. This topology manages to squeeze the power (35 to 40 mW over 0.4 to 6 GHz) at low NF (1.8 to 3 dB), but is still short in terms of out-of-band IIP3 (+3 to +5 dBm). In fact, the dual-path receiver in [9] combining the noise cancellation and virtual-ground approach balances better the NF (1.9 dB) and out-of-band IIP3 (+13.5 dBm). Even so, there is still room to improve its power (35.1 to 78 mW over 0.08 to 2.7 GHz) and area (1.2 mm²) efficiencies.

The balun-LNA-I/Q-mixer (Blixer) [10] [Fig. 1(b)] is another alternative for wideband RF coverage at low power. Its original structure stacks a 4-path (i.e., no harmonic rejection) active

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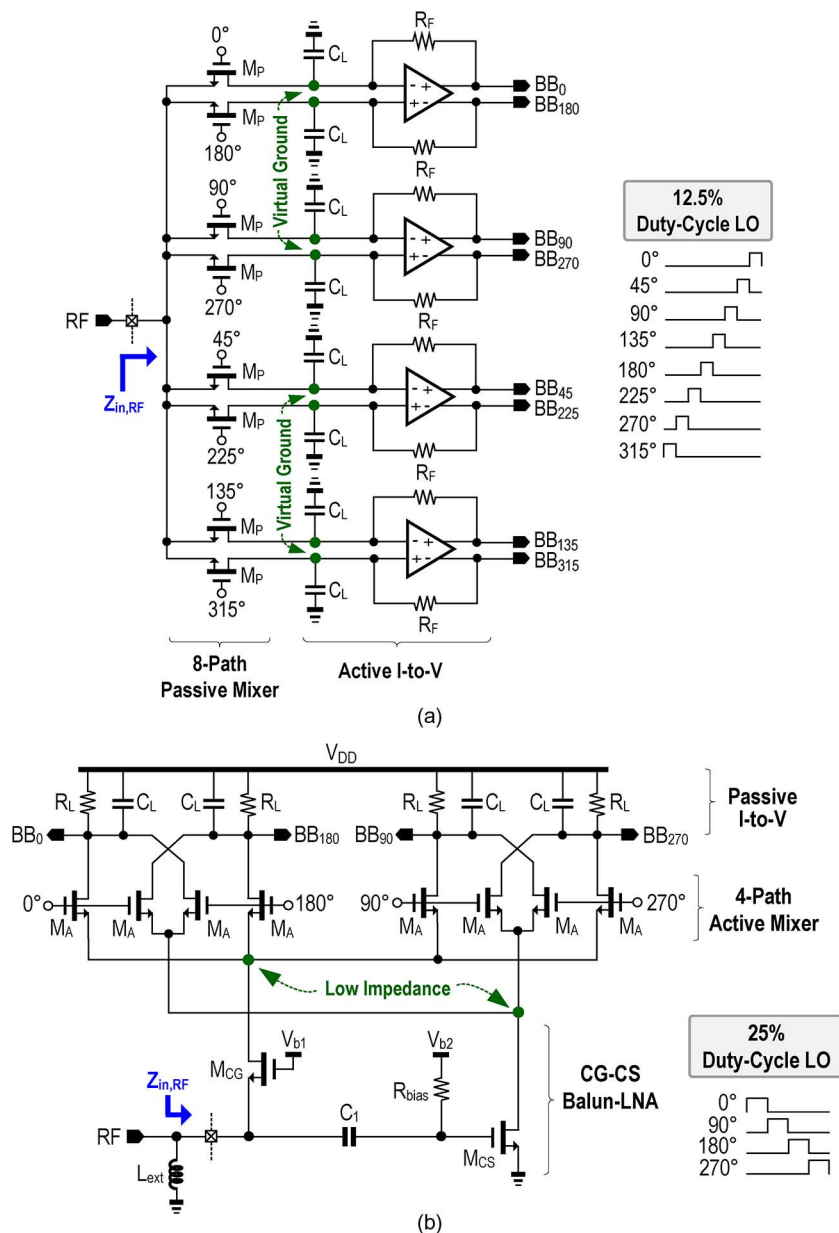


Fig. 1. Examples of wideband receivers. (a) 8-path passive-mixer-first design with an active I-to-V BB [2]. (b) Simplified balun-LNA-I/Q-mixer (Blixer) with a 4-path active mixer and a passive I-to-V BB [10].

mixer atop the balun-LNA for current-reuse and current-mode signal processing. Together with the common-gate common-source (M_{CG} and M_{CS}) input stage for noise cancellation, low NF (5 ± 0.5 dB) and wide RF bandwidth (0.5 to 7 GHz) were achieved concurrently at small power (20 to 44 mW) and area (0.02 mm², no BB filter). However, owing to no RF filtering and lower linearity of active mixers, the out-of-band IIP3 (−3 dBm) is less competitive with [1]–[4]. In addition, a bulky external inductor L_{ext} (40 nH) is entailed to attain a wideband input impedance match, while an AC-coupling network (R_{bias} and C₁) is also entailed for biasing the CS transistor (M_{CS}); both induce in-band signal loss.

This paper presents a single-ended-input current-reuse wideband receiver with an N-path configuration to enhance the performance. It targets the TV-band (0.15 to 0.85 GHz) appli-

cations such as mobile TV and IEEE 802.11af. For the former, a NF < 5 dB is expected (no balun), and rejection of the third and fifth LO harmonics is required due to in-band harmonic mixing (i.e., $0.15 \times 3 = 0.45$ GHz, $0.15 \times 5 = 0.75$ GHz). The required out-of-band IIP3 is −8 dBm and IIP2 is 23 dBm [11]. The stacked RF-to-BB front-end is based on an 8-path active mixer, unifying not only RF amplification and downconversion, but also high-order BB current-mode filtering in one branch. A feedforward 8-path passive mixer elegantly realizes the input impedance matching, RF filtering, input biasing and noise cancelling. The generated 8-phase BB signals allow two-step harmonic recombination (HR) solely at BB for enhancing the third and fifth harmonic-rejection ratios (HRR_{3,5}). The fabricated 65 nm CMOS receiver shows balanced NF (4.6 ± 0.9 dB) and out-of-band IIP3 (+17.4 dBm) with small power

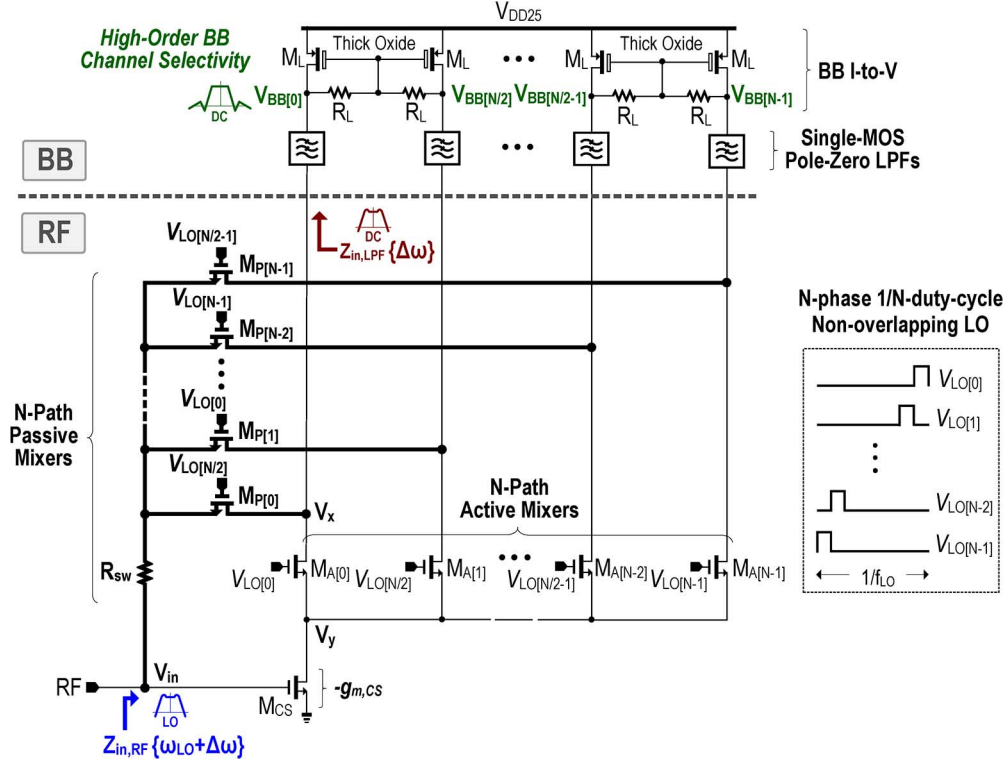


Fig. 2. Proposed stacked RF-to-BB front-end. It unifies RF amplification, downconversion and BB filtering in one combined cell. The N-path passive mixer assists the input impedance matching, RF filtering and noise cancelling, without resorting to any external components.

(10.6 to 16.2 mW) and area (0.55 mm², with BB LPF), without resorting from any external components.

After the Introduction in Section I, Section II presents the proposed receiver architecture and details its circuit design. The experimental results are summarized in Section III, and conclusions are given in Section IV.

II. RECEIVER ARCHITECTURE AND CIRCUIT DETAILS

A. Stacked RF-to-BB Front-End With Parallel N-Path Active/Passive Mixers

The proposed stacked RF-to-BB front-end is depicted in Fig. 2. To cover the VHF-H and UHF bands (150 to 850 MHz) that have together 140% fractional bandwidth, $N = 8$ alleviates harmonic mixing due to the critical second to 6th LO harmonics. The 7th LO harmonic is pushed out band ($0.15 \times 7 = 1.05$ GHz), as well as the harmonic reradiation term appears in the passive-mixer-first design. Another option is $N = 4$ which is suitable for high-frequency applications, as harmonic mixing is no longer severe, and LO-path power can be saved during frequency division. In the analysis below, the symbol N is preserved for generality.

The receiver is headed by a CS amplifier (M_{CS}) serving as the LNA, which is the only RF V-to-I conversion. Its output and bias currents are then modulated by an N-path active mixer [$M_{A[0]} \dots M_{A[N-1]}$] driven by an N-phase 1/N-duty-cycle LO [$V_{LO[0]} \dots V_{LO[N-1]}$]. A high-order current-mode LPF is stacked atop each mixer offering the channel selection before BB I-to-V conversion via R_L . The current-mode LPF features a low-pass input impedance ($Z_{in,LPF}$) and is referred

to a single-MOS pole-zero topology to achieve high stopband rejection at low voltage headroom consumption. Similar to [3] and [12], the I/O supply (e.g., 2.5 V in 65 nm CMOS) is useful to extend the transistor overdrives and 1 dB compression point (P_{-1dB}), while utilizing the thin-oxide and thick-oxide MOS for the RF and BB circuitry, respectively, and it can leverage the speed, 1/f noise and gain (i.e., output conductance). The node-voltage trajectory check and protection circuitry similar to [3] have been applied to ensure there is no risk of device reliability.

The N-phase BB outputs [$V_{BB[0]} \dots V_{BB[N-1]}$] allow two-step HR solely at BB (outside the front-end), rejecting the critical LO harmonics up to $N - 2$ (N is even) [1]. The LO is generated by a div-by-8 circuit optimized at typical 1.2 V. A feedforward N-path passive mixer [$M_{P[0]} \dots M_{P[N-1]}$] driven by the same set of LO is added and its equivalent ON-resistance is denoted as R_{sw} . [$M_{P[0]} \dots M_{P[N-1]}$] is anti-phased with [$M_{A[0]} \dots M_{A[N-1]}$] during the mixing for the following three intents:

Input Impedance Matching and LO-defined RF Filtering: The N-path active/passive mixer generates a frequency-translational loop as illustrated in Fig. 3. Owing to the bidirectional transparency of passive mixers, $M_{P[0]}$ can frequency-translate the low-pass $Z_{in,LPF}\{\Delta\omega\}$ at V_x to bandpass $Z_{in,RF}\{\omega_{LO} + \Delta\omega\}$ at V_{in} , enabling LO-defined input matching and RF filtering. Afterwards, the BB signal at V_x is upconverted to V_{in} before being finally downconverted back to V_x by the $-g_{m,CS}$ stage and $M_{A[0]}$. V_{in} contains the fundamental tone at f_{LO} and harmonic components at $|1 - gN|f_{LO}$ (with $g = \pm 1, \pm 2 \dots$), and all of them will

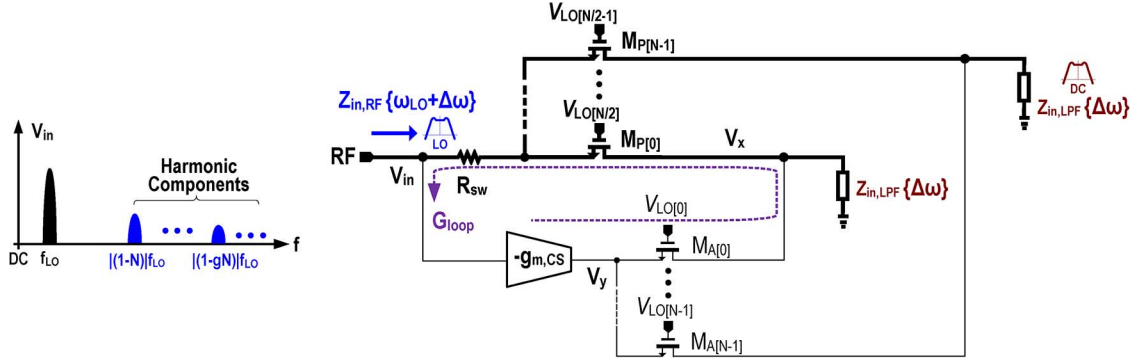


Fig. 3. Functional view of the frequency-translational loop created by the N-path active/passive mixers.

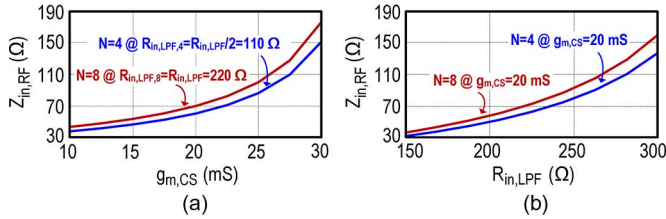


Fig. 4. Simulated RF input impedance $Z_{in,Rf}$ versus: (a) $g_{m,CS}$ under $N = 4$ and 8 ; (b) $R_{in,LPF}$ under $N = 4$ and 8 . The selected $Z_{in,Rf} = 70 \Omega$, $g_{m,CS} = 20 \text{ mS}$, $R_{in,LPF} = 220 \Omega$ and $N = 8$.

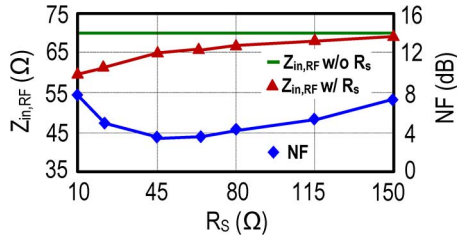


Fig. 5. Simulated RF input impedance $Z_{in,Rf}$ and NF versus R_s variations.

contribute to the input impedance via the N-path active mixer after downconversion to V_x . The equivalent input impedance is given by

$$Z_{in,Rf}\{\omega_{LO} + \Delta\omega\} \approx \frac{R_{sw} + \frac{1}{N} \text{sinc}^2\left(\frac{\pi}{N}\right) \cdot Z_{in,LPF}\{\Delta\omega\}}{1 - G_{loop}} \quad (1)$$

where G_{loop} is the loop gain:

$$G_{loop} = \frac{1}{N} \cdot g_{m,CS} \cdot Z_{in,LPF}\{\Delta\omega\}, \quad (2)$$

$g_{m,CS}$ is the transconductance of M_{CS} , and the last summation term is the frequency-translational factor of the N-path mixing. The resistive part of $Z_{in,LPF}$, denoted as $R_{in,LPF}$, is directly given by the transconductance of the LPF's transistor (i.e., $1/g_{m,LPF}$). $N = 4$ or $N = 8$ generates a similar $Z_{in,Rf}$ value and it goes up with $g_{m,CS}$ and $R_{in,LPF}$ as shown in Fig. 4(a) and (b), respectively. To cover the TV band, the selected $Z_{in,Rf}$ is 70Ω to take into account the S_{11} bandwidth and input capacitance. The NF and $Z_{in,Rf}$ of the receiver with R_s and without R_s are plotted in Fig. 5. It shows that $Z_{in,Rf}$ is

within 63 to 67Ω even when R_s (i.e., the antenna impedance) changes from 35 to 80Ω .

Given a fixed bias current, $N = 4$ and $N = 8$ show the same G_{loop} ($= g_{m,CS}R_{in,LPF}/N$) at DC, as $R_{in,LPF}$ goes up proportionally when N increases. In this work ($N = 8$), $g_{m,CS}$ is set at 20 mS suitable for noise cancelling (analyzed later) and G_{loop} should be below 1 from (2), thus the corresponding $R_{in,LPF}$ should be below 400Ω . The designed value of $R_{in,LPF}$ is 220Ω for input impedance matching, with the resultant G_{loop} is 0.55 , which is well below 1 for stability. Such a G_{loop} results in $2.2\times$ increment of $Z_{in,Rf}$, permitting a smaller R_{sw} (6Ω) to enhance the ultimate stopband rejection at V_{in} , which is theoretically 13.3 dB [$2R_{sw}/(R_{sw} + R_s)$] for $R_s = 50 \Omega$ due to the frequency-translational property of the passive mixer. Moreover, to enlarge the voltage headroom and enhance the linearity, the active mixer was biased in the *triode* region. This act brings down the swing at V_y (drain node of M_{CS}) and frequency-translates the low-pass response at V_x to bandpass response at V_y , as shown in Fig. 6(a). With this extra filtering, V_y shows larger out-of-band rejection than V_{in} [Fig. 6(b)], e.g., V_y has 2.5 dB higher rejection than V_{in} at 200 MHz offset for $W/L_{MA} = 12/0.06$. Those responses at V_y also imply that the in-band gain and stopband rejection are in tradeoff under different sizes of the active mixer (W/L_{MA}), which correspond to different equivalent ON-resistances. Further, a large W/L_{MA} also implies more LO power. Nevertheless, due to the presence of the passive mixer, bandpass filtering happens at the forefront V_{in} , inducing a similar response at V_y that is the RF node which can limit the out-of-band linearity. With the filtering at V_{in} and V_y , the active mixer can be downsized (W/L : $12/0.06$) for saving the LO power, while still generating $>10 \text{ dB}$ and $>13 \text{ dB}$ rejection at V_{in} and V_y at 150 MHz offset, respectively. Moreover, the filtering profile of $Z_{in,LPF}$ can be peaked around the cutoff, which is a better bandpass shape after frequency-translational to V_{in} [13], [14]. In fact, both the RF and BB bandwidth can be concurrently tuned due to the frequency-translational effect of the mixer, which will be detailed in Section II-B.

Input Biasing: Without any external components and AC-coupling networks, the gate of M_{CS} can be handily biased via the passive mixers copying the DC voltage from V_x to V_{in} , also giving adequate overdrive voltage ($V_{DS} = 420 \text{ mV}$) on M_{CS} for better linearity. Furthermore, owing to no AC-coupling capacitor, the RF bandwidth can easily cover the low-frequency

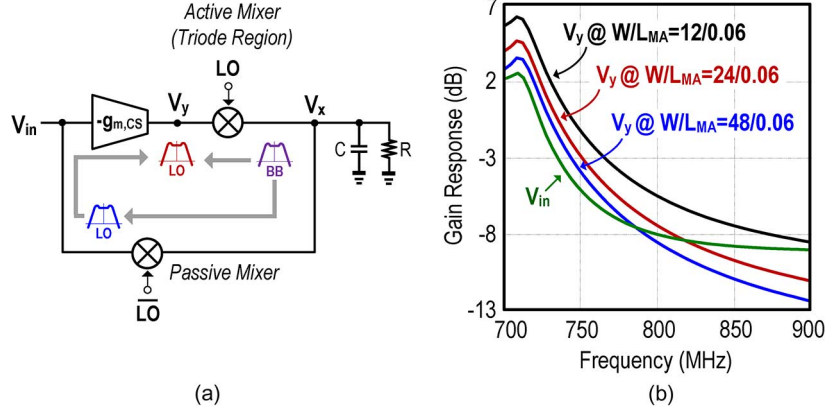


Fig. 6. (a) Low-pass to bandpass response translation from V_x to V_{in} via the passive mixer, and from V_x to V_y via the active mixer. (b) Simulated responses at V_{in} and V_y with respect to the device size of the active mixer. V_y has stronger out-of-band rejection than V_{in} due to the extra filtering provided by the active mixer.

range (150 MHz), better than other CG-CS receiver front-ends that entail both a bulky external inductor (40 nH in [10] and 80 nH in [12]) and AC-coupling.

Noise Cancellation: Noise cancellation of R_{sw} and LPF can be concurrently achieved under the parallel N-path active/passive mixers. The passive mixer serves as a current-sensing path, while the active mixer serves as a voltage-sensing path to add the signals constructively and cancel the noise of R_{sw} and LPF under $g_{m,CS} R_S = 1$. As shown in Fig. 7(a), both the noise contribution of R_{sw} and LPF are modeled as noise current sources. For the former, R_{sw} induces a noise current to R_S ($-k_1 \cdot i_{n,R_{sw}}$), and is sensed by the $-g_{m,CS}$ stage to produce an anti-phased output noise current ($k_1 \cdot g_{m,CS} \cdot R_S \cdot i_{n,R_{sw}}$), which nullifies the noise inherently. The output noise due to the R_{sw} can be derived as

$$\overline{i_{n,R_{sw},out}^2} = \left| \frac{(1 - g_{m,CS} \cdot R_S) R_{sw}}{(R_S + R_{sw})N + (1 - g_{m,CS} \cdot R_S) Z_{in,LPF} \{ \Delta \omega \}} \right|^2 \cdot \overline{i_{n,R_{sw}}^2} \quad (3)$$

For the LPF, when the receiver is operated differentially, the noise of LPF [Fig. 7(b)] generates a noise current on R_S ($k_2 \cdot i_{n,LPF}$), which is copied to another path with the same phase ($k_2 \cdot g_{m,CS} \cdot R_S \cdot i_{n,LPF}$), being a cancellable common-mode noise. Thus, the differential output noise due to the LPF is simplified as

$$\overline{i_{n,LPF,out}^2} = \left| \frac{(1 + c_1)(1 - g_{m,CS} \cdot R_S)}{1 + c_2} \right|^2 \cdot \overline{i_{n,LPF}^2} \quad (4)$$

where c_1 and c_2 are constants as given by

$$c_1 = \frac{g_{m,CS} \cdot R_S}{1 + g_{m,LPF}(R_S + R_{sw})N}, \quad (5)$$

$$c_2 = g_{m,LPF}(R_S + R_{sw})N - \frac{(g_{m,CS} \cdot R_S)^2}{1 + g_{m,LPF}(R_S + R_{sw})N}. \quad (6)$$

The above expressions show that the noise of both passive mixer and LPF can be made insignificant when the condition $g_{m,CS} \cdot$

$R_S = 1$ is met. Again, due to the high drain-source output impedance of M_{CS} , the active mixer contribution is insignificant to the in-band noise. Considering the major noise sources from $M_{CS}(v_{n,CS})$ and load ($v_{n,L}$), the receiver noise factor (F) can be derived as

$$F = \left(1 + \frac{\overline{v_{n,CS}^2}}{\overline{v_{n,R_S}^2}} + 2N \cdot \frac{R_S^2}{R_L^2} \cdot \frac{\overline{v_{n,L}^2}}{\overline{v_{n,R_S}^2}} \right) \frac{1}{\text{sinc}^2\left(\frac{\pi}{N}\right)}. \quad (7)$$

A large R_L reduces its noise contribution, rendering the in-band NF dominated by the thermal noise of M_{CS} (i.e., $F \approx 1 + \gamma$, where γ is the channel noise factor). Thus, although this receiver front-end consumes low power, it shows a theoretical NF limit of ~ 3 dB, which is higher than the dual-path receiver in [9], but it is comparable to other high-linearity passive-mixer-first receivers such as [2]. To reduce also the $1/f$ noise, M_{CS} is upsized (W/L: 120/0.18). A large N is more beneficial to the NF due to the frequency-translational factor $\text{sinc}^2(\pi/N)$ of the mixer. For example, the NF for $N = 4$ shows around 0.68 dB degradation when compared with that under $N = 8$ under the same current condition with the same M_{CS} , because R_L for $N = 8$ is two times as that for $N = 4$, thus the load of the two cases contribute the same noise as seen from (7). In this design ($N = 8$), for a 1.6 mA bias current (i.e., corresponding to $g_{m,CS}$ of 20 mS), the simulated NF of the receiver front-end is 3.6 dB, of which ~ 0.5 dB is contributed by M_L and R_L . As revealed in [9] and [15], the noise cancelling mechanism is relatively robust to mismatches. From simulations, the NF varies only 0.15 dB with 20% current offset. When the input parasitic capacitance (1.5 pF) is accounted, the NF is degraded by ~ 0.4 dB in the covered frequency range. From Fig. 5, the NF is ~ 4 dB when R_s is changed from 35 to 80 Ω . Beyond that, the NF increases further due to both impedance mismatch and imperfect noise cancellation.

B. Current-Mode Single-MOS Pole-Zero LPF

Traditional LPFs using operational amplifiers are unsuitable for current reuse with other circuitry. Current-mode LPF, such as the pipe filter [16], is more transistorized and suitable for stacking with the active mixer for current-reuse and current-mode filtering [12] that has in-band noise

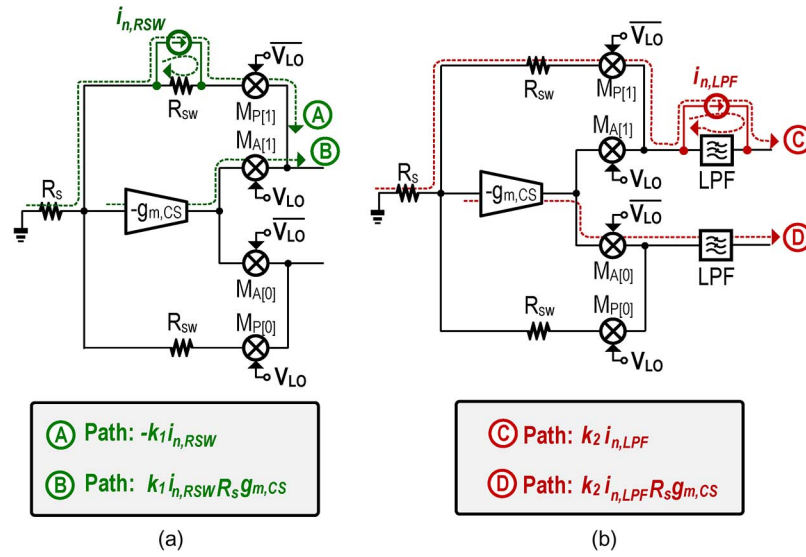


Fig. 7. Simplified two-phase noise equivalent circuits of the RF front-end. (a) $M_{A[1]}$ and $M_{P[1]}$ are anti-phase to realize noise cancellation of R_{sw} ; (b) $M_{P[1]}$ and $M_{A[0]}$ and in-phase, rendering the noise of LPF a cancellable common-mode noise at the differential output. k_1 and k_2 are constant representing the noise currents leak to R_s .

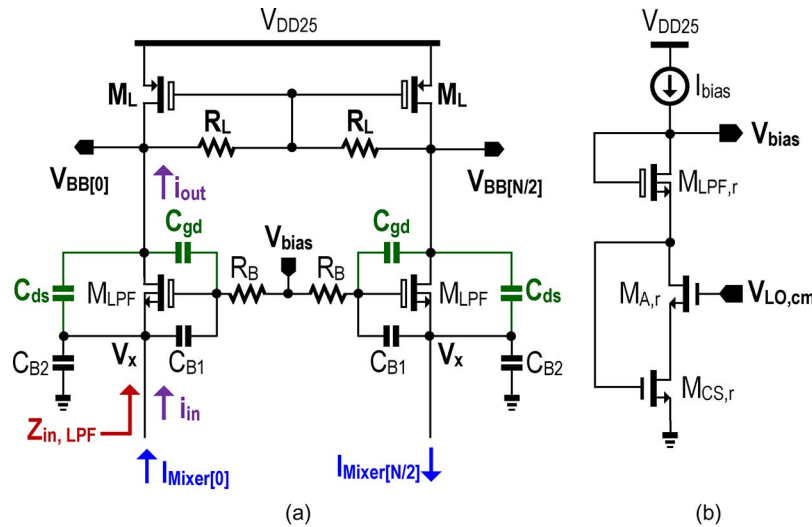


Fig. 8. (a) Proposed single-MOS pole-zero LPF and load (differential form); (b) its replica bias circuit.

shaping and high linearity. However, a second-order current-mode Biquad [16] involves two transistors in cascode, pressuring the voltage headroom. More importantly, its input impedance features an in-band zero at DC, which is inappropriate for frequency translation to RF that otherwise nullifies the in-band gain. The single-MOS current-mode Biquad in [17] alleviates the problems of voltage headroom and zero at DC, but still, only two poles are synthesized. To enhance the close-in stopband rejection, a current-mode single-MOS pole-zero LPF is proposed as detailed below.

The differential schematic of the single-MOS pole-zero LPF and its replica bias circuit are shown in Fig. 8(a) and (b), respectively. For the LPF, M_{LPF} (with $g_{m,LPF}$) is the only active device, working with $C_{B1,2}$ and R_B to create the complex poles [17], and plus C_{gd} and C_{ds} to create the stopband zeros. The BB I-to-V conversion and common-mode feedback are associated with the self-biased M_L such that a big R_L can be applied, al-

leviating the tradeoff between voltage headroom and BB gain. As M_L is diode-connected, it can be considered as a current mirror to copy the signals to the next HR stage (Section II-C). M_L and M_{LPF} are thick-oxide MOS to withstand the high V_{DD} (2.5 V) that enlarges the device overdrives and P_{-1dB} . Working at BB, bigger M_L and M_{LPF} are allowed to reduce the $1/f$ noise. Moreover, R_L can be tuned for gain control without affecting the output DC bias point. The grounded C_{B2} is added for LO feedthrough mitigation and better out-of-band attenuation of interferences.

For the bias circuit, $M_{CS,r}$, $M_{A,r}$ and $M_{LPF,r}$ are the replicas of M_{CS} , M_A and M_{LPF} , respectively. The gate bias of $M_{CS,r}$ is handily copied from the drain of $M_{A,r}$. $V_{LO,cm}$ copies the common-mode voltage of the LO. After simplification, the I/O transfer function and input impedance $[Z_{in,LPF}(s)]$ of the LPF can be derived as in equations (8)–(9) shown at the bottom of the next page, where the two pairs of dominant poles and zeros

are located at f_p and f_z , as shown in equations (10)–(11) at the bottom of this page.

When sizing the LPF, an intentionally large transistor M_{LPF} (W/L: 768/0.5) with bulk-source connection is used, which has equivalent parasitic C_{gd} and C_{ds} of ~ 0.6 pF, creating the two stopband zeros. Differing from the current-mode Biquads in [16], [17] that only can synthesize two complex poles, this design offers faster-roll-off pole-zero filtering, being more cost-effective than its real-pole-only counterparts [1]–[4]. Fig. 9(a) shows the simulated filtering profile with $C_{\text{B1,2}} = 24$ pF, $R_{\text{B}} = 400 \Omega$, $R_{\text{L}} = 5$ k Ω and $g_{\text{m,LPF}} = 4.5$ mS. Without C_{gd} and C_{ds} , the stopband profile is 40 dB/dec. When C_{gd} and C_{ds} are presented and increased to 0.3 pF, the stopband zeros effectively boost the stopband rejection. In this design, the zeros are placed at 150 MHz offset, so as to filter out: 1) the LO-to-IF leakage for the targeted RF bandwidth due to 150 MHz (the employed 8-path active mixer can be considered as an extension of 2-path single-balanced active mixer), and 2) the GSM850/900 bands when the receiver is operated up to 710 MHz for IEEE 802.11af. From simulations, a 26 dB improvement (58 dB rejection in total) is achieved when comparing it with pure-pole Biquad at 150 MHz offset. In Monte-Carlo simulations, the -3 dB BW_{mean} is 14.6 MHz ($\sigma = 0.48$ MHz) and the stopband zero is located at 154 MHz ($\sigma = 6.3$ MHz) with average rejection of 54.7 dB ($\sigma = 1.08$ dB). The RF-to-BB gain at $V_{\text{BB}[0]}$ can be expressed as $s/N \cdot \text{sinc}(\pi/N) \cdot g_{\text{m,CS}} \cdot R_{\text{L}}$, which is 26 dB in the design with $R_{\text{L}} = 5$ k Ω . For the receiver front-end, the simulated in-band $\text{P}_{-1\text{dB}}$ and IIP3 at $V_{\text{BB}[0]}$ are -17 and 0 dBm at a 2.5 V supply, respectively. Given a bias current, the gain and NF are almost constant if the supply is reduced to 1.8 V, but the in-band $\text{P}_{-1\text{dB}}$ and IIP3 will be penalized to -26 and -11 dBm, respectively.

The current-mode LPF features in-band noise shaping when it is operated with the active mixer. Its noise contribution can

be modeled as a current source connected between drain and source of M_{LPF} . To evaluate it, a derivation is done with the result given in (12) after simplification. By resorting from C_{gd} and C_{ds} to create the stopband zeros, the noise distribution also differs from the typical Biquad. From simulations [Fig. 9(b)], the output noise has a bandpass shape under the condition of $C_{\text{gd}} = C_{\text{ds}} = 0.3$ pF, other than a high-pass shape without C_{gd} and C_{ds} , because they shunt the noise current at high frequency. Their in-band noise responses are the same. (See equation (12) at the bottom of the next page). Recalling Fig. 9(a), the LPF features a peak response around the cutoff for its input impedance [see (9)] due to C_{gd} and C_{ds} ; they enhance not only the filtering profile, but also avoid the fast roll-off shape when it is translated to RF.

Another interesting property of this LPF is about its stopband profile and R_{L} as showed in Fig. 9(c). As the current-mode filtering effects at input and output nodes of the LPF, mainly the passband gain is altered by R_{L} , easing the tradeoff between the in-/out-of-band linearity. For instance, a large R_{L} can enhance the stopband rejection at the expense of in-band IIP3 and $\text{P}_{-1\text{dB}}$, and is bounded by the $Z_{\text{in,LPF}}$ variations.

Due to the frequency-translation property of the N-path mixer, the BB LPF can define concurrently the RF and BB bandwidth. Thus, without affecting most in-band metrics and power, adjusting C_{B} can effectively suppress the out-of-band interferers before they reach the active devices at both RF and BB. From simulations, when $C_{\text{B1,2}}$ is increased from 24 to 96 pF (tradeoff with the die area), a higher Q bandpass response can be created at V_{in} and V_{y} , as shown in Fig. 10. The zero of $Z_{\text{in,LPF}}$ is chosen at ~ 10 MHz, where the 1 dB gain peak leads to ~ 1.5 dB variations of in-band IIP3 (simulation). The Q factor can be lowered by reducing $g_{\text{m,LPF}}$ and R_{B} . The ultimate rejection is limited by the size of R_{SW} . The BB responses at V_{x} and $V_{\text{BB}[0]}$ are 20 dB/dec and >40 dB/dec, respectively, as expected from (8) and (9).

$$\frac{i_{\text{out}}(s)}{i_{\text{in}}(s)} \approx \frac{s^2 \frac{C_{\text{gd}} + C_{\text{ds}}}{C_{\text{B2}}} + \frac{g_{\text{m,LPF}}}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}}}{s^3 [(C_{\text{gd}} + C_{\text{ds}}) R_{\text{L}}] + s^2 \left[1 + \frac{C_{\text{gd}} g_{\text{m,LPF}} R_{\text{L}}}{C_{\text{B1}}} + \frac{(C_{\text{B1}} + C_{\text{B2}})(C_{\text{gd}} + C_{\text{ds}}) R_{\text{L}}}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}} \right] + s \frac{(C_{\text{B1}} + C_{\text{B2}})}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}} + \frac{g_{\text{m,LPF}}}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}}} \quad (8)$$

$$Z_{\text{in,LPF}}(s) \approx \frac{s^2 \left[\frac{(C_{\text{gd}} + C_{\text{ds}}) R_{\text{L}}}{C_{\text{B2}}} \right] + s \left[\frac{1}{C_{\text{B2}}} + \frac{C_{\text{ds}}(1 + g_{\text{m,LPF}} R_{\text{L}})}{C_{\text{B1}} C_{\text{B2}}} + \frac{(C_{\text{gd}} + C_{\text{ds}}) R_{\text{L}}}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}} \right] + \frac{1}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}}}{s^3 [(C_{\text{gd}} + C_{\text{ds}}) R_{\text{L}}] + s^2 \left[1 + \frac{C_{\text{gd}} g_{\text{m,LPF}} R_{\text{L}}}{C_{\text{B1}}} + \frac{(C_{\text{B1}} + C_{\text{B2}})(C_{\text{gd}} + C_{\text{ds}}) R_{\text{L}}}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}} \right] + s \frac{(C_{\text{B1}} + C_{\text{B2}})}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}} + \frac{g_{\text{m,LPF}}}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}}}} \quad (9)$$

$$f_p = \frac{1}{2\pi} \sqrt{\frac{g_{\text{m,LPF}}}{C_{\text{B1}} C_{\text{B2}} R_{\text{B}} + C_{\text{B2}} C_{\text{gd}} g_{\text{m,LPF}} R_{\text{L}} R_{\text{B}} + (C_{\text{B1}} + C_{\text{B2}})(C_{\text{gd}} + C_{\text{ds}}) R_{\text{L}}} \quad (10)$$

$$f_z = \frac{1}{2\pi} \sqrt{\frac{g_{\text{m,LPF}}}{C_{\text{B1}}(C_{\text{gd}} + C_{\text{ds}}) R_{\text{B}}} \quad (11)$$

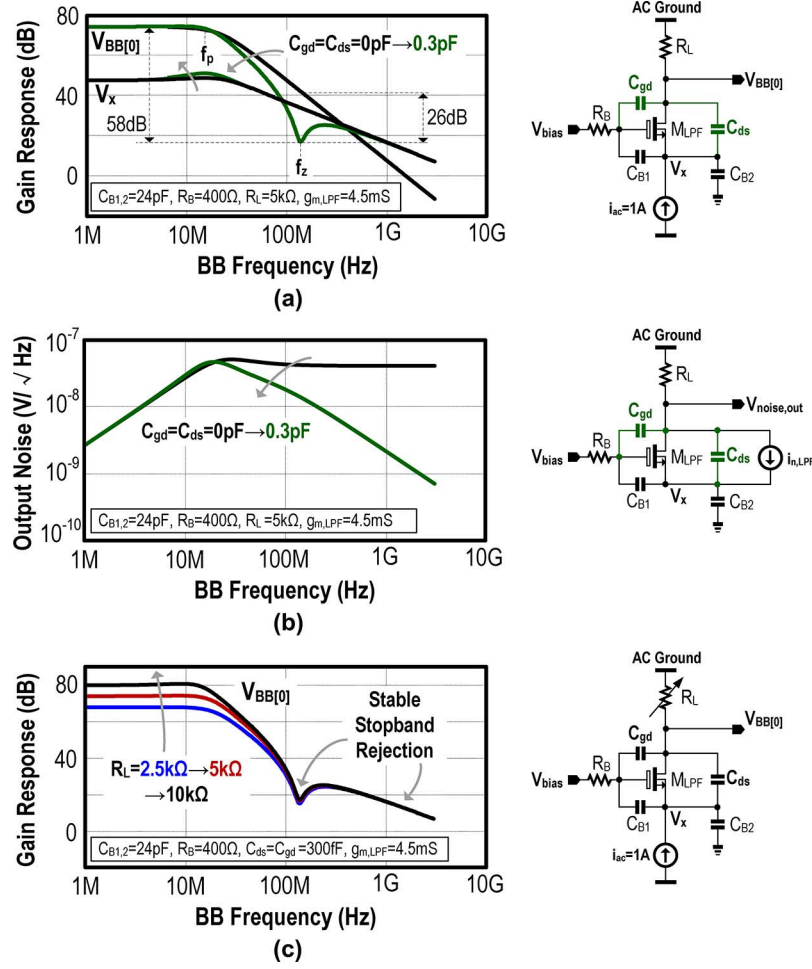


Fig. 9. Simulated (a) $V_{BB[0]}$ and V_x showing the rejection added by the stopband zeros. (b) Output noise with and without stopband zeros. (c) Sizing R_L for in-band gain and linearity tradeoff.

C. BB-Only Two-Stage Harmonic-Recombination (HR) Amplifier

Single-stage HR measured an uncalibrated $\text{HRR}_{3,5}$ of 34 to 45 dB [4], [9]. The proposed BB-only two-stage HR amplifier boosts the $\text{HRR}_{3,5}$ without any gain scaling at RF [1], resulting in simpler layout and lower parasitics. Fig. 11(a) shows the principle of the two-stage HR to recombine the 8-phase BB outputs $\{V_{BB[0]} \dots V_{BB[7]}\}$ from the front-end, and generate the final differential BB I/Q outputs $\{\pm V_{O,I}, \pm V_{O,Q}\}$. Three 45° -apart signals of $\{V_{BB[0]} : V_{BB[1]} : V_{BB[2]}\}$, $\{V_{BB[1]} : V_{BB[2]} : V_{BB[3]}\}$ and $\{V_{BB[2]} : V_{BB[3]} : V_{BB[4]}\}$, with weighting ratio of $\{2 : 3 : 2\}$, are arranged to generate three new 45° -apart signals of $\{V_{H1[0]} : V_{H1[1]} : V_{H1[2]}\}$, which are then weighted again by $\{5 : 7 : 5\}$ to reproduce the desired gain ratio $\{1 : \sqrt{2} : 1\}$ for

harmonic cancellation. This two-step HR method can approximate the gain ratio $\{1 : \sqrt{2} : 1\}$ with $<0.1\%$ error [1]. From the illustrated vector diagram, by pushing back the two-stage HR to BB, the multiplication of errors to improve HRR still holds. The total relative gain error is made insignificant due to the multiplication of error: $(\varepsilon_o + \varepsilon_{1,HR})\varepsilon_{2,HR}/4$, where ε_o is the relative gain error of the front-end; $\varepsilon_{1,HR}$ and $\varepsilon_{2,HR}$ are the relative gain errors of the BB first and second HR stages, respectively. The error ε_o is merged into the first stage and theoretically the second stage with 1% error can improve the harmonic rejection by 46 dB under an ideal 8-phase LO.

In the implementation [Fig. 11(b)], identical amplifiers with differential configuration in both first and second stages are employed to ensure that each signal has the same load condition, mitigating the parasitic effects. The gain weighting is based on

$$\overline{i_{\text{noise,LPF}}^2}(s) \approx$$

$$\frac{(s^2 C_{B1} C_{B2} R_B + s C_{B1} + s C_{B2}) \cdot \overline{i_{n,LPF}^2}}{s^3 [(C_{gd} + C_{ds}) C_{B1} C_{B2} R_B R_L] + s^2 [C_{B1} C_{B2} R_B + (C_{gd} + C_{ds})(C_{B1} + C_{B2}) R_L + C_{B2} C_{ds} g_{m,LPF} R_B R_L] + s(C_{B1} + C_{B2} + C_{ds} g_{m,LPF} R_L) + g_{m,LPF}} \quad (12)$$

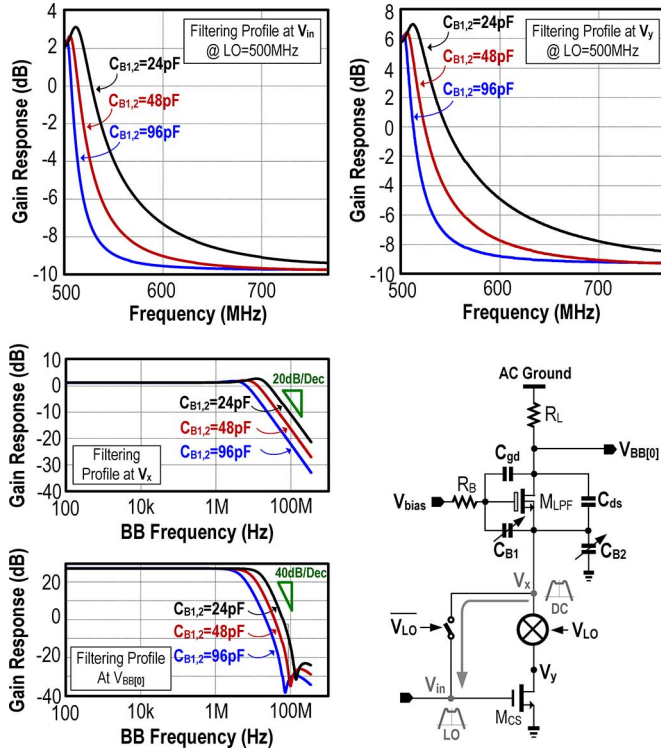


Fig. 10. Simulated frequency-translated RF bandwidth at V_{in} and V_y , and BB bandwidth at V_x and $V_{BB[0]}$ are concurrently controlled by $C_{B1,2}$.

a PMOS-input amplifier $\{2 : 3 : 2\}$ followed by a NMOS-input amplifier $\{5 : 7 : 5\}$ with self-biased loads. By extending the two-stage HR to BB, the circuit complexity is reduced and the irrational gain ratio $\{1 : \sqrt{2} : 1\}$ is realized accurately due to the realized rational numbers.

Owing to the embedded BB channel selectivity at the front-end, the linearity of such a HR amplifier is highly relaxed, so as its power budget. The latter also leads to limited BB bandwidth assisting the stopband rejection. From Monte-Carlo simulations, the in-band $HRR_{3,5} \geq 62$ dB (mean) and 53 dB (worst) under an ideal 8-phase LO. Thus, the $HRR_{3,5}$ should be limited mainly by the LO phase error similar to [1].

D. 8-Phase 12.5%-Duty-Cycle LO Generator

To lower the LO phase error and jitter at pulse edge, a dynamic div-by-8 circuit [Fig. 12(a)] based on transmission-gate flip-flop cell as in [1] is employed to generate a 12.5% 8-phase LO without needing AND gates. For saving the LO power, the 8-phase LO is buffered to drive the mixer with rise and fall time of ~ 25 ps (2% LO period at 850 MHz), of which the effect on the gain and NF is insignificant for such a sub-GHz operation. In the covered band from 0.15 to 0.85 GHz, the simulated phase error goes up from $\sigma = 0.045^\circ$ to 0.4° , at the power of 2.8 to 7.5 mW [Fig. 12(b)]. If a high HRR is desired, the accuracy of the phase error can be enhanced with more dynamic power being provided to the high-frequency LO buffer and dividers, as analyzed in [1].

Simulated at 0.55 GHz, the output phase noise of the LO generator is -155 dBc/Hz at $\Delta f = 0.15$ GHz, where Δf is the frequency offset from the LO. As V_{in} has ~ 10 dB rejection at $\Delta f = 0.15$ GHz, the 0 dBm blocker NF is at least 9 dB (i.e.,

174 dBm $-$ 155 dBc $-$ 10 dB) due to the reciprocal mixing effect. To address this, the LO generator proposed in [9] can be employed, which has a power efficiency of 13.3 mA/GHz in 40 nm CMOS.

III. EXPERIMENTAL RESULTS

The receiver was fabricated in a 1.2/2.5 V 65 nm CMOS process. Deep n-well was employed for the bulk-source connection in the single-MOS LPF. The chip micrograph is shown in Fig. 13. Without any on-chip inductors or external components, the die area is small (0.55 mm²) and it is dominated by the 8-path LPFs with $C_B = 24$ pF. All measurements were on one randomly selected die and small die-to-die variations were observed.

A. Input Matching, NF, Gain and Power Consumption

The receiver covers 0.15 to 0.85 GHz (VHF-H and UHF bands) with a LO-defined narrowband input matching $S_{11} < -12.5$ dB [Fig. 14(a)]. It serves as an indirect measurement of the bandpass filtering effect translated to V_{in} . Both RF-to-IF gain (51 ± 1 dB) and NF (4.6 ± 0.9 dB) are wideband stable and the results include the PCB losses [Fig. 14(b)]. The NF increases with frequency due to the limited drivability of the LO buffers and phase noise of the LO generator. The latter couples to the RF port through the mixer parasitic capacitances and raises the NF up to ~ 1 dB at 850 MHz RF. The estimated pad capacitance at the RF input is ~ 1.5 pF, which affects the NF at high frequency but improves the S_{11} . The power increases with the RF frequency from 10.6 to 16.2 mW due to the dynamic power of the LO generator. The static power (RF+BB) is only 7.5 mW comprising the current-reuse front-end (1.6 mA at 2.5 V) and the two-step BB HR amplifier (1.4 mA at 2.5 V).

B. Linearity

Both the Blixer [10] and this work involve only one RF V-to-I conversion, but the Blixer uses wideband input matching and RF gain, while this work features bandpass filtering at V_{in} , thus significantly improving the out-of-band linearity. Two-tone tests with frequency at $[f_{LO} + \Delta f, f_{LO} + \Delta f + 1$ MHz] and $[f_{LO} + \Delta f, f_{LO} + 2\Delta f - 1$ MHz] were applied to measure IIP2 and IIP3, respectively. At 0.7 GHz RF and maximum gain, the in-band IIP2/IIP3 is $+15/-12$ dBm with an input power of around -50 dBm, whereas the out-of-band IIP2/IIP3 is $+61/+17.4$ dBm with an input power of around -25 dBm [Fig. 15(a)]. As shown in Fig. 15(b), the measured P_{-1dB} at 20 MHz is -25 dBm and the ultimate out-of-band P_{-1dB} is $> +2.5$ dBm, which are consistent with the IIP3 measurements. Another critical scenario is that two tones at $[f_{LO} - \Delta f, \Delta f + 1$ MHz] or $[f_{LO} + \Delta f, \Delta f - 1$ MHz] would also generate second-order distortion. The measurement at 0.7 GHz with $\Delta f = 150$ MHz shows that the IIP2 with two tones at 0.151 and 0.55 GHz is $+22$ dBm, and with 0.149 and 0.85 GHz is $+21$ dBm. Both are limited by M_{CS} at RF.

C. BB Response and HRR

The BB bandwidth is close to 9 MHz, with strong stopband rejection of 86.3 dB at 150 MHz offset, thanks to the dual poles and dual stopband zeros associated with the LPF [Fig. 16(a)].

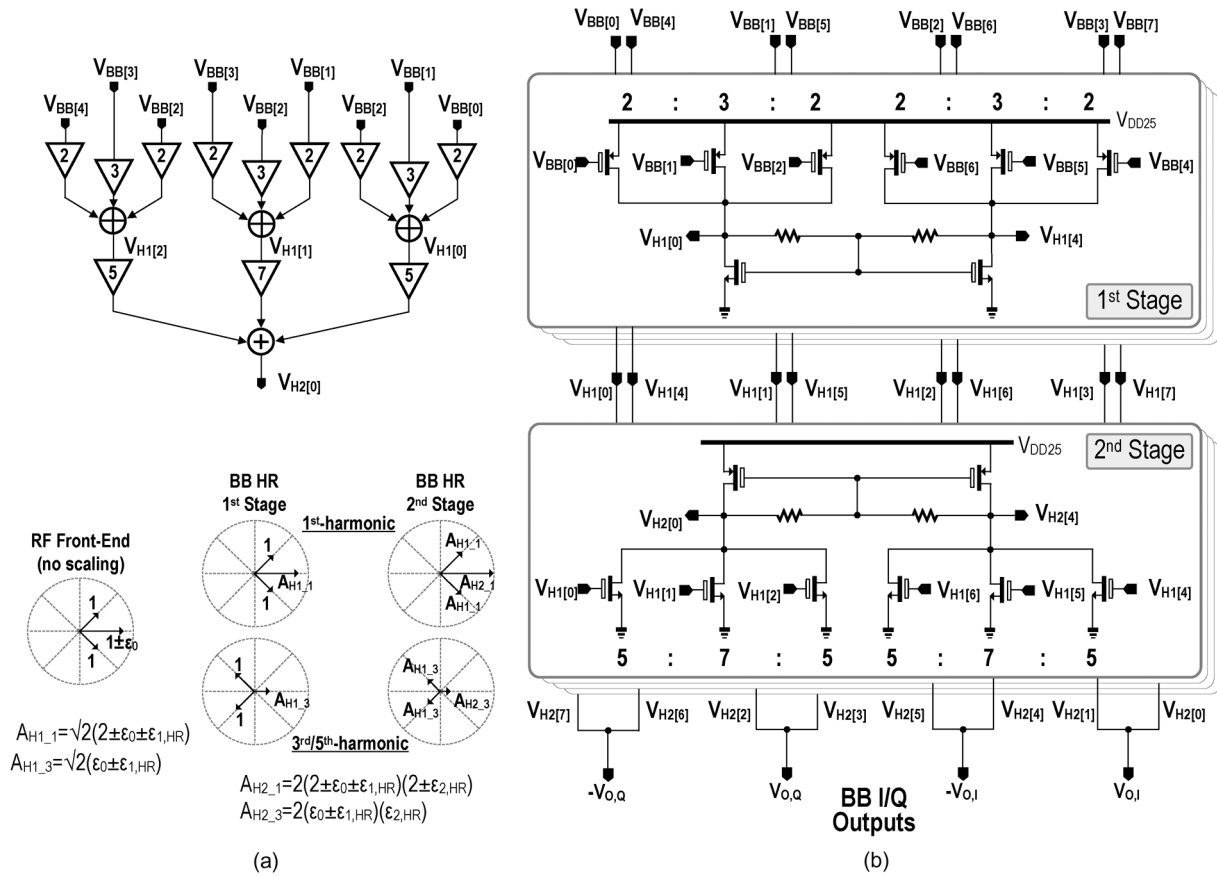


Fig. 11. (a) Block diagram of the 2-stage BB-only HR and its vector diagram; (b) its circuit implementation as a 2-stage HR amplifier.

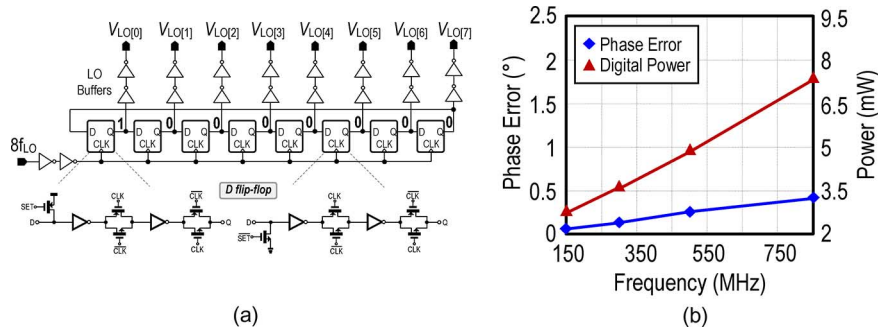


Fig. 12. (a) 8-phase LO generator and (b) its simulated phase error and power versus LO frequency.

The measured HRR_{2-6} from 3 chips are >51 dB without any calibration or trimming [Fig. 16(b)], confirming its improvement over the conventional one-stage BB HR that is normally <45 dB. To prevent 1 dB gain compression at the BB output, the maximum RF input power at the third LO harmonic is -18 dBm.

Although a single-ended RF input can eliminate the external wideband balun and its associated losses, the noise from the LO divider and buffer at fundamental frequency will couple to the RF via the 8-path passive mixer, thus degrading the NF after being downconverted to BB by the mixer as discussed in [9]. This effect is reflected in the measurement of $1/f$ noise versus the intermediate frequency [Fig. 17(a)]. Due to the uncorrelated phase noise of the LO, both $1/f$ noise and thermal noise go up with the RF/LO frequency. The degradation of $1/f$ noise

may come from LO self-mixing, and incomplete $1/f$ noise cancellation of the BB LPF transistors at high frequency. The $1/f$ noise corners are around 100 to 200 kHz comparable to the passive-mixer-first design [2].

D. Blocker Tolerability

The blocker tolerability of the receiver is measured as follows: the CW blocker is given by a signal generator (Agilent E8267D) that has a phase noise of -147 dBc/Hz at $\Delta f = 0.15$ GHz, which is much higher than the kT noise (-174 dBm/Hz). Thus, a 0.7 GHz high-pass filter (Mini-Circuits SHP-700+) should be added at the RF port to suppress such a phase noise [9, Fig. 2], [18]. For the reference LO, it is given by another signal generator (Agilent E4438C) that has a phase noise of -152 dBc/Hz. After div-by-8, the phase noise

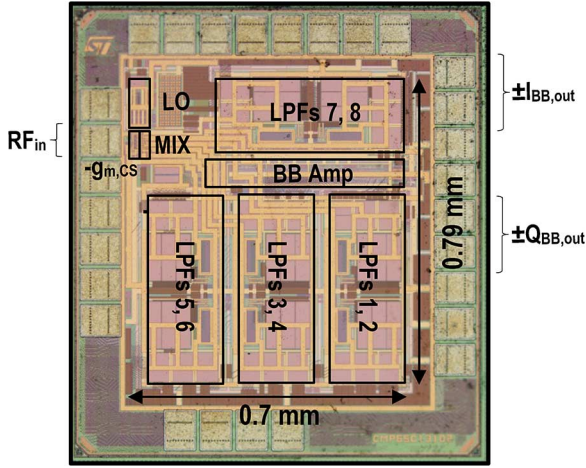
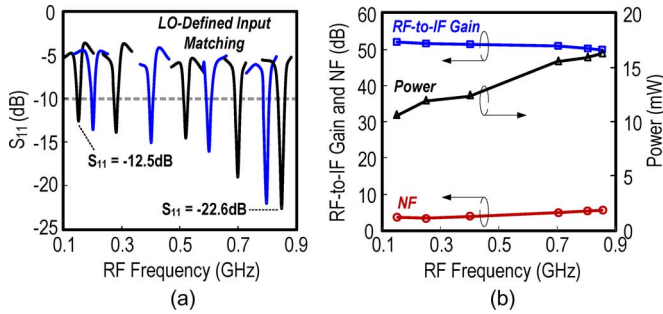
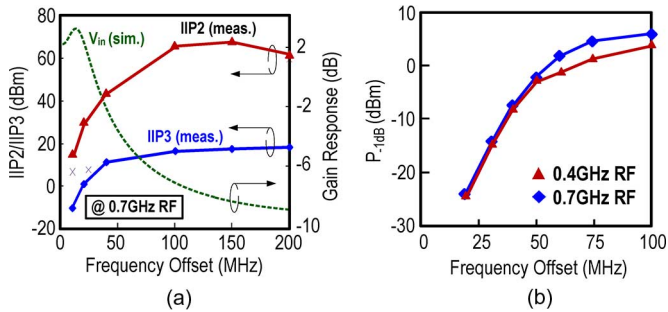


Fig. 13. Chip micrograph of the fabricated receiver in 65 nm CMOS.


 Fig. 14. Measured (a) LO-defined narrowband S_{11} , and (b) RF-to-IF gain, power and NF versus RF frequency.

 Fig. 15. Measured (a) in-band to out-of-band IIP2/IIP3. It obeys the filtering profile provided at V_{in} , and (b) P_{-1dB} versus frequency offset from in-band to out-of-band.

is close to -170 dBc/Hz at $\Delta f = 0.15$ GHz, implying that off-chip filtering is unnecessary for the reference LO, as the phase noise is dominated by the on-chip LO generator here (see Section II-D). Measured at 0.55 GHz ($\Delta f = 0.15$ GHz) and 0.46 GHz RF ($\Delta f = 0.24$ GHz), the blocker NF against the power of the CW blocker at 0.7 GHz are plotted in Fig. 17(b). With the 0.7 GHz high-pass filter offering 18 (35) dB rejection at 0.55 (0.46) GHz, the 0 dBm-blocker NF is around 20 (12) dB. The 18 dB rejection at 0.55 GHz is inadequate to suppress the phase noise from the signal generator to achieve < -174 dBm/Hz, rendering a higher blocker NF. Simulations show that a 0 dBm-blocker degrades the NF by only 1 dB under an ideal LO. When the LO phase noise is included, as

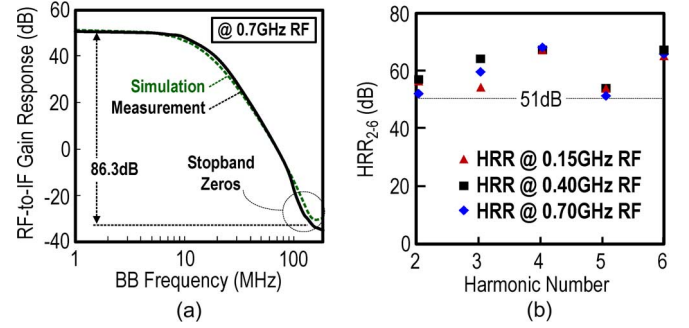
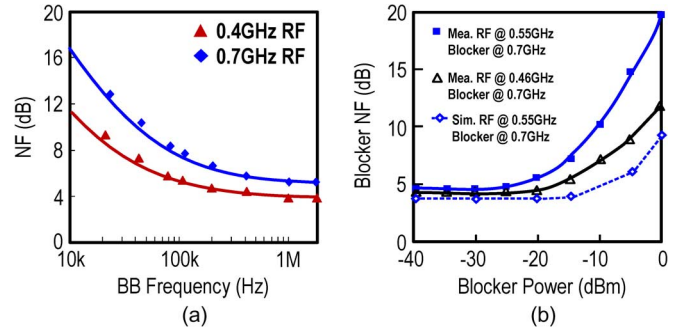

 Fig. 16. Measured (a) RF-to-IF gain response showing the enhanced rejection profile due to the stopband zeros, and (b) HRR_{2-6} without calibration or tuning.


Fig. 17. Measured (a) BB NF; (b) blocker NF.

shown in Fig. 17(b), the simulated blocker NF is < 10 dB. In practices, on top of the reciprocal mixing effect, a large blocker can also saturate M_{CS} , LO phase error can degrade the out-of-band rejection offered by the passive mixers and affect the effectiveness of noise cancelling. To enhance the rejection at a smaller Δf , the area budget (size of $C_{B1,2}$) of the receiver should be increased.

E. LO Reradiation

The measured direct LO reradiation at 0.2 (0.7) GHz is -70 (-67) dBm, and -70 (-66) dBm at the third harmonic at the absence of RF input. The simulated LO reradiation at the 8th harmonic is -47 (-44) dBm at 0.2 (0.7) GHz RF, which is hard to be measured due to the limited PCB isolation between the RF and LO ports.

F. Chip Summary and Comparison

The chip summary is given in Table I. Benchmarking with the state-of-the-art passive-mixer-based receivers [1], [4], [8], [9], this work [19] succeeds in saving the total power consumption without sacrificing the NF, out-of-band linearity and HRR, but the blocker NF is inferior when compared with [9]. Nevertheless, no external components are entailed and strong BB filtering is achieved in a small die size. Besides, its advantages over the active-mixer-based TV-band receiver [12] are also evident as compared in Table II.

IV. CONCLUSIONS

A wideband receiver exploiting parallel N-path active/passive mixers, single-MOS pole-zero LPFs and BB-only two-stage HR amplifiers has been designed and verified in

TABLE I
CHIP SUMMARY AND BENCHMARK WITH RECENT PASSIVE-MIXER-BASED RXS

	This Work and [19]	JSSC'13 [4]	VLSI'13 [8]	ISSCC'12 [9]	ISSCC'09 [1]
RX Architecture	Current-Reuse RF Front-End + Feedforward Passive Mixer	Passive Mixer + BB LNA	RF LNA + Passive Mixer + G_m -C + Op-Amp	2-Path Noise-Cancelling+ Passive-Mixer + OpAmp	RF LNA + Passive Mixer + Op-Amp
Downconversion	Active // Passive	Passive	Passive	Passive	Passive
RF Input Style	Single-Ended	Single-Ended	Differential	Single-Ended	Differential
RF Range (GHz)	0.15 to 0.85	0.7 to 1.6 (8-phase path)	0.4 to 3 (8-phase path)	0.08 to 2.7	0.4 to 0.9
Power (mW) @ RF	10.6 @ 0.15GHz 16.2 @ 0.85GHz	10~12 @ 0.7GHz 10~12 @ 1.6GHz	20 @ 0.4GHz 40 @ 3GHz	37 @ 0.08GHz 70 @ 2.7GHz	49 @ 0.4GHz 60 @ 0.9GHz
DSB NF (dB)	4.6±0.9	10.5±2.5	1.8 to 2.4	1.9±0.4	4±0.5
Ultimate Out-of-Band IIP3 (dBm)	+17.4	+10	+3	+13.5	+16
Ultimate Out-of-Band IIP2 (dBm)	+61* +22/+21**	+26.6	+85 (calibrated)	+54	+56
External Parts	Zero	Zero	Transformer	Zero	2 Inductors and 1 Transformer
Active Area (mm ²)	0.55	2.9 (inc. VCOs)	~0.5 (from Fig.)	1.2	1
BB Filtering Style	2 Complex Poles + 2 Stopband Zeros (Current-Mode)	1 Real Pole (Passive-RC)	2 Real Poles (Active/Passive-RC)	2 Real Poles (Active/Passive-RC)	2 Real Poles (Active-RC)
HRR _{3,5} (dB)	>53, >51	34, 34	70, 55 (calibrated)	42, 45	60, 64
0dBm-Blocker NF (dB)	12 ($\Delta f = 240$ MHz)	N/A	14 ($\Delta f = 80$ MHz)	4.1 ($\Delta f = 80$ MHz)	N/A
BB Bandwidth (MHz)	9	20	0.5 to 50	2	12
RF-to-IF Gain (dB)	51±1	37	36	72	34.4±0.2
Supply (V)	1.2, 2.5	1.3	0.9	1.3	1.2
CMOS Technology	65 nm	65 nm	28 nm	40 nm	65 nm

* Two tones at $[f_{LO} + \Delta f, f_{LO} + \Delta f + 1 \text{ MHz}]$; ** Two tones at $[f_{LO} - \Delta f, \Delta f + 1 \text{ MHz}]/[f_{LO} + \Delta f, \Delta f - 1 \text{ MHz}]$

TABLE II
BENCHMARK WITH AN ACTIVE-MIXER-BASED MOBILE-TV RX

	This Work and [19]	ISSCC'11 [12]
Downconversion	Active // Passive	Active
Power (mW) @ RF	10.6 @ 0.15GHz 16.2 @ 0.85GHz	43 @ 0.17GHz 50 @ 0.86GHz
External Parts	Zero	1 Inductor
BB Filtering Style	2 Complex Poles + 2 Stopband Zeros	2 Complex Poles + 1 Real Pole
HRR _{3,5} (dB)	>53, >51	35, 39
RF-to-IF Gain (dB)	51±1	35±1
DSB NF (dB)	4.6±0.9	4±0.2
IIP3 (dBm)	-12 @ 51dB Gain ($\Delta f = 10$ MHz)	-3.4 @ 35dB Gain ($\Delta f = 10$ MHz)
Active Area (mm ²)	0.55	0.46
Supply (V)	1.2, 2.5	1.2, 2.5
CMOS Technology	65 nm	65 nm

65 nm CMOS. It features an N-path active mixer to enable current-reuse and current-domain signal processing in a stacked RF-to-BB front-end. For the RF filtering, input impedance matching, input biasing and noise cancelling, they are concurrently achieved with the feedforward N-path passive

mixer. High-order BB filtering is merged with the front-end by adopting a single-MOS pole-zero LPF. The BB-only two-stage HR amplifier improves the harmonic rejection with low hardware intricacy. Measurement results verified the merits of this work in balancing the NF and linearity with power and area.

REFERENCES

- [1] Z. Ru, N. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3374, Dec. 2009.
- [2] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
- [3] J. Borremans *et al.*, "A 40 nm CMOS 0.4–6 GHz receiver resilient to out-of-band blockers," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, Jul. 2011.
- [4] C. Andrews *et al.*, "A wideband receiver with resonant multi-phase LO and current reuse harmonic rejection baseband," *IEEE J. Solid-State Circuits*, vol. 48, pp. 1188–1198, May 2013.
- [5] A. Ghaffari *et al.*, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.
- [6] A. Mirzaei *et al.*, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 52–65, Jan. 2012.
- [7] A. Mirzaei *et al.*, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011.

- [8] J. Borremans *et al.*, "A 0.9 V low-power 0.4–6 GHz linear SDR receiver in 28 nm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2013, pp. 146–147.
- [9] D. Murphy *et al.*, "A blocker-tolerant, noise-canceling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, pp. 2943–2963, Dec. 2012.
- [10] S. Blaakmeer *et al.*, "The BLIXER, a wideband balun-LNA-I/Q-mixer topology," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2706–2715, Dec. 2008.
- [11] V. Giannini *et al.*, "A 2-mm² 0.1–5 GHz software-defined radio receiver in 45-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3486–3498, Dec. 2009.
- [12] P.-I. Mak and R. P. Martins, "A 0.46-mm² 4 dB NF unified receiver front-end for full-band mobile TV in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1970–1984, Sep. 2011.
- [13] M. Darvishi *et al.*, "Widely tunable 4th order switched Gm-C band-pass filter based on N-path filters," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3105–3119, Dec. 2012.
- [14] M. Darvishi *et al.*, "Design of active N-path filters," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, Dec. 2013.
- [15] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.
- [16] A. Pirola *et al.*, "Current-mode, WCDMA channel filter with in-band noise shaping," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1770–1780, Sep. 2010.
- [17] J. Greenberg *et al.*, "A 40 MHz-to-1 GHz fully integrated multistandard silicon tuner in 80-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2746–2761, Nov. 2013.
- [18] J. Park and B. Razavi, "A 20 mW GSM/WCDMA receiver with RF channel selection," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 356–357.
- [19] F. Lin, P.-I. Mak, and R. P. Martins, "An RF-to-BB-current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 74–75.



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