A 0.14-mm^2 1.4-mW 59.4-dB-SFDR 2.4-GHz ZigBee/WPAN Receiver Exploiting a "Split-LNTA + 50% LO" Topology in 65-nm CMOS

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***Abstract*—A compact low-power 2.4-GHz ZigBee/wireless personal area network receiver is reported. It optimizes passive pregain with an inverter-based split low-noise transconductance amplifier (split-LNTA) to avoid the RF balun and its associated insertion loss, while enabling isolated in-phase (I)/quadrature (Q) passive mixing. The latter essentially saves power as a 50%-duty-cycle local oscillator (50% LO) can be generated more efficiently than its 25% counterpart. Specifically, a 2.4-GHz *LC* voltage-controlled oscillator (VCO) followed by an input-impedance-boosted Type-II *RC-CR* network produces the desired 50% four-phase LO with optimized power, I/Q accuracy, and phase noise. We also analytically compare the proposed "split-LNTA + 50% LO" architecture with the existing "single-LNTA + 25% LO," identifying their distinct features under current- and voltage-mode operations. The receiver fabricated in 65-nm CMOS exhibits 32-dB voltage gain, 8.8-dB noise figure (NF) and −7-dBm out-band input-referred third-order intercept point that correspond to 59.4-dB spurious-free dynamic range. The VCO measures −111.4-dBc phase noise at 3.5-MHz offset. The achieved power (1.4 mW) and area (0.14 mm^2) efficiencies are favorably comparable with the state-of-the-art.**

***Index Terms*—CMOS, local oscillator (LO), low-noise transconductance amplifier (LNTA), passive mixer, *RC-CR* network, receiver, RF, transimpedance amplifier (TIA), voltage-controlled oscillator (VCO).**

I. Introduction

THE proliferation of short-range wireless applications for Internet of Things and personal healthcare calls for ultra-low power and cost CMOS radios [1]. Ultra-low voltage (ULV) designs have been one of the key directions to approach a better power efficiency [2]–[5]. Regrettably, an ULV supply will limit the voltage swing, and device's f_T and overdrives, deteriorating the spurious-free dynamic range (SFDR) while necessitating area-hungry inductors (or transformers) to assist the bias and tune out the parasitic capacitances. This paper describes the design and implementation of a compact, low-power, and high-SFDR receiver suitable for ZigBee or wireless personal area network (WPAN) applications. The research background can be introduced as follows.

Four potential receiver architectures are shown in Fig. 1. The first [see Fig. 1(a)] employs a single low-noise transconductance amplifier (single-LNTA) followed by two passive in-phase (I) and quadrature (Q) mixers and transimpedance amplifiers (TIAs). If a 50%-duty-cycle local oscillator (50% LO) is applied, this topology can suffer from image current circulation between the I and Q paths, inducing I/Q crosstalk, unequal high-side, and low-side gains, input-referred second-order intercept point (IIP2) and input-referred third-order intercept point (IIP3) [6]. Lowering the LO duty cycle to 25% [see Fig. 1(b)] can alleviate such issues [7] at the expense of extra sine-to-square LO buffers and logic operation. Another alternative is to add two signal buffers before the mixers [see Fig. 1(c)], but they must be linear enough (i.e., more power) to withstand the voltage gain of the low-noise amplifier (LNA) [8], [9]. The basis of our proposed solution [see Fig. 1(d)] is to split the LNTA into two, such that a single-ended RF input is maintained, while allowing isolated passive mixing that facilitates the use of a 50% LO for power savings.

This paper is organized as follows. Section II overviews the operating principle of the proposed "split-LNTA + 50% LO" receiver. An analytical comparison of it with the existing "single-LNTA + 25% LO" architecture is given in Section III. In Section IV, a number of techniques are proposed, including: 1) a low-power voltage-mode TIA to enhance the out-channel linearity both at RF and baseband (BB); 2) a mixed-supply (V_{DD}) design approach [10] to alleviate the design tradeoffs in RF LNTA (power, gain, and noise) and BB TIA (power, linearity, and signal swing); 3) a low-power LO generation scheme that consists of an *LC* voltage-controlled oscillator (VCO), and an *input-impedance-boosted* Type-II *RC–CR* network. They optimize the VCO's output swing with the *LC* tank's quality factor, while offering adequate I/Q accuracy at low power. The measurement results are reported in Section V, and conclusions are drawn in Section VI.

II. Proposed "Split-LNTA + 50% LO" Receiver

The split-LNTA (Fig. 2) is based on two self-biased inverter-based amplifiers (M_1, M_2, and R_F), which have no

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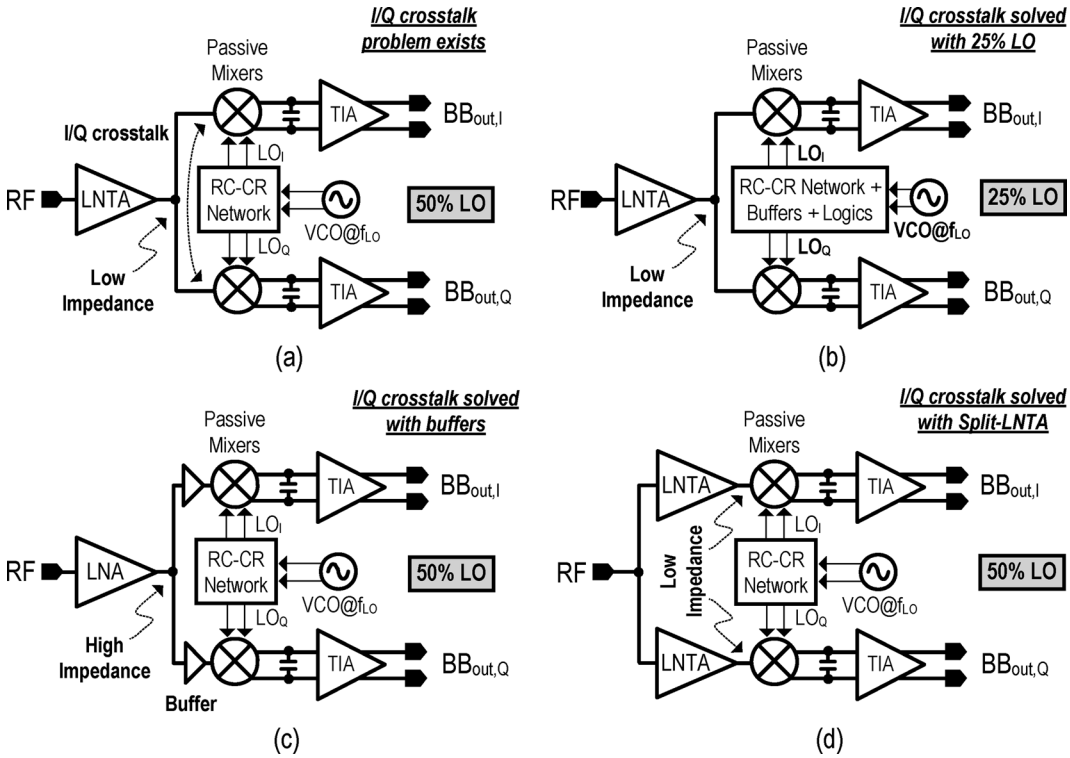

Fig. 1. Four potential receiver architectures. (a) Single-LNTA + 50% LO. (b) Single-LNTA + 25% LO. (c) Single-LNA + 50% LO + signal buffers. (d) Split-LNTA + 50% LO (proposed).

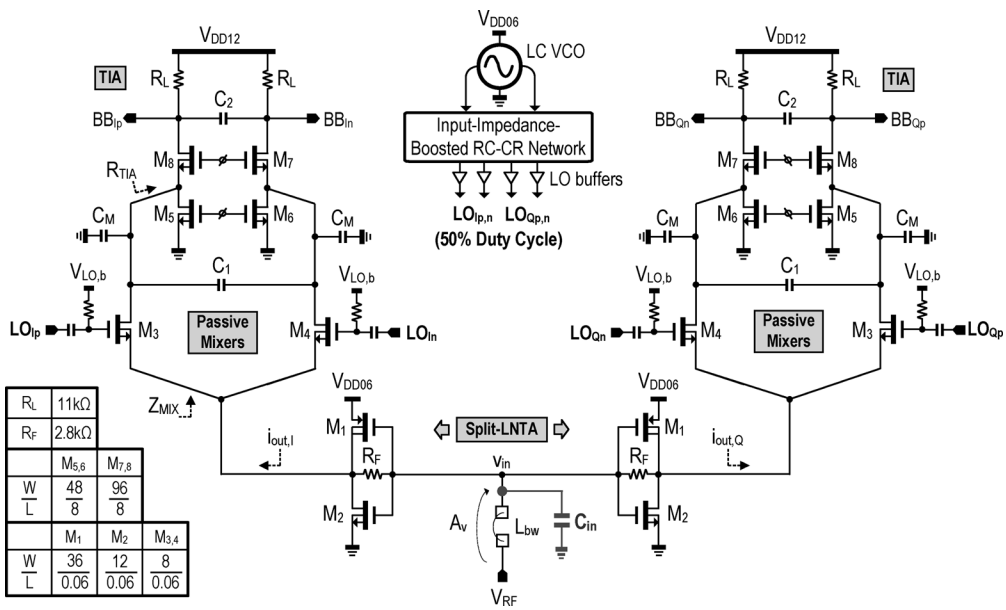

Fig. 2. Schematic of the proposed receiver exploiting passive pre-gain, split-LNTA, passive mixers, 50% LO and common-gate TIAs.

inner parasitic pole. They also can take the speed advantage of fine linewidth CMOS to lower the device overdrive voltages, featuring a high g_m-to-I_d efficiency at low V_{DD} ($V_{DD06} = 0.6$ V). Its single-ended RF input avoids the RF balun and its associated insertion loss. In front of the split-LNTA, a proper co-design between the RF input capacitance ($C_{\rm in}$) and bondwire ($L_{\rm bw}$) facilitates the input impedance matching, while offering a passive pre-gain (A_v) decisively important to the noise figure (NF) and power efficiency. The two LNTAs convert the RF signal ($v_{\rm in}$) into two equal currents $i_{{\rm out},I}$ and $i_{{\rm out},Q}$ for the I and Q channels, respectively. To avoid the parasitics and area impact from ac coupling, $i_{{\rm out},I}$ and $i_{{\rm out},Q}$ are directly dc-coupled to the passive mixers (M_3 and M_4). As long as the dc current passing through M_3 and M_4 is kept small, the $1/f$ noise induced by the mixers can be minimized [11]. This aim can be achieved by matching the output common-mode level of the LNTA to that of the BB TIA.

The 50% four-phase LO ($\rm LO_{Ip,n}$ and $\rm LO_{Qp,n}$) is generated by a 2.4-GHz *LC* VCO followed by a new type-II *RC–CR* network, which features a capacitor divider at the input to boost the input impedance. When driving the LO to the mixers (M_3 and M_4), a proper dc level ($V_{{\rm LO},b}$) can optimize the switching

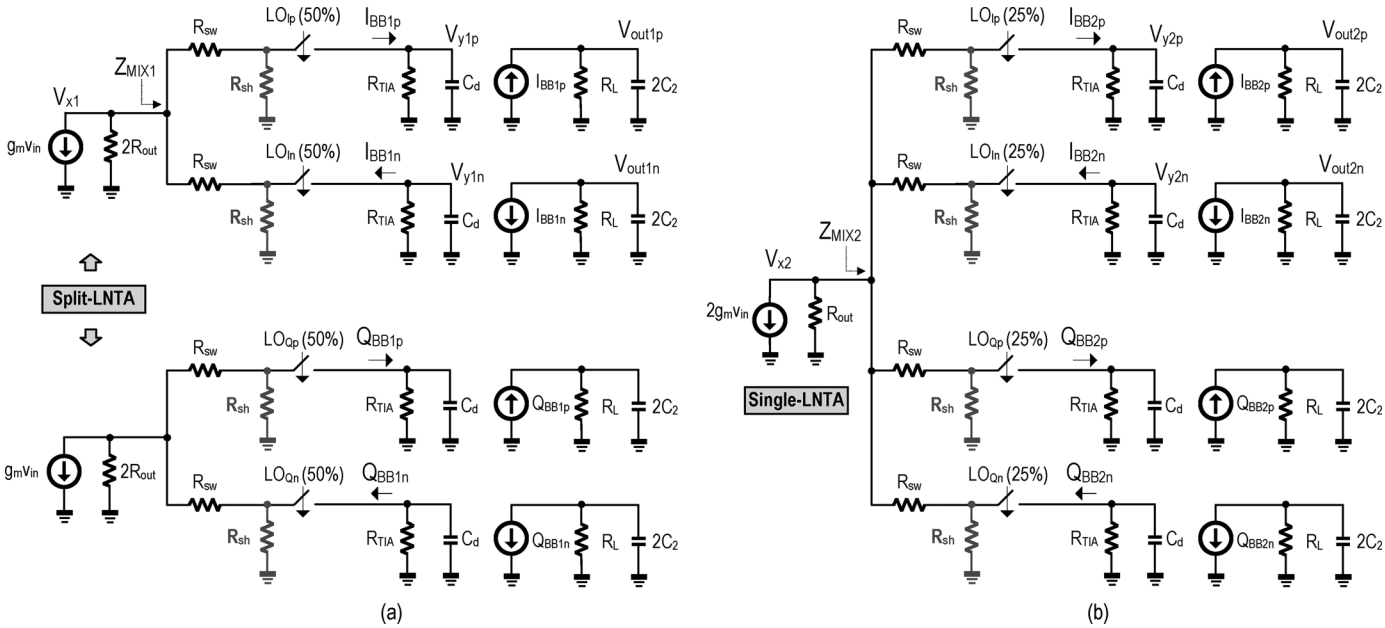

Fig. 3. Small-signal equivalent circuits. (a) Split-LNTA + 50% LO. (b) Single-LNTA + 25% LO.

time. The downconverted low-IF (2 MHz) signal is further amplified by a common-gate TIA (M_{5-8} and R_L), which uses a 1.2-V (V_{DD12}) supply to accommodate more signal swing and enhance linearity. Here, we assume a complex low-IF filter will follow the BB TIA, rendering the $1/f$ noise and IIP2 not significant and will not be further addressed. Due to the bidirectional transparency of passive mixers [7], [8], the BB capacitors (C_1 and C_M) can enhance the selectivity at both RF (the output of the LNTA) and BB, improving the out-band linearity. The grounded C_M also helps to suppress the common-mode RF feedthrough, which is limited by the bondwire inductance that appears in series with C_M under common-mode operation.

III. Comparison of "Split-LNTA + 50% LO" and "Single-LNTA + 25% LO" Architectures

This section presents an analytical comparison of the two architectures: "split-LNTA + 50% LO" and "single-LNTA +25% LO." For brevity, "50% LO" and "25% LO" are exploited to represent them, respectively. Fig. 3(a) and (b) shows their simplified equivalent circuits. For a fair comparison, the two LNTAs in Fig. 3(a) are modeled as g_m (transconductance) and $2R_{\rm out}$ (output resistance), whereas the single LNTA in Fig. 3(b) is modeled as $2g_m$ and $R_{\rm out}$. These models are developed under the same approach described in [12]–[14], where the harmonic up-conversion in passive mixers is modeled as $R_{\rm sh}$. The impedances looking into the 50%-LO and 25%-LO mixers are denoted as $Z_{\rm MIX1}$ and $Z_{\rm MIX2}$, respectively. Each mixer features an on-resistance of $R_{\rm sw}$. $R_{\rm TIA}$ is the input resistance of the TIA. The single-ended differential mode capacitance is denoted as C_d $(= C_M + 2C_1)$.

A. Gain

For Fig. 3(a), we summarize in (1)–(5) the derived expressions of both $Z_{\rm MIX1}$ and the voltage gain (A_{Vx1}) at V_{x1} at the LO + IF frequency ($\omega_{\rm LO} + \omega_{\rm IF}$); the BB output current ($I_{\rm BB1}$) with respect to $v_{\rm in}$; the voltage gain (A_{Vy1}) at $V_{y1p,n}$, and finally, the voltage gain ($A_{V\rm out1}$) at $V_{\rm out1p,n}$,

$$Z_{\rm MIX1}|@(\omega_{\rm LO}+\omega_{\rm IF}) \approx R_{\rm sw} + \left(\frac{2Z_{\rm BB}}{\pi^2}//R_{\rm sh}\right) \tag{1}$$

where

$$\begin{aligned} Z_{\rm BB} &= \frac{1}{s(2C_1+C_M)}//R_{\rm TIA} \\ R_{\rm sh} &\approx \frac{2}{3}(2R_{\rm out}+R_{\rm sw}) \\ A_{Vx1}@(\omega_{\rm LO}+\omega_{\rm IF}) &\approx g_m(2R_{\rm out}//Z_{\rm MIX1}) \end{aligned} \tag{2}$$

$$\begin{aligned} \frac{I_{\rm BB1}}{v_{\rm in}}@{\rm DC} &= \frac{I_{\rm BB1p}-I_{\rm BB1n}}{v_{\rm in}} \\ &\approx g_m \frac{2R_{\rm out}}{R_{\rm TIA}+2(2R_{\rm out}+R_{\rm sw})}\frac{4}{\pi} = G_{m1} \end{aligned} \tag{3}$$

$$A_{Vy1}@{\rm DC} = A_{Vy1p} - A_{Vy1n} \approx G_{m1}R_{\rm TIA} \tag{4}$$

$$A_{V\rm out1}@{\rm DC} = A_{V\rm out1p} - A_{V\rm out1n} \approx G_{m1}R_L. \tag{5}$$

Similarly, for Fig. 3(b), we have (6)–(10), the derived expressions of both $Z_{\rm MIX2}$ and the voltage gain (A_{Vx2}) at V_{x2} at the LO + IF frequency ($\omega_{\rm LO} + \omega_{\rm IF}$); the BB output current ($I_{\rm BB2}$) with respect to $v_{\rm in}$; the voltage gain (A_{Vy2}) at $V_{y2p,n}$, and finally, the voltage gain ($A_{V\rm out2}$) at $V_{\rm out2p,n}$,

$$Z_{\rm MIX2}|@(\omega_{\rm LO}+\omega_{\rm IF}) \approx R_{\rm sw} + \left(\frac{2Z_{\rm BB}}{\pi^2}//R_{\rm sh}\right) \tag{6}$$

where

$$\begin{aligned} Z_{\rm BB} &= \frac{1}{s(2C_1+C_M)}//R_{\rm TIA} \\ R_{\rm sh} &\approx 4(R_{\rm out}+R_{\rm sw}) \\ A_{Vx2}@(\omega_{\rm LO}+\omega_{\rm IF}) &\approx 2g_m(R_{\rm out}//Z_{\rm MIX2}) \end{aligned} \tag{7}$$

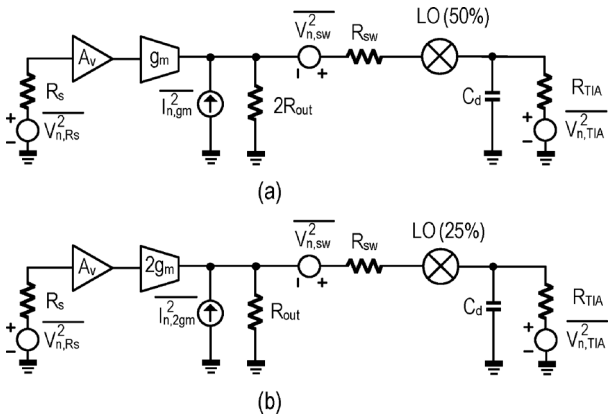

Fig. 4. Equivalent LTI noise model with pre-gain for: (a) 50% LO [see Fig. 3(a)] and (b) 25% LO [see Fig. 3(b)].

$$\frac{I_{\rm BB2}}{v_{\rm in}}@{\rm DC} = \frac{I_{\rm BB2p} - I_{\rm BB2n}}{v_{\rm in}} \approx 2g_m \frac{R_{\rm out}}{R_{\rm TIA} + 4(R_{\rm out} + R_{\rm sw})} \frac{4\sqrt{2}}{\pi} = G_{m2} \quad (8)$$

$$A_{Vy2}@{\rm DC} = A_{Vy2p} - A_{Vy2n} \approx G_{m2} R_{\rm TIA} \quad (9)$$

$$A_{V{\rm out}2}@{\rm DC} = A_{V{\rm out}2p} - A_{V{\rm out}2n} \approx G_{m2} R_L. \quad (10)$$

Note that the output capacitance of the LNTA was neglected. In fact, the output capacitance of LNTA will induce $C_{\rm out}$ and $2C_{\rm out}$ for the g_m and $2g_m$ LNTA stages, respectively. This will render the output impedance ratio at V_{x1} and V_{x2} slightly larger than 2. Besides, the parasitic capacitor will also affect $R_{\rm sh}$. The proposed separated g_m stage imposes a smaller $C_{\rm out}$ and thus lowers the degradation of gain and NF than those predicted by (11) and (12). With proper sizing, one can achieve $R_{\rm sw} \ll R_{\rm out}$ and $R_{\rm sw} \ll R_{\rm TIA}$ and R_L, such that the gain difference between 25% LO and 50% LO at different RF and BB nodes can be estimated as

$$\begin{aligned} A_{Vx1,2}@\omega_{\rm LO} &= 20\log A_{Vx2} - 20\log A_{Vx1} \\ &\approx 20\log \frac{2\left(R_{\rm out} // \frac{2R_{\rm TIA}}{\pi^2} // 4R_{\rm out}\right)}{2R_{\rm out} // \frac{2R_{\rm TIA}}{\pi^2} // \frac{4R_{\rm out}}{3}} \\ &= 6 \text{ dB} \\ \Delta A_{Vy1,2}@{\rm DC} &= 20\log A_{Vy2} - 20\log A_{Vy1} \\ &= 20\log\left(\sqrt{2}\frac{R_{\rm TIA} + 4R_{\rm out} + 2R_{\rm sw}}{R_{\rm TIA} + 4R_{\rm out} + 4R_{\rm sw}}\right) \\ &\approx 3 \text{ dB} \\ \Delta A_{V{\rm out}1,2}@{\rm DC} &= 20\log A_{V{\rm out}2} - 20\log A_{V{\rm out}1} \\ &= 20\log\left(\sqrt{2}\frac{R_L + 4R_{\rm out} + 2R_{\rm sw}}{R_L + 4R_{\rm out} + 4R_{\rm sw}}\right) \\ &\approx 3 \text{ dB}. \end{aligned} \quad (11)$$

From (11), the 25% LO should have a higher gain at both RF and BB nodes than the 50% LO. However, as analyzed in Section III-C, a higher gain at RF will penalize the IIP3, while a higher BB gain can be achieved easily by using a larger R_L. For the impact of these gain differences to NF, we analyze them next.

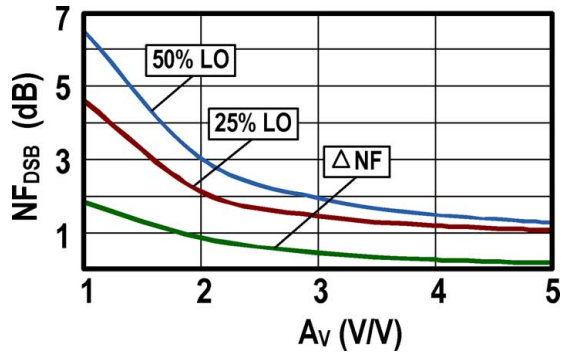

Fig. 5. Simulated $\rm NF_{DSB}$ and ΔNF against A_v for 50% LO and 25% LO.

B. NF

The NF is analyzed according to the equivalent LTI noise model [12]–[14]. As shown in Fig. 4(a) and (b), the four noise sources are the thermal noises from $R_s(V^2_{n,Rs} = 4kTR_s)$, LNTA($I^2_{n,g_m} = 4kT\gamma_1 g_m$ *or* $I^2_{n,2g_m} = 4kT\gamma_1 2g_m$), $R_{\rm sw}(V^2_{n,\rm sw} = 4kTR_{\rm sw})$ and the noise from the TIA is $V^2_{n,\rm TIA} \approx 4kT\gamma_2/g_{m\_\rm TIA} \approx 4kT\gamma_2 R_{\rm TIA}$, given that the output impedance of the mixer is sufficiently large. Here, $g_{m\_\rm TIA}$ is the transconductance of the bias transistor for the TIA, while the noise from the CG device is degenerated. An accurate model of the TIA noise can be found elsewhere[11]. The noise of R_F is ignorable and the noise coupling between the I and Q paths under a 50% LO is minor (confirmed by simulations), easing the NF calculation of each path separately. The noise factor (F) can be found by dividing the total output noise by the portion contributed by R_s,

$$F = 1 + \frac{\gamma_1}{R_s A_v^2 G_m} + \frac{R_{\rm sw}}{R_s A_v^2 G_m^2 R^2} + \frac{(R+R_{\rm sw})^2}{R_s A_v^2 G_m^2 R^2 \beta\gamma_2 R_{\rm TIA}} + \frac{a\gamma_1}{R_s A_v^2 G_m} + a + \frac{aR_{\rm sw}}{R_s A_v^2 G_m^2 R^2} \quad (12)$$

where $\beta = 2/\pi^2$ is the down-conversion scaling factor and a is the harmonic folding factor

$$a = \left(\frac{\pi^2}{4} - 1\right),\ G_m = g_m,\ \text{and } R = 2R_{\rm out} \text{ for Fig. 4(a)}$$

$$a = \left(\frac{\pi^2}{8} - 1\right),\ G_m = 2g_m,\ \text{and } R = R_{\rm out} \text{ for Fig. 4(b).}$$

In (12), the second term is from the LNTA, the third term is from the mixer, and the fourth term is from the TIA. The rest of the terms are the noise folding from the odd harmonics of the LO for the LNTA, R_s and $R_{\rm SW,}$ respectively. The NF calculated from (12) for 50% LO is single sideband (SSB). For a double-sideband (DSB) NF, it is 3 dB less. Since the harmonic's power of the 50% LO is larger than that of the 25% LO, the folding terms of the 50% LO are also higher. From (12), one can plot the DSB NF of the 50% LO and 25% LO in Fig. 5 as a function of A_V, where $\Delta{\rm NF} = NF_{50\%} - NF_{25\%}$, $R_{\rm sw} = 50\,\Omega$, $\gamma_1 = \gamma_2 = 1$, $g_m = 9$ mS, $R_{\rm out} = 200\ \Omega$, and $R_{\rm TIA} = 2.5$ kΩ. It can be seen that ΔNF is reduced to 0.91 dB (0.51 dB) when A_V is just 2 V/V (3 V/V), which is easily achievable in practice. In fact, a moderated A_V can even eliminate the need of the LNTA (or LNA) [3]. However, when also considering the input matching and LO-to-RF isolation, both pre-gain and the LNTA should

be employed concurrently. The simulated LO-to-RF isolation is < -100 dBm. Due to the passive pre-gain, the IIP3 of the receiver is more demanding than the NF, promoting the use of a 50% LO. Together with its power advantage (i.e., lower VCO frequency and no divider), our proposed topology (i.e., pre-gain + split-LNTA + 50% LO) should ease the tradeoff between the NF, IIP3, area, and power.

C. IIP3

The third-order intermodulation (IM3) distortion is analyzed to assess the linearity. The aim is to find the in-band IIP3 of the receiver under 50% LO and 25% LO in response to two-tone excitation. Assuming that the nonlinearity of the receiver is dominated by the LNTA, its nonlinearity contributions are considered as follows:

a) third-order LNTA nonlinearity due to input excitation $v_{\rm in}$ $[\alpha_2(I/V^3)]$;
b) third-order LNTA nonlinearity due to output excitation v_x $[\alpha_3(I/V^3)]$.

Thus, $i_{\rm ds} = \alpha_1 v_{\rm in} + \alpha_2 v_{\rm in}^3 + \alpha_3 v_X^3$. If the coefficients α_1, α_2, and α_3 are assumed to be proportional to the device W/L.

For 50% LO, $\alpha_1 = g_m, \alpha_2 = g_{m3}, \alpha_3 = g_{o3}$.

For 25% LO, $\alpha_1 = 2g_m, \alpha_2 = 2g_{m3}, \alpha_3 = 2g_{o3}$.

g_{m3} and g_{03} are the third-order nonlinear transconductance and conductance, respectively. With a two-tone excitation of amplitude A and the first-order voltage gain and current gain given in (1)–(11), the IM3 output voltage for each of the nonlinear coefficients listed above can be written as

$$v_{o3\alpha 2} = \frac{3}{4} g_{m3} A^3 I_{\rm BB1} R_L;\; v_{o3\alpha 3} = \frac{3}{4} g_{o3} A_{Vx1}^3 A^3 I_{\rm BB1} R_L$$

for a 50% LO. Thus,

$$\begin{aligned} {\rm IM}_{3\_50\%} &= \frac{v_{o3\alpha 2} + v_{o3\alpha 3}}{v_{01\alpha 1}} \\ &= \frac{\frac{3}{4} g_{m3} A^3 I_{\rm BB1} R_L + \frac{3}{4} g_{o3} A_{Vx1}^3 A^3 I_{\rm BB1} R_L}{A g_m I_{\rm BB1} R_L}. \end{aligned}$$

Let

$${\rm IM}_{3\_50\%} = 1 \rightarrow {\rm IIP}_{3\_50\%} = \sqrt{\frac{4 g_m}{3(g_{m3} + g_{o3} A_{Vx1}^3)}}. \quad (13)$$

Following the same procedure, the IIP3 for 25% LO can be derived as

$${\rm IIP}_{3\_25\%} = \sqrt{\frac{4 g_m}{3(g_{m3} + g_{o3} A_{Vx2}^3)}}. \quad (14)$$

Since $A_{Vx2} > A_{Vx1}$, we can find that, from (13) and (14), the LNTA's third-order nonlinearity term is larger for a 25% LO. Thus, the IIP3 of the 50% LO should be better than that of the 25% LO, benefiting the SFDR since both architectures will feature a similar NF after adding the pre-gain.

D. Current- and Voltage-Mode Operations

Both 25% LO and 50% LO architectures can be intensively designed for current- or voltage-mode operation. For a *high-performance* design like [7], [8], and [12], $R_{\rm TIA} \ll R_{\rm out}$ and $R_{\rm sw} \ll R_{\rm out}$ are preferred to keep the signals in the deep current mode. As such, (3) and (8) can be simplified as $G_{m1} = 2g_m/\pi$ and $G_{m2} = 2\sqrt{2} g_m/\pi$, respectively. Both of them are higher when compared to themselves in the voltage-mode operation. In terms of IIP3 and NF, the current mode is also preferable since $A_{Vx1} \approx g_m(R_{\rm sw} + (2/\pi^2)R_{\rm TIA})$ and $A_{Vx2} \approx 2g_m(R_{\rm sw} + (2/\pi^2)R_{\rm TIA})$ will be lower, and the noise due to the folding term and TIA will be also smaller, as noted in (12).

Nevertheless, the current-mode operation also brings up two sizing constraints being less attractive for *low-power* design, which are: 1) a low $R_{\rm sw}$ entails a large device W/L and a higher overdrive voltage for the mixers; both calling for a larger power budget in the LO path and 2) a low $R_{\rm TIA}$ implies that the TIA has to draw a large bias current. For example, if a low $R_{\rm TIA}$ of 50 Ω is required from the 1.2-V TIA (a common-gate amplifier), its bias current is as high as $I_{\rm bias} = 2$ mA for a typical overdrive voltage of 200 mV. Thus, for *ultra-low-power* applications like Zigbee/WPAN that has relaxed NF and linearity requirements, higher $R_{\rm sw}$ and $R_{\rm TIA}$ are preferable to operate the receiver *more* on the voltage mode. A summary of performance differences in current- and voltage-mode operations is given in Table I.

TABLE I
PROPOSED RECEIVER UNDER CURRENT- AND VOLTAGE-MODE OPERATIONS

Mode	Gain	NF	In-Band IIP3	Power	Suitable for
Current Mode (Small $R_{\rm sw}$ & $R_{\rm TIA}$)	↗	↘	↗	↗	High Performance
Voltage Mode (Large $R_{\rm sw}$ & $R_{\rm TIA}$)	↘	↗	↘	↘	Ultra Low Power

IV. CIRCUIT TECHNIQUES

A. Impedance Up-Conversion Matching

From Section III, we expect a passive pre-gain A_v of 2–3 V/V. As shown in Fig. 6(a), A_v can be derived under $R_{\rm in} = R_s$,

$$\frac{V_{\rm out}^2}{2R_{\rm out}} = \frac{V_s^2}{8R_s},\; V_{\rm out} = V_{\rm in} A_v, V_{\rm in} = 0.5 V_s \Rightarrow A_v = \sqrt{\frac{R_{\rm out}}{R_{\rm in}}}.$$

Thus, an *up-conversion* matching network is entailed to ensure $A_v > 1$. A convenient way to achieve it is to use $L_{\rm bw}$ to resonant with $C_{\rm in}$. The schematic is shown in Fig. 6(b). The parallel connection of $C_{\rm in}$ and $R_{\rm out}$ can be transformed into a series connection of $C_{\rm ser}$ and $R_{\rm ser}$, as shown in Fig. 6(c). At $L_{\rm bw} C_{\rm ser}$ resonance, and with $R_{\rm ser} = R_s$ and $i = V_s/2R_{\rm ser}$, we have

$$V_{\rm out} = V_{R_{\rm ser}} + V_{C_{\rm ser}} = \frac{V_S}{2}\left(1 - j\frac{Q_C}{2}\right)$$

where

$$\begin{aligned} V_{R_{\rm ser}} &= -j\frac{Q_C V_s}{2} s C_{\rm ser} R_{\rm ser} = \frac{V_s}{2} \\ V_{C_{\rm ser}} &= \frac{1}{j\omega_0 C_{\rm ser}} \frac{V_s}{2R_{\rm ser}} = -j\frac{Q_C}{2} V_s, \\ \omega_0 &= \frac{1}{\sqrt{L_{\rm bw} C_{\rm ser}}} \text{ and } Q_C = \frac{\sqrt{\frac{L_{\rm bw}}{C_{\rm ser}}}}{R_{\rm ser}}. \end{aligned}$$

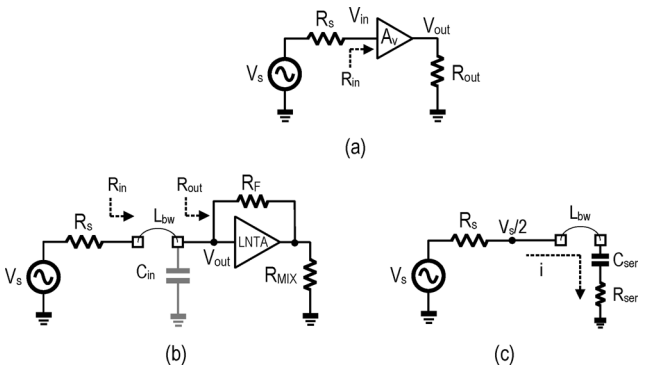

Fig. 6. Input impedance matching. (a) A_v converts $R_{\rm out}$ to $R_{\rm in}$ to match with R_s. (b) $L_{\rm bw}$ $C_{\rm in}$ as an impedance conversion network and its (c) narrowband equivalent circuit.

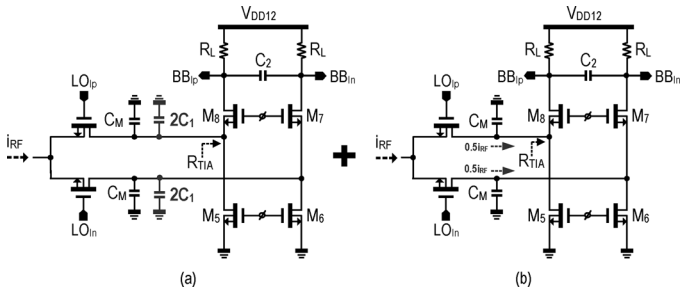

Fig. 7. Equivalent circuits of the mixer-TIA interface for the: (a) differential low-IF signal and (b) common-mode RF feedthrough.

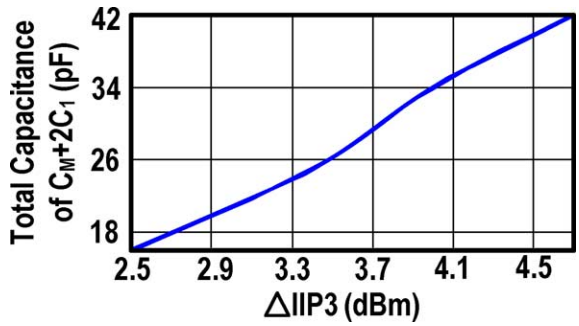

Fig. 8. Out-band IIP3 can be improved by allowing more total capacitance of $C_M + 2C_1$.

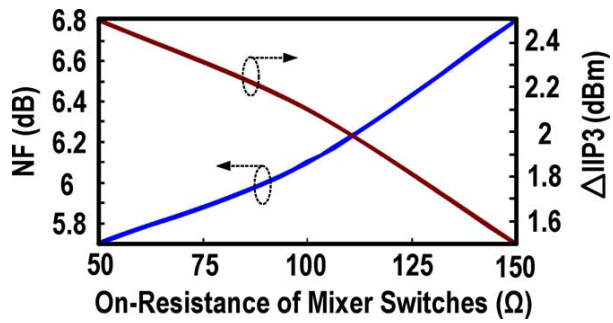

Fig. 9. On-resistance of the mixer switches represents a tradeoff among the LO-path's power, out-band IIP3, and NF.

Interestingly, such a voltage boosting factor $\sqrt{1+Q_c^2/4}$ is larger than the conventional inductively degenerated LNA, which is only $Q_C/2$. In fact, when the capacitance of the printed circuit board (PCB) trace is accounted, the Q of the matching network will be higher, easing the impedance matching.

B. Mixer-TIA Interface Biased for Impedance Transfer Filtering

For the employed single-balanced passive mixers, the RF-to-IF feedthrough has to be addressed. Based on Fig. 7, we can calculate the currents i_{M7} and i_{M8} with respect to the RF current $i_{\rm RF}$ as given by

$$i_{M7} = \frac{i_{\rm RF}}{2}[1 - \text{sign}\,(\cos\omega_{\rm LO}t)] \tag{15}$$

$$i_{M8} = \frac{i_{\rm RF}}{2}[1 + \text{sign}\,(\cos\omega_{\rm LO}t)]. \tag{16}$$

They imply that the currents can be decomposed into the differential mode [see Fig. 7(a)] with an amplitude of $2i_{\rm RF}/\pi$ at BB, and into the common mode [see Fig. 7(b)] with an amplitude of $0.5i_{\rm RF}$ at RF. To suppress the latter, C_M was added to create a low-pass pole ($C_M//R_{\rm TIA}$). For the differential IF signal, the pole is located at $(C_M + 2C_1)//R_{\rm TIA}$, which suppresses the out-of-channel interferers before they enter the TIA. As such, the TIA can be biased under a very small bias current. The resultant high input impedance of the TIA, indeed, benefits both BB and RF filtering because of the bidirectional impedance-translation property of the passive mixers [7], [8]. Fig. 8 shows the simulated out-band IIP3, which is subject to the allowed total capacitance of $C_M + 2C_1$. For instance, when $C_M + 2C_1$ is increased from 16 to 42 pF, the out-band IIP3 raises from +2.5 to +4.7 dBm at the expense of the die area. For the on-resistance of the mixer switches ($R_{\rm sw}$), it involves a tradeoff of the LO path's power to the out-band IIP3 and NF. As shown in Fig. 9, if $R_{\rm sw}$ is increased from 50 to 150 Ω for power savings, the NF and out-band IIP3 will be penalized by ∼ 1 dB.

C. RC–CR Network and VCO Co-Design

The *LC* VCO [see Fig. 10(a)] employs a complementary NMOS–PMOS (M_{1-4}) negative transconductor. For power savings, M_1 and M_2 are based on ac-coupled gate bias ($V_{{\rm vco},b}$) to lower the supply to 0.6 V. Here, we implement a capacitive divider (C_{M1} and C_{M2}) to boost the input impedance of its subsequent two-stage *RC–CR* network [see Fig. 10(b)]. The optimization details are presented next.

The *RC–CR* network is excellent for low-power and narrowband I/Q generation. With a Type-II architecture, both phase balancing and insertion loss can be better optimized than its Type-I counterpart [15]. For instance, the simulated insertion loss of a two-stage Type-II *RC–CR* network is roughly 2 dB, as shown in Fig. 11, which will be raised to 4–5 dB if a Type-I topology is applied (not shown). For low-power LO buffering, the amplitude balancing is critical because its imbalance will lead to inconsistent zero-crossing points, resulting in AM to duty-cycle distortion. Fig. 12 (V_{RC1-4}) and Fig. 13 ($\text{LO}_{Ip,n}$ and $\text{LO}_{Qp,n}$) are the simulated transient waveforms, showing the consistent duty cycle and zero-crossing points achieved in the proposed design.

For an *RC–CR* network operated at 2.4 GHz, if we select $R_{N1} = 1$ kΩ, C_{N1} is just 66 fF, which benefits the area, VCO

	$M_{1,2}$	$M_{3,4}$	L_P	C_{M1}	C_{M2}	R_{N1}	C_{N1}	R_{N2}	C_{N2}
$\frac{W}{L}$	$\frac{12}{0.12}$	$\frac{24}{0.12}$	4.6nH	530fF	280fF	450Ω	35fF	900Ω	120fF

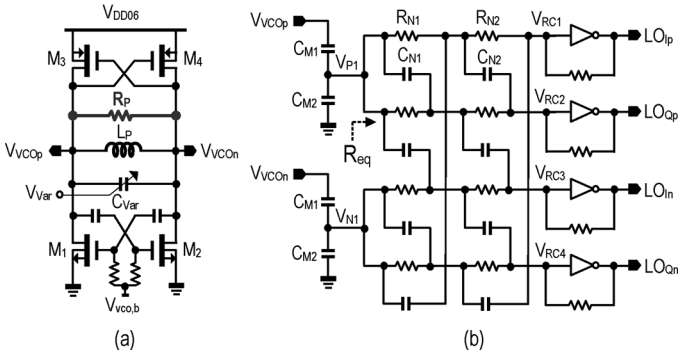

Fig. 10. (a) *LC* VCO and (b) proposed input-impedance-boosted two-stage Type-II *RC–CR* network for four-phase 50% LO generation.

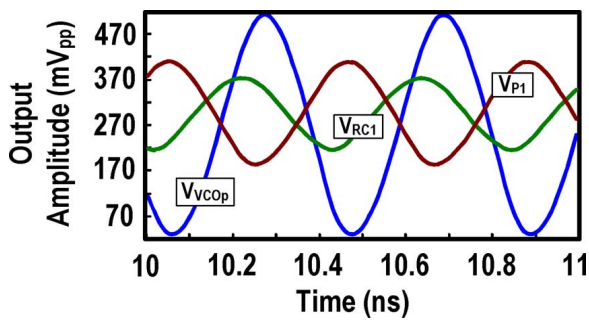

Fig. 11. Simulated time-domain signals at the output of the VCO ($V_{\mathrm{VCO}p}$), capacitor divider (V_{p1}), and the *RC–CR* network (V_{RC1}).

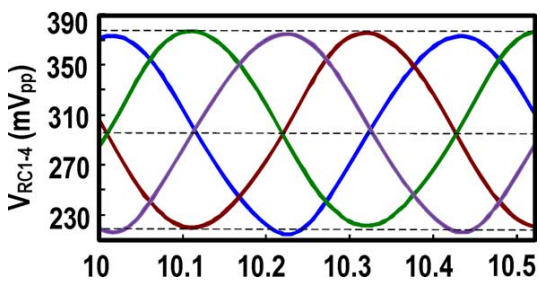

Fig. 12. Simulated time-domain signals at V_{RC1-4}.

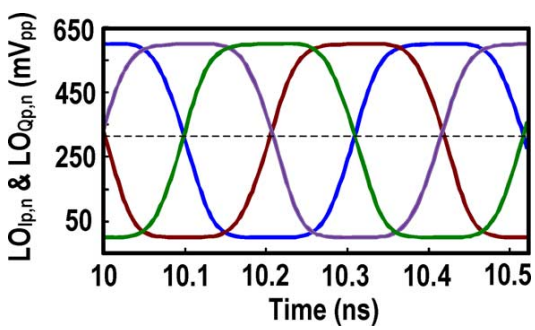

Fig. 13. Simulated time-domain signals at $\mathrm{LO}_{Ip,n}$ and LO_{Qp-n}.

tuning range, and phase noise, but the I/Q accuracy over PVT variations should be considered [16]

$$\frac{\sigma\,(\text{Image Out})}{\text{Desired Out}} = 0.25\sqrt{\left(\frac{\sigma_R}{R}\right)^2 + \left(\frac{\sigma_C}{C}\right)^2}. \tag{17}$$

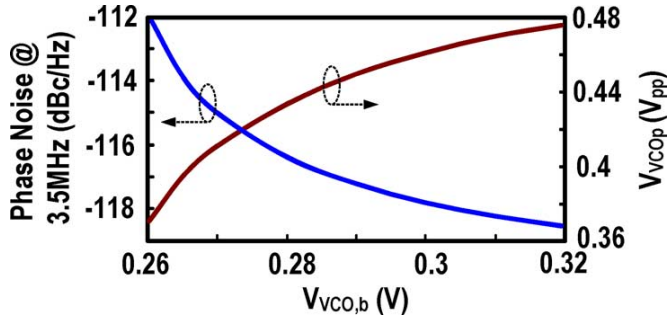

Fig. 14. Tradeoff between VCO output amplitude and phase noise with respect to $V_{\mathrm{vco},b}$.

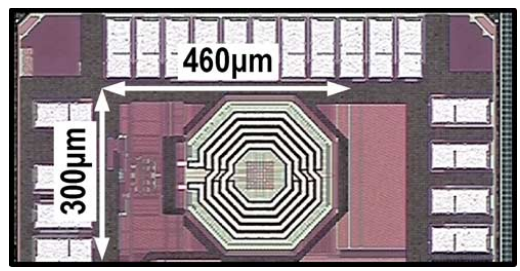

Fig. 15. Chip micrograph of the fabricated receiver.

Since ZigBee/WPAN applications call for a low image-rejection ratio (IRR) of 20–30 dB [17], according to (17), the matching of the resistors (σ_R) and capacitors (σ_C) can be relaxed to 2.93% for a 30-dB IRR (3σ). The sizes of $C_{N1,2}$ and $R_{N1,2}$ are summarized in Fig. 10. The poles from $C_{N1,2}$ and $R_{N1,2}$ are distributed around 2.4 GHz to cover the PVT variations. The impact of R_{N1} to the VCO can be analyzed as follows.

When the VCO's inductor is 4 nH with a Q of 20 ($R_P \approx 1.2$ kΩ), we have $R_{\mathrm{tank}} \approx 0.5R_P//0.5R_{N1}$. Thus, directly connecting the *RC–CR* network to the VCO will limit the *LC* tank's Q_{tank} degrading the phase noise [18], [19]. To alleviate this, we boost up the equivalent input resistance of the *RC–CR* network (R_{eq}) by adding a capacitive divider (C_{M1} and C_{M2}). For the total tank capacitance C_{tank}, it can be approximated as

$$C_{\mathrm{tank}} \approx 2C_{\mathrm{Var}} + \frac{(C_{M2} + 2C_{N1})\,C_{M1}}{C_{M1} + C_{M2} + 2C_{N1}}. \tag{18}$$

By defining an input-impedance boosting factor n,

$$n = \frac{C_{M1}}{C_{M1} + C_{M2} + 2C_{N1}} \tag{19}$$

we have

$$V_{P1} \approx nV_{\mathrm{VCO}p}. \tag{20}$$

It means that the signal swing (V_{P1}) delivered to the *RC–CR* network are in tradeoff with n. Handily, in our VCO, sweeping $V_{\mathrm{vco},b}$ can track the phase noise with the output swing (Fig. 14). Given a bias current and a phase-noise target, R_{tank} can be set from $V_{\mathrm{VCO}p} \approx 2I_{\mathrm{bias}}R_{\mathrm{tank}}$, and n can be set from (21) with a specific R_p and R_{eq},

$$R_{\mathrm{tank}} \approx \frac{R_{\mathrm{eq}}}{n} \parallel \frac{R_P}{2}. \tag{21}$$

In this work, $n = 0.6$ is selected to balance the output swing with C_{tank} and the total tank resistance (R_{tank}).

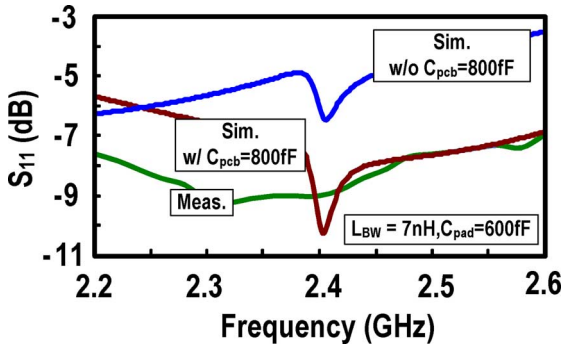

Fig. 16. Measured S_{11}, and simulated S_{11} with and without $C_{\rm pcb}$.

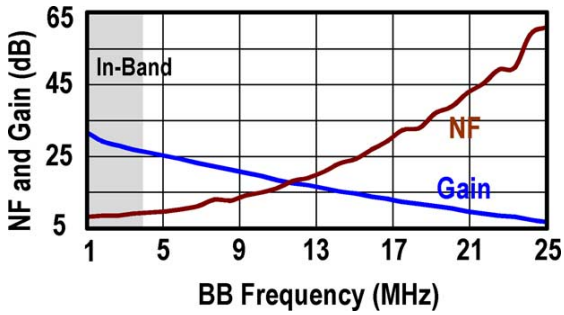

Fig. 17. Measured receiver gain and NF versus BB frequency.

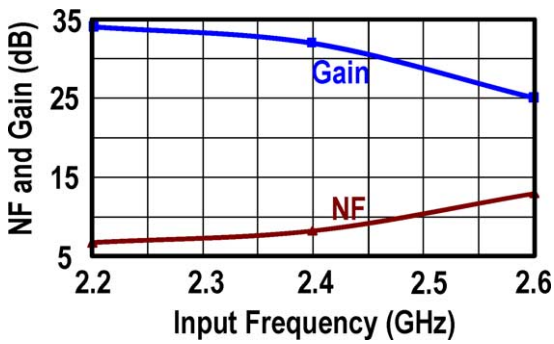

Fig. 18. Measured receiver gain and NF versus input signal frequency.

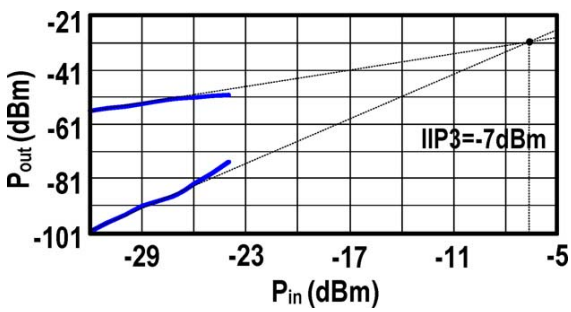

Fig. 19. Measured out-of-band IIP3.

V. Experimental Results

The receiver (Fig. 15) fabricated in 65-nm CMOS occupies an active area of 0.14 mm^2 and is encapsulated in a 44-pin CQFP package for PCB-based measurements. The estimated bondwire inductance is $\sim$ 7 nH for the provided package (13.5 $\times$ 13.5 mm). Fig. 16 shows that the measured S_{11} is -8 dB within 2.24–2.46 GHz (for a different package, an external inductor or capacitor can be added to optimize S_{11}). The simulation results with and without considering the PCB trace capacitances

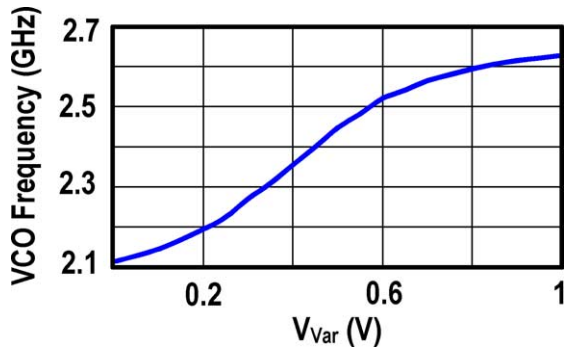

Fig. 20. Measured VCO turning range.

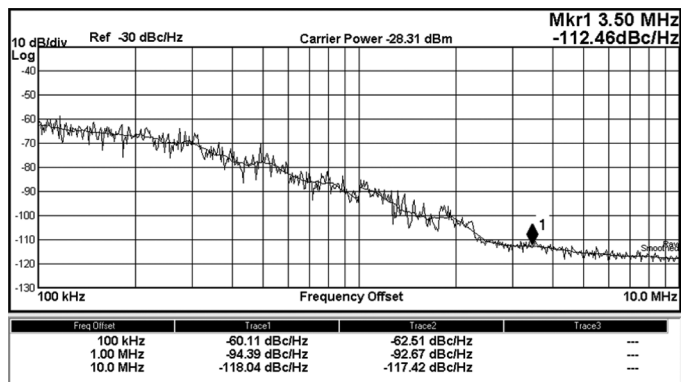

Fig. 21. Measured VCO phase noise at 2.4 GHz.

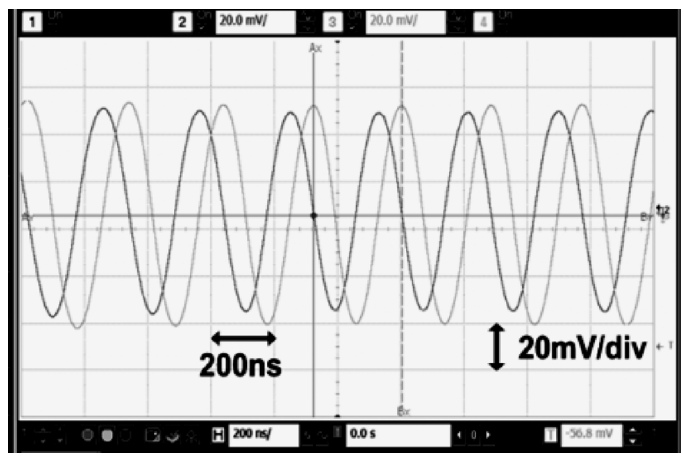

Fig. 22. Measured I/Q BB transient outputs.

are also given. The measured voltage gain is 32.8–28.2 dB and the DSB NF is between 8.6–9 dB for an IF spanning from 1 to 3 MHz, as shown in Fig. 17. We also measured the gain and NF from 2.2 to 2.6 GHz (Fig. 18).

For a narrowband receiver, the linearity is mainly justified by the out-channel linearity tests. According to the case given in [17] and [20], two tones are applied at [$f_{\rm LO}$ + 10 MHz, $f_{\rm LO}$ + 22 MHz] with a power level sweeping from -24 to -32 dBm. Due to the RF and BB filtering associated with the bidirectional property of passive mixers, the out-band IIP3 (Fig. 19) achieves -7 dBm and the $P_{1\ \rm dB}$ is -26 dBm.

For the VCO, it measures 21% tuning range from 2.623 to 2.113 GHz, as shown in Fig. 20. At 3.5-MHz offset, the phase noise (Fig. 21) is -112.46 dBc/Hz, fulfilling the specification

TABLE II
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART

Parameters	JSSC'08 [21]	JSSC'10 [22]	JSSC'10 [17]	TCAS-I'10 [24]	TMTT'11 [23]	TMTT'11 [26]	TMTT'06 [27]	ISSCC'13 [5]	ISSCC'13 [25]	This Work
Gain (dB)	35	67	75	24.5	51	22.5	30	83	55	**32**
DSB NF (dB)	7.5	16	9	16.5 (SSB)	3.2	7 (SSB)	7.3 (SSB)	6.1	9	**8.8**
Out-Band IIP3 (dBm)	-10	-10.5	-12.5	-19 (in-band data)	-32 (in-band data)	-21.5 (in-band data)	-8	-21.5	-6	**-7**
SFDR (dB)	58.3	52.3	55.5	38.3	36.5	51	59.8	51.6	60	**59.4**
VCO Phase Noise (dBc/√Hz)	N/A	-127 @ 3 MHz	-116 @3.5 MHz	N/A	N/A	N/A	N/A	-112 @ 1 MHz	-115 @ 3.5 MHz	**-111.4 @ 3.5 MHz**
Power (mW)	5.4 (w/o VCO)	32.5 (w/ VCO)	3.6 (w/ VCO)	2.52 (w/o VCO)	8.1 (w/o VCO)	1.06 (w/o VCO)	1.8 (w/o VCO)	1.6 (w/ VCO)	2.7 (w/ VCO)	**1.4 [b] (w/ VCO)**
No. of Inductor or Transformer	2	3	1	3	5	3	2	4	2	**1**
Die Area (mm^2)	0.23 (w/o VCO)	2.88 (w/ VCO)	0.35 (w/ VCO)	N/A	1.27 (w/o VCO)	1.1 (w/o VCO)	2.07 [a] (w/o VCO)	2.5 [a] (w/ VCO)	0.26 [a] (w/ VCO)	**0.14 (w/ VCO)**
Supply (V)	1.35	0.6	1.2	1.8	1.8	1.2	1.8	0.3	0.6/1.2	**0.6/1.2**
CMOS Tech.	90 nm	90 nm	90 nm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	65 nm	65 nm	**65 nm**

a: Include more BB gain stages and filters b: The power breakdown is LNTA: 0.4 mW, TIA: 0.18 mW and VCO + Buffer: 0.82 mW

(-102 dBc/Hz [17], [20]) with an adequate margin. From frequency 100 kHz to 1 MHz, the result fits the $1/f^3$ slope, and from 1 to 10 MHz, it starts to be saturated, primarily limited by the small output amplitude (-28.31 dBm) of the test buffer.

Based on transient measurements, the I/Q BB differential outputs (Fig. 22) has ~ 0.72-dB gain mismatch and 2° phase mismatch, corresponding to an IRR of ~ 25 dB.

The performance summary and benchmark are given in Table II. This work succeeds in achieving the highest power and area efficiencies via proposing a mixed-V_{DD} topology co-optimized with a number of circuit techniques. Only one on-chip inductor is entailed in the VCO. The achieved NF and out-band IIP3 correspond to a competitive SFDR of 59.4 dB according to [17], [19]

$$\mathrm{SFDR} = \frac{2(P_{\mathrm{IIP3}} + 174\ \mathrm{dBm} - \mathrm{NF} - 10\log B)}{3} - \mathrm{SNR}_{\min} \tag{22}$$

where $\mathrm{SNR}_{\min} = 4$ dB is the minimum signal-to-noise ratio required by the application, and $B = 2$ MHz is the channel bandwidth. As presented in Figs. 8 and 9, the SFDR can be further optimized by allowing more budgets in area (bigger $C_M + 2C_1$) and/or power (smaller on-resistance of the mixer switches), being a design-friendly architecture easily adaptable to different specifications.

VI. CONCLUSIONS

A mixed-V_{DD} 2.4-GHz ZigBee/WPAN receiver measured state-of-the-art performances has been described. It features passive pre-gain, a split-LNTA, a high-input-impedance BB TIA, and a low-power 50% LO generation scheme. They together lead to improved power and area efficiencies, as well as a high SFDR while eliminating the need of a RF balun. These beneficial features render this work a superior receiver candidate for cost and power reduction of ZigBee/WPAN radios in nanoscale CMOS.

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