A 2.4 GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer + Hybrid Filter Topology in 65 nm CMOS

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***Abstract*—A 2.4 GHz ZigBee receiver unifying a balun-LNA-I/Q-mixer (Blixer) and a baseband (BB) hybrid filter in one cell is fabricated in 65 nm CMOS. Without any external components, wideband input matching and passive pre-gain are concurrently achieved via co-optimizing an integrated low-Q network with a balun-LNA. The latter also features active-gain boosting and partial-noise canceling to enhance the gain and noise figure (NF). Above the balun-LNA are I/Q double-balanced mixers driven by a 4-phase 25% LO for downconversion and gain-phase balancing. The generated BB currents are immediately filtered by an IF-noise-shaping current-mode Biquad and a complex-pole load, offering first-order image rejection and third-order channel selection directly atop the Blixer. Together with other BB and LO circuitries, the receiver measures 8.5 dB NF, 57 dB gain and -6-dBm $\mathrm{IIP3_{out\text{-}band}}$ at 1.7 mW power and 0.24 mm² die size. The $\mathrm{S_{11}}$-bandwidth (<-10 dB) covers 2.25 to 3.55 GHz being robust to packaging variations. Most performance metrics compare favorably with the state-of-the-art.**

***Index Terms*—Balun low-noise amplifier (Balun-LNA), CMOS, current reuse, hybrid filter, local oscillator (LO), mixer, noise figure (NF), noise-canceling, noise-shaping, output balancing, polyphase filter (PPF), RC-CR network, receiver, voltage-controlled oscillator (VCO), wireless, ZigBee.**

I. Introduction

ULTRA-LOW-POWER (ULP) radios have essentially underpinned the development of short-range wireless technologies [1] such as personal/body-area networks and Internet of Things. The main challenges faced by those ULP radios are the stringent power and area budgets, and the pressure of minimum external components to save cost and system volume. Balancing them with the performance metrics such as noise figure (NF), linearity and input matching involves many design tradeoffs at both architecture and circuit levels.

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Ultra-low-voltage receivers have been extensively studied for short-range ZigBee, Bluetooth and energy-harvesting applications [2]–[5]. Yet, the lack of voltage headroom will limit the signal swing and transistor's $\mathrm{f_T}$, imposing the need of bulky inductors or transformers to facilitate the biasing and tune out the parasitics. Thus, the die area is easily penalized, such as 5.76 mm² in [4] and 2.5 mm² in [5]. In fact, the current-reuse topologies should benefit more from technology scaling when the NF is less demanding. Advanced process nodes such as 65 nm CMOS feature sufficiently high-$\mathrm{f_T}$ and low-$\mathrm{V_T}$ transistors for GHz circuits to operate at very small bias currents. Unsurprisingly, when cascoding the building blocks for current reuse, such as the low-noise amplifier (LNA) plus mixer [6], the RF bandwidth and linearity can be improved as well, by avoiding any high-impedance nodes at their interface.

Several NF-relaxed current-reuse receivers have been reported. The LNA-Mixers-VCO (LMV) cell [7] is illustrated in Fig. 1. Sharing the bias current among more blocks successfully saves the power (2.4 mW), but the NF, gain and $\mathrm{S_{11}}$ are sensitive to its external high-Q inductor ($\mathrm{L_{ext}}$) for narrowband input matching and passive pre-gain. Also, under the same bias current, it is hard to optimize the LNA's NF (RF path) with the phase noise of the VCO (LO path). Finally, although a single VCO can save area, the narrow-band I/Q generation has to be embedded into the LNA, rendering the I/Q accuracy more susceptible to process variations.

To return the I/Q generation back to the LO path, [8] adopted two VCOs to tailor a quadrature LMV (QLMV) cell. Although its power is further optimized (1 mW), three on-chip inductors and one off-chip balun are entailed, penalizing the die size and system cost. Also, both LMV and QLMV cells share the same pitfall that only a 50%-duty-cycle LO (50% LO) can be used for the mixing, which is less effective than 25% LO in terms of gain (i.e., 3 dB higher), NF and I/Q isolation [6]. Finally, as their baseband (BB) channel selection and image rejection are out of their current-reuse paths, any large out-band blockers will be converted into voltages before filtering. This fact constitutes a hard tradeoff between noise, linearity and power (i.e., 1.2 mW BB power in [7] and 5.2 mW BB power in [8]).

Another example is the current-reuse circuit-reuse receiver reported in [9]. It merges the RF LNA and BB transimpedance amplifier (TIA) in one cell [Fig. 2(a)]. A conceptual view of its operation is given in Fig. 2(b). Without the VCO, and by using

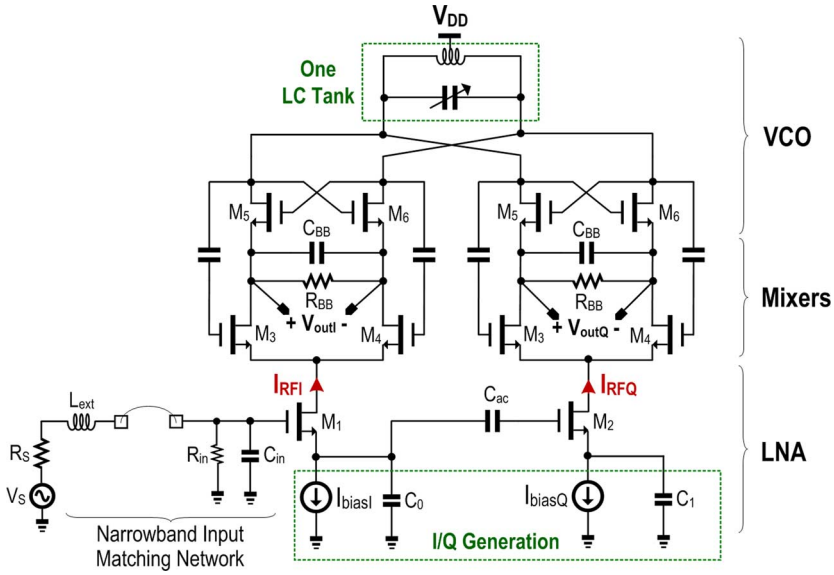


Fig. 1. LMV cell [6]. L_{ext} is external for narrowband input matching and pre-gain. One LC-tank VCO saves the chip area, but putting the I/Q generation in the LNA (M_1–M_2) degrades NF. Only single-balanced mixers (M_3–M_4) can be used.

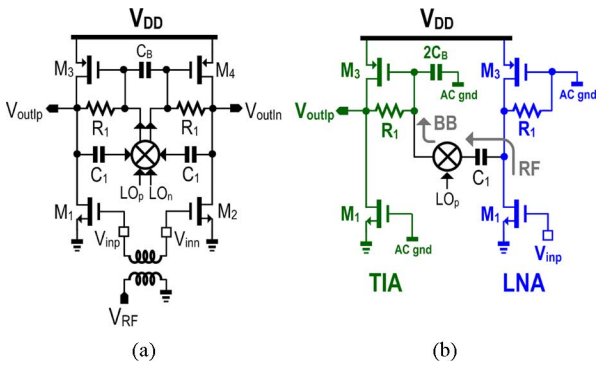


Fig. 2. (a) Circuit-reuse receiver merging RF LNA and BB TIA [9]. (b) Its single-ended equivalent circuit illustrating its RF-to-BB operation conceptually (from right to left).

passive mixers, this topology can reserve more voltage headroom for the dynamic range. A RF balun is nevertheless entailed for its fully-differential operation, and several constraints limit its NF and linearity: 1) the LNA and TIA must be biased at the same current; 2) the LNA's NF should benefit more from short-channel devices for M_{1-2}, but the BB TIA prefers long-channel ones to lower the $1/f$ noise; and 3) any out-band blockers will be amplified at the LNA's (TIA's) output before deep BB filtering.

This paper describes the details of an extensive-current-reuse ZigBee receiver [10] with most RF-to-BB functions merged in one cell, while avoiding any external components for input-impedance matching. Together with a number of ULP circuits and optimization techniques, the receiver fabricated in 65 nm CMOS measures high performances in terms of IIP3, S_{11}- bandwidth, power and area efficiencies with respect to the prior art.

Section II overviews the receiver architecture. Section III details the implementation of key building blocks. Measurement results and performance benchmarks are summarized in Section IV, and conclusions are given in Section V.

II. Proposed Current-Reuse Receiver Architecture

The block diagram is depicted in Fig. 3. As discussed above and detailed in [8] for the QLMV cell, merging the LO path with the signal path is not that desirable, as they will add noise to each other and induce signal loss. In fact, stacking of building blocks should be in conformity with the signal flow from RF to BB, such that all bias currents serve only the signal currents. In this work, the LO path is separated, which also facilitates the use of a 25% LO for better overall performance than in its 50% counterpart. The single-ended RF input (V_{RF}) is taken by a low-Q input-matching network before reaching the Balun-LNA-I/Q-Mixer (Blixer). Merging the latter with the hybrid filter not only saves power, but also reduces the voltage swing at internal nodes benefitting the linearity. The wideband input-matching network is also responsible for the pre-gain to enhance the NF. Unlike the LMV cell that only can utilize single-balanced mixers [7], here the balun-LNA featuring a differential output ($\pm i_{LNA}$) allows the use of double-balanced mixers (DBMs). Driven by a 4-phase 25% LO, the I/Q-DBMs with a large output resistance robustly correct the differential imbalances of $\pm i_{LNA}$. The balanced BB currents ($\pm i_{MIX,I}$ and $\pm i_{MIX,Q}$) are then filtered directly in the current domain by a current-mode Biquad stacked atop the DBM. The Biquad features in-band noise-shaping centered at the desired intermediate frequency (IF, 2 MHz). Only the filtered output currents ($\pm i_{rLPF,I}$ and $\pm i_{rLPF,Q}$) are returned as voltages ($\pm V_{o,I}$ and $\pm V_{o,Q}$) through the complex-pole load, which performs both image rejection and channel selection. Out of the current-reuse path there is a high-swing variable-gain amplifier (VGA). It essentially deals with the gain loss of its succeeding three-stage RC-CR polyphase filter (PPF), which is responsible for large and robust image rejection over mismatches and process variations. The final stage is an inverter amplifier before 50 Ω test buffering. The 4-phase 25% LO can be generated by an external 4.8 GHz reference (LO_{ext}) after a divide-by-2 (DIV1) that features 50%-input 25%-output, or from an integrated 10 GHz VCO after DIV1 and DIV2 (25%-input 25%-output) for additional testability.

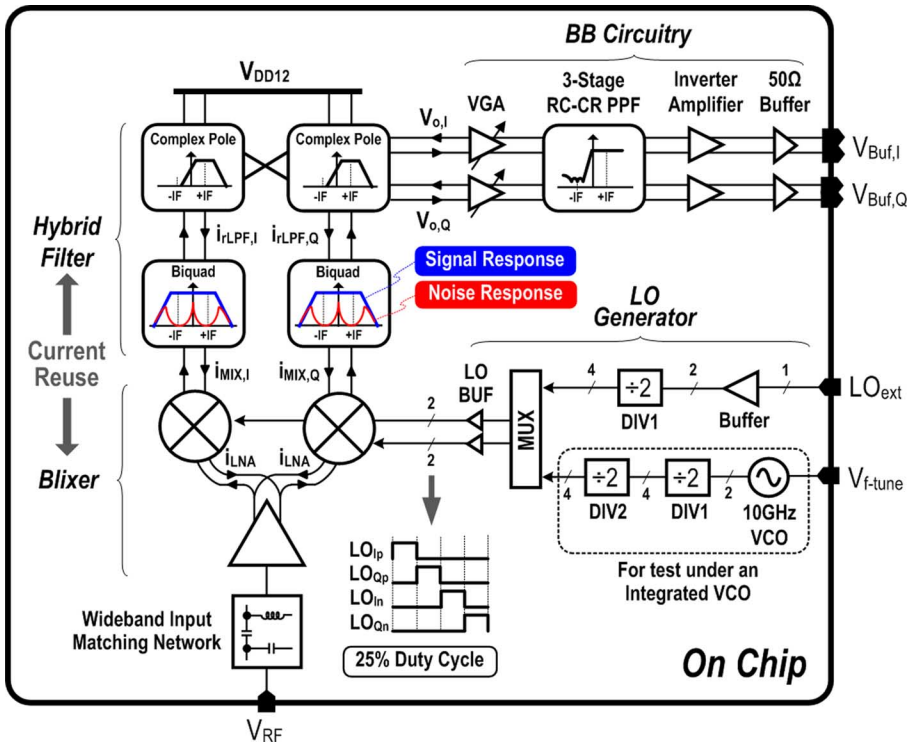


Fig. 3. Proposed RF-to-BB-current-reuse ZigBee receiver.

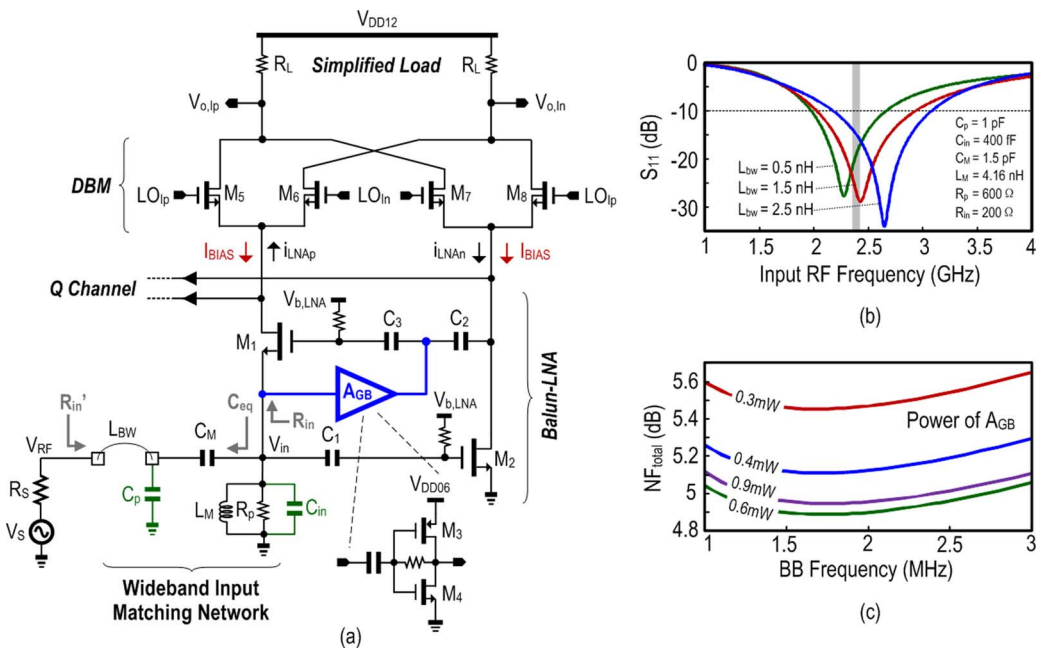


Fig. 4. (a) Proposed wideband input matching network, balun-LNA and I/Q-DBMs (Q channel is omitted and the load is simplified as $\mathrm{R_L}$). (b) Variation of $\mathrm{S_{11}}$-bandwidth with bondwire inductance $\mathrm{L_{BW}}$. (c) Power of $\mathrm{A_{GB}}$ versus NF.

III. Circuit Implementation

A. Wideband Input-Matching Network

Its schematic is illustrated in Fig. 4(a). A low-Q inductor ($\mathrm{L_M}$) and two tapped capacitors ($\mathrm{C_p}$ and $\mathrm{C_M}$) are employed for impedance down-conversion resonant and passive pre-gain. A high-Q inductor is unnecessary since the Q of the LC matching is dominated by the low input resistance of the LNA. Thus, a low-Q inductor results in area savings, while averting the need of an external inductor for cost savings. $\mathrm{L_M}$ also serves as the bias inductor for $\mathrm{M_1}$. $\mathrm{R_p}$ is the parallel shunt resistance of $\mathrm{L_M}$. $\mathrm{C_p}$ stands for the parasitic capacitance from the pad and ESD diodes. $\mathrm{R_{in}}$ and $\mathrm{C_{in}}$ are the equivalent resistance and capacitance at node $\mathrm{V_{in}}$, respectively. $\mathrm{R'_{in}}$ is the downconversion resistance of $\mathrm{R_{in}}$. $\mathrm{L_{BW}}$ is the bondwire inductance and $\mathrm{R_s}$ is the source resistance. To simplify the analysis, we first omit $\mathrm{L_{BW}}$ and $\mathrm{C_{in}}$, so that $\mathrm{L_M}$, $\mathrm{C_p}$, $\mathrm{C_M}$, $\mathrm{R_S}$ and $\mathrm{R_T}$ $(= \mathrm{R_p}//\mathrm{R_{in}})$ together

form a tapped capacitor facilitating the input matching. Generally, $S_{11} \leq -10$ dB is required and the desired value of R'_{in} is from 26 to 97 Ω over the frequency band of interest. Thus, given the R_T and C_M values, the tolerable C_p can be derived from $R'_{in} = R_T(C_M/(C_M + C_p))^2$. The pre-gain value ($A_{pre,amp}$) from V_{RF} to V_{in} is derived from $V_{in}^2/2R_T = V_{RF}^2/2R_S$, which can be simplified as $A_{pre,amp} = \sqrt{R_T/R_S}$. The -3 dB bandwidth of $A_{pre,amp}$ is related to the network's quality factor (Q_n) as given by: $Q_n = R_T/2\omega_0 L_M = \omega_0/\omega_{-3dB}$, with $\omega_0 = 1/\sqrt{L_M C_{EQ}}$ and $C_{EQ} = C_M C_p/(C_M + C_p)$.

In our design ($R_T = 150\ \Omega$, $C_M = 1.5$ pF, $L_M = 4.16$ nH, $R_p = 600\,\Omega$, $C_p = 1$ pF, and $R_{in} = 200\,\Omega$), $A_{pre,amp}$ has a passband gain of ~4.7 dB over a 2.4 GHz bandwidth (at RF = 2.4 GHz) under a low Q_n of 1. Thus, the tolerable C_p is sufficiently wide (0.37 to 2.1 pF). The low-Q L_M is extremely compact (0.048 mm^2) in the layout and induces a small parasitic capacitance (~ 260 fF, part of C_{in}). Fig. 4(b) demonstrates the robustness of S_{11}-bandwidth against L_{BW} from 0.5 to 2.5 nH. The variation of C_{in} to S_{11}-bandwidth was also studied. From simulations, the tolerable C_{in} is 300 to 500 fF at $L_{BW} = 1.5$ nH. The correlation between S_{11}-bandwidth and Q_n is derived in Appendix A.

B. Balun-LNA With Active Gain Boost and Partial Noise Canceling

The common-gate (CG) common-source (CS) balun-LNA [11] avoids the off-chip balun and achieves a low NF by noise canceling, but the asymmetric CG-CS transconductances and loads make the output balancing not wideband consistent. Both [6] and [12] have addressed this issue. In [6], output balancing is achieved by scaling M_{5-8} with cross-connection at BB, but that is incompatible with this work that includes a hybrid filter. In [12], by introducing an AC-coupled CS branch and a differential current balancer (DCB), the same load is allowed for both CS and CG branches for wideband output balancing. Thus, the NF of such a balun-LNA can be optimized independently. This technique is transferred to this ULP design, but only with the I/Q-DBMs inherently serve as the DCB, avoiding a high voltage supply [12]. The detailed schematic is depicted in Fig. 4(a). To maximize the voltage headroom, M_1 (with $g_{m,CG}$) and M_2 (with $g_{m,CS}$) were sized with non-minimum channel length ($L = 0.18\ \mu$m) to lower their V_T. The AC-coupled gain stage is a self-biased inverter amplifier (A_{GB}) powered at 0.6-V (V_{DD06}) to enhance its transconductance ($g_{m,AGB}$)-to-current ratio. It gain-boosts the CS branch while creating a loop gain around M_1 to enhance its effective transconductance under less bias current (I_{BIAS}). This scheme also allows the same I_{BIAS} for both M_1 and M_2, requiring no scaling of load (i.e., only R_L). Furthermore, a small I_{BIAS} lowers the supply requirement, making a 1.2 V supply (V_{DD12}) still adequate for the Blixer and hybrid filter, while relaxing the required LO swing (LO_{IP} and LO_{In}). C_{1-3} for biasing are typical metal-oxide-metal (MoM) capacitors to minimize the parasitics.

The balun-LNA features partial-noise canceling. To simplify the study, we ignore the noise induced by DBM (M_5–M_8) and the effect of channel-length modulation. The noise transfer function (TF) of M_1's noise ($I_{n,CG}$) to the BB differential output ($V_{o,Ip}$–$V_{o,In}$) can be derived when LO_{Ip} is high, and the input impedance is matched:

$$TF_{I_{n,CG}} = -\frac{1}{2}\left(R_L - R_{in}G_{m,CS}R_L\right) \tag{1}$$

where $G_{m,CS} = g_{m,CS} + g_{m,AGB}$. The noise of M_1 can be fully canceled if $R_{in}G_{m,CS} = 1$ is satisfied. However, as analyzed in Section III-A, $R_{in} \approx 200\ \Omega$ is desired for input matching at low power. Thus, $G_{m,CS}$ should be $\approx$ 5 mS, rendering the noises of $G_{m,CS}$ and R_L still significant. Thus, device sizings for *full* noise cancellation of M_1 should not lead to the lowest total NF (NF_{total}). In fact, one can get a more optimized $G_{m,CS}$ (via $g_{m,AGB}$) for stronger reduction of noise from $G_{m,CS}$ and R_L, instead of that from M_1. Although this noise-canceling principle has been discussed in [13] for its single-ended LNA, the output balancing was not a concern there. In this work, the optimization process is alleviated since the output balancing and NF are decoupled. The simulated NF_{total} up to the $V_{o,Ip}$ and $V_{o,In}$ nodes against the power given to the A_{GB} is given in Fig. 4(c). NF_{total} is reduced from 5.5 dB at 0.3 mW to 4.9 dB at 0.6 mW, but is back to 5 dB at 0.9 mW. Due to the use of passive pre-gain and a larger R_p that is ~3 times R_{in}, the noise contribution of the inductor is <1% from simulations. The simulated NF at the outputs of the LNA and test buffer are 5.3 and 6.6 dB, respectively. The relationship of $G_{m,CS}$ and NF_{total} is derived in Appendix B, which is also applicable to the balun-LNA in [12].

C. Double-Balanced Mixers Offering Output Balancing

As analyzed in [12] the active-gain-boosted balun-LNA can only generate unbalanced outputs. Here, the output balancing is inherently done by the I/Q-DBMs under a 4-phase 25% LO. For simplicity, this principle is described for the I channel only under a 2-phase 50% LO, as shown in Fig. 5, where the load is simplified as R_L. During the first-half LO cycle when LO_{Ip} is high, i_{LNAp} goes up and appears at $V_{o,Ip}$ while i_{LNAn} goes down and appears at $V_{o,In}$. In the second-half LO cycle, both of the currents' sign and current paths of i_{LNAp} and i_{LNAn} are flipped. Thus, when they are summed at the output during the whole LO cycle, the output balancing is robust, thanks to the large output resistance (9 kΩ) of M_5–M_8 enabled by the very small I_{BIAS} (85 μA). To analytically prove the principle, we let $i_{LNAp} = \alpha I_A \cos(\omega_s t + \varphi_1)$ and $i_{LNAn} = -I_A \cos(\omega_s t + \varphi_2)$, where I_A is the amplitude, ω_s is the input signal frequency, α is the unbalanced gain factor and φ_1 and φ_2 are their arbitrary initial phases. When there is sufficient filtering to remove the high-order terms, we can deduce the BB currents $i_{MIX,Ip}$ and $i_{MIX,In}$ as given by

$$\begin{aligned} i_{MIX,Ip} &= \frac{2}{\pi}\alpha I_A \cos(\omega_s t + \varphi_1) \times \cos\omega_0 t \\ &\quad + \frac{2}{\pi} I_A \cos(\omega_s t + \varphi_2) \times \cos\omega_0 t \\ &= \frac{\alpha I_A}{\pi}\cos(\omega_s t - \omega_0 t + \varphi_1) \\ &\quad + \frac{I_A}{\pi}\cos(\omega_0 t - \omega_s t + \varphi_2) \end{aligned} \tag{2}$$

$$\begin{aligned} i_{MIX,In} &= -\frac{I_A}{\pi}\cos(\omega_s t - \omega_0 t + \varphi_2) \\ &\quad - \frac{\alpha I_A}{\pi}\cos(\omega_0 t - \omega_s t + \varphi_1) \\ &= -i_{MIX,Ip} \end{aligned} \tag{3}$$

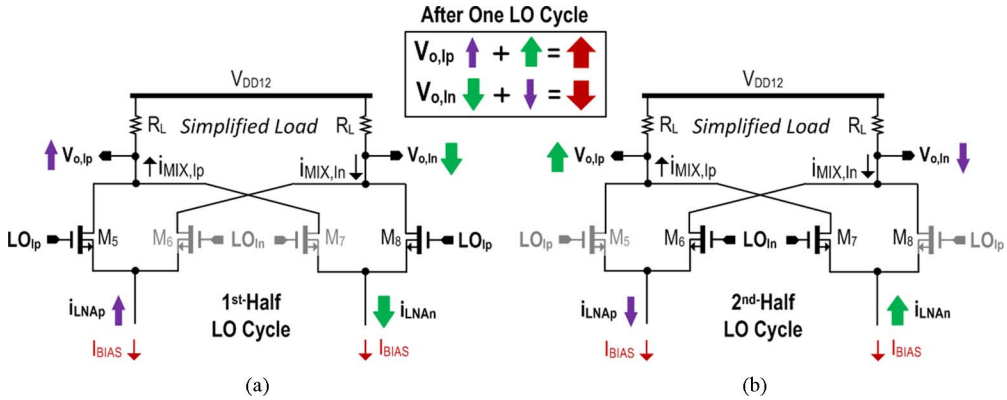


Fig. 5. Operation of the I-channel DBM. It inherently offers output balancing after averaging in one LO cycle as shown in their (a) first-half LO cycle and (b) second-half LO cycle.

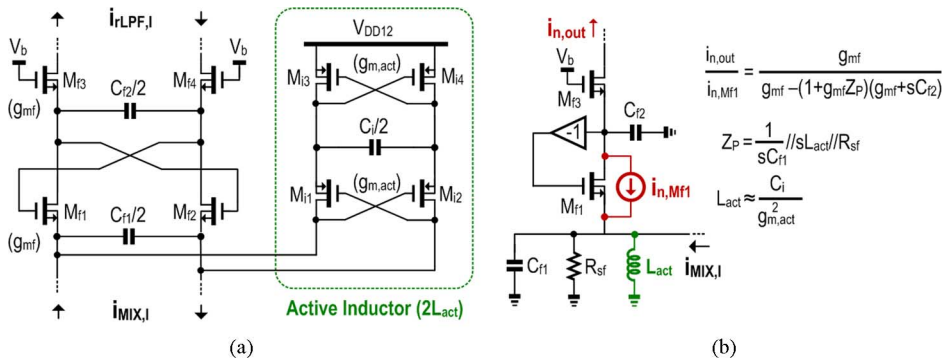


Fig. 6. (a) Proposed IF-noise-shaping Biquad and (b) its small-signal equivalent circuit showing the noise TF of $\mathrm{M_{f1}}$.

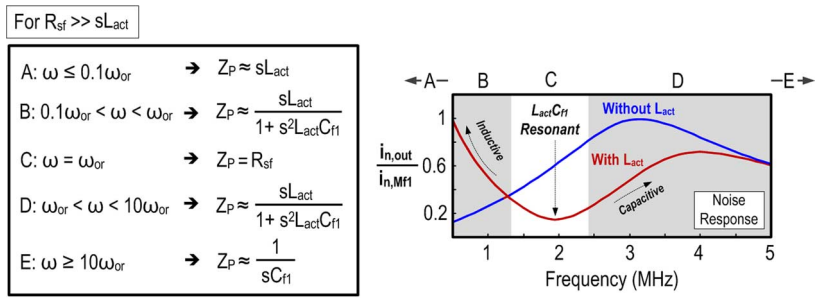
and a consistent proof for I/Q-DBMs under a 4-phase 25% LO is obtained. Ideally, from (2)–(3), the DBM can correct perfectly the gain and phase errors from the balun-LNA, independent of its different output impedances from the CG and CS branches. In fact, even if the conversion gain of the two mixer pairs ($\mathrm{M_5}$, $\mathrm{M_8}$ and $\mathrm{M_6}$, $\mathrm{M_7}$) does not match (e.g., due to non-50% LO duty cycle), the double-balanced operation can still generate balanced outputs (confirmed by simulations). Of course, the output impedance of the DBM can be affected by that of the balun-LNA [Fig. 4(a)], but is highly desensitized due to the small size of $\mathrm{R_L}$ (i.e., the input impedance of the hybrid filter) originally aimed for current-mode operation. Thus, the intrinsic imbalance between $\mathrm{V_{o,Ip}}$ and $\mathrm{V_{o,In}}$ is negligibly small (confirmed by simulations).

For devices sizing, a longer channel length ($\mathrm{L} = 0.18\ \mu\mathrm{m}$) is preferred for $\mathrm{M_{5-8}}$ to reduce their $1/\mathrm{f}$ noise and $\mathrm{V_T}$. Hard-switch mixing helps to desensitize the I/Q-DBMs to LO gain error, leaving the image rejection ratio (IRR) mainly determined by the LO phase error that is a tradeoff with the LO-path power. Here, the targeted LO phase error is relaxed to $\sim 4^\circ$, as letting the BB circuitry (i.e., the complex-pole load and three-stage RC-CR PPF) to handle the IRR is more power efficient, as detailed in Sections III-E and III-F.

D. Hybrid Filter First Half – Current-Mode Biquad With IF Noise-Shaping

The current-mode Biquad [Fig. 6(a)] proposed in [14] is an excellent candidate for current-reuse with the Blixer for channel selection. However, this Biquad can only generate a noise-shaping zero spanning from DC to $\sim 2\pi 0.1\mathrm{Q_B}\omega_{0\mathrm{B}}$ MHz for $\mathrm{M_{f1}}$–$\mathrm{M_{f2}}$, where $\mathrm{Q_B}$ and $\omega_{0\mathrm{B}}$ are the Biquad's quality factor and -3 dB cutoff frequency, respectively. This noise shaping is hence ineffective for our low-IF design having a passband from ω_1 to ω_2 ($= \omega_{0\mathrm{B}}$), where $\omega_1 > 0.1\mathrm{Q_B}\omega_{0\mathrm{B}}$. To address this issue, an active inductor ($\mathrm{L_{act}}$) is added at the sources of $\mathrm{M_{f1}}$–$\mathrm{M_{f2}}$. The $\mathrm{L_{act}C_{f1}}$ resonator shifts the noise-shaping zero to the desired IF. The cross-diode connection between $\mathrm{M_{i1}}$–$\mathrm{M_{i4}}$ (all with $\mathrm{g_{m,act}}$) emulate $\mathrm{L_{act}} \approx \mathrm{C_i/g_{m,act}^2}$ [15], [16]. The small-signal equivalent circuit to calculate the noise TF of $\mathrm{i_{n,Mf1}/i_{n,out}}$ is shown in Fig. 6(b). The approximated impedance of $\mathrm{Z_P}$ in different frequencies related to $\omega_{0\mathrm{r}}$ is summarized in Fig. 7(a), where $\omega_{0\mathrm{r}} = (\omega_1 + \omega_2)/2$ is the resonant frequency of $\mathrm{L_{act}C_{f1}}$ at IF. The simulated $\mathrm{i_{n,Mf1}/i_{n,out}}$ is shown in Fig. 7(b). At the low frequency range, $\mathrm{Z_P}$ behaves inductively, degenerating further $\mathrm{i_{n,Mf1}}$ when the frequency is increased. At the resonant frequency, $\mathrm{Z_P} = \mathrm{R_{sf}}$, where $\mathrm{R_{sf}}$ is the parallel impedance of the active inductor's shunt resistance and DBM's output resistance. The latter is much higher when compared with $\mathrm{R_L}$ thereby suppressing $\mathrm{i_{n,Mf1}}$. At the high frequency range, $\mathrm{Z_P}$ is more capacitive dominated by $\mathrm{C_{f1}}$. It implies $\mathrm{i_{n,Mf1}}$ can be leaked to the output via $\mathrm{C_{f1}}$, penalizing the in-band noise. At even higher frequencies, the output noise decreases due to $\mathrm{C_{f2}}$, being the same as its original form [14].

The signal TF can be derived from Fig. 8. Here $\mathrm{R_L} = 1/\mathrm{g_{mf}}$, $\mathrm{L_{biq}} = \mathrm{C_{f2}/g_{mf}^2}$. For an effective improvement of NF, $\mathrm{L_{act}} \gg \mathrm{L_{biq}}$ should be made. The simulated $\mathrm{NF_{total}}$ at $\mathrm{V_{o,Ip}}$ and $\mathrm{V_{o,In}}$



(a) (b)

Fig. 7. (a) Equivalent impedance of Z_P versus ω_{or}, and (b) simulated noise TF of $i_{n,out}/i_{n,Mf1}$ with and without L_{act}.

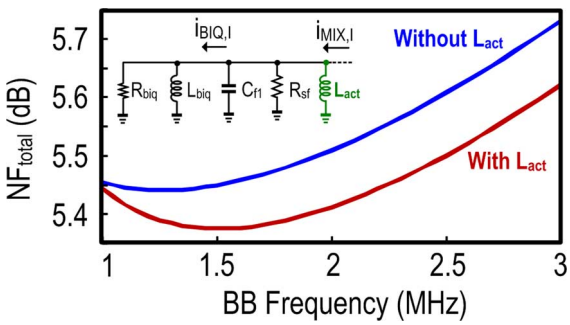


Fig. 8. Simulated NF_{Total} (at $V_{o,Ip}$ and $V_{o,In}$) with and without L_{act}.

with and without the L_{act} is shown Fig. 8, showing about 0.1 dB improvement at the TT corner (reasonable contribution for a BB circuit). For the SS and FF corners, the NF improvement reduces to 0.04 and 0.05 dB, respectively. These results are expected due to the fact that at the FF corner, the noise contribution of the BB is less significant due to a larger bias current; while at the SS corner, the IF noise-shaping circuit will add more noise by itself, offsetting the NF improvement. Here M_{f1}–M_{f4} use isolated P-well for bulk-source connection, avoiding the body effect while lowering their V_T.

E. Hybrid Filter Second Half – Complex-Pole Load

Unlike most active mixers or the original Blixer [6] that only use a RC load, the proposed "load" synthesizes a first-order complex pole at the positive IF (+IF) for channel selection and image rejection. The circuit implementation and principle are shown in Fig. 9(a) and (b), respectively. The real part (R_L) is obtained from the diode-connected M_L, whereas the imaginary part ($g_{m,Mc}$) is from the I/Q-cross-connected M_C. The entire hybrid filter [i.e., Fig. 7(a) + Fig. 9(b)] offers 5.2 dB IRR, and 12 dB (29 dB) adjacent (alternate) channel rejection as shown in Fig. 10 (the channel spacing is 5 MHz). Similar to g_m-C filters the center frequency is defined by $g_{m,Mc}R_L$. When sizing the -3 dB bandwidth, the output conductances of M_C and M_L should be taken into account.

F. Current-Mirror VGA and RC-CR PPF

Outside the current-reuse path, $V_{o,I}$ and $V_{o,Q}$ are AC-coupled to a high-swing current-mirror VGA formed with M_L [Fig. 9(a)] and a segmented M_{VGA} (Fig. 11), offering gain controls with a 6 dB step size. To enhance the gain precision,

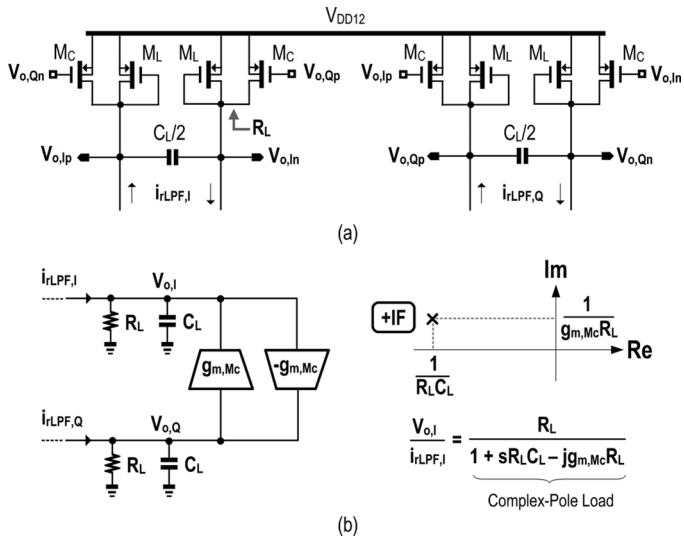


Fig. 9. (a) Proposed complex-pole load and (b) its small-signal equivalent circuit and pole plot.

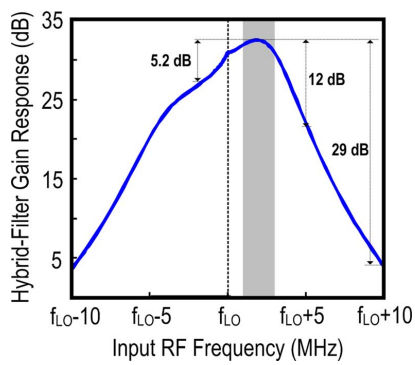


Fig. 10. Simulated hybrid-filter gain response.

the bias current through M_{VGA} is kept constant, so as its output impedance. With the gain switching of M_{VGA}, the input-referred noise of M_{VGA} will vary. However, when the RF signal level is low the gain of the VGA should be high, rendering the gain switching not influencing the receiver's sensitivity. The VGA is responsible for compensating the gain loss (30 dB) of the three-stage passive RC-CR PPF that provides robust image rejection of >50 dB (corner simulations). With the hybrid filter rejecting the out-band blockers the linearity of the VGA is further relaxed, so as its power budget (192 μW, limited by the noise and gain requirements).

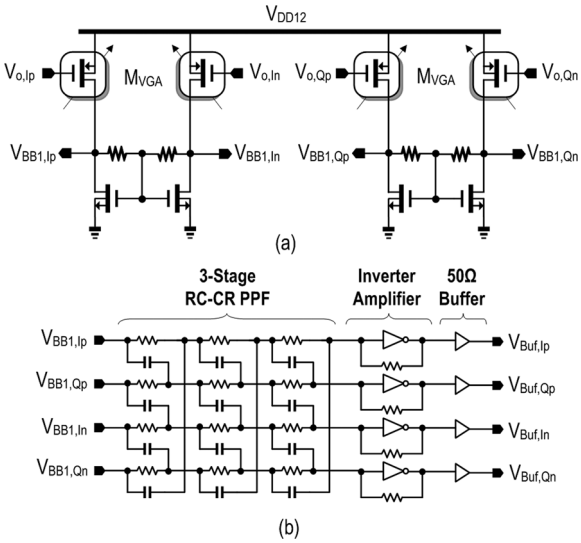


Fig. 11. Schematics of the BB (a) VGA, and (b) three-stage RC-CR PPF, inverter amplifier and 50-Ω buffer.

A three-stage RC-CR PPF can robustly meet the required IRR in the image band (i.e., the $-$IF), and cover the ratio of maximum to minimum signal frequencies [17], [18]. In our design, the expected IRR is 30 to 40 dB and the ratio of frequency of the image band is f_{max}/f_{min} $(=3)$. However, counting the RC variations as large as $\pm 25\%$, the conservative $\Delta f_{eff} = f_{max\_eff}/f_{min\_eff}$ should be close to 5. The selected RC values are guided by [18]

$$\frac{\sigma\,(\text{Image Out})}{\text{Desired Out}} = 0.25\sqrt{\left(\frac{\sigma_R}{R}\right)^2 + \left(\frac{\sigma_C}{C}\right)^2}. \qquad (4)$$

Accordingly, the matching of the resistors (σ_R) and capacitors (σ_C) can be relaxed to 0.9% (2.93%) for 40 dB (30 dB) IRR with a 3σ yield. Here, $\sim$150 kΩ resistors are chosen to ease the layout with a single capacitor size (470 fF), balancing the noise, area, and IRR. The simulated worst IRR is 36 dB without LO mismatch, and still over 27 dB at a 4° LO phase error checked by 100× Monte-Carlo simulations. Furthermore, if the 5 dB IRR offered by the complex-pole load is added, the minimum IRR of the IF chain should be 32 dB. The final stage before 50 Ω output buffering is a self-biased inverter amplifier (power $= 144\ \mu$W), which embeds one more real pole for filtering. The simulated overall IF gain response is shown in Fig. 12, where the notches at DC offered by the AC-coupling network, and around the –IF offered by the three-stage RC-CR PPF, are visible. The IRR is about 57 dB [$=$ 52 dB (RC-CR PPF) + 5 dB (complex-pole load)] under an ideal 4-phase 25% LO for the image band from $[f_{LO}-3, f_{LO}-1]$ MHz.

G. VCO and Dividers and LO Buffers

To fully benefit the speed and low-V_T advantages of fine linewidth CMOS, the entire LO path is powered at a lower supply of 0.6 V to reduce the dynamic power. For additional testability, an on-chip VCO is integrated. It is optimized at $\sim$10 GHz to save area and allows division by 4 for I/Q generation. The loss of its LC tank is compensated by complementary NMOS-PMOS negative transconductors.

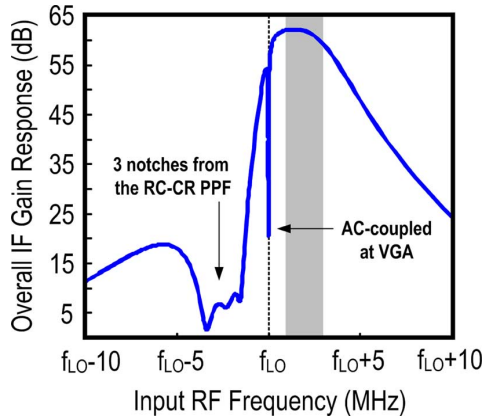


Fig. 12. Simulated overall IF gain response.

The divider chain [Fig. 13(a)] cascades two types of div-by-2 circuits (DIV1 and DIV2) to generate the desired 4-phase 25% LO, from a 2-phase 50% output of the VCO. The two latches (D1 and D2) are employed to build DIV1 that can directly generate a 25% output from a 50% input [20], resulting in power savings due to less internal logic operation (i.e., AND gates [19]) and load capacitances. Each latch consists of two sense devices, a regenerative loop and two pull up devices. For 25%-input 25%-output division, DIV2 is proposed that it can be directly interfaced with DIV1. The 25% output of DIV1 are combined by M_{D1} to M_{D4} to generate a 50% clock signal for D3 and D4.

For testing under an external LO_{ext} source at 4.8 GHz, another set of D1 and D2 is adopted. The output of these two sets of clocks are combined by transmission gates and then selected. Although their transistor sizes can be reduced aggressively to save power, their drivability and robustness in process corners can be degraded. From simulations, the sizing can be properly optimized. The four buffers (Buf_{1-4}) serve to reshape the pulses from DIV2 and enhance the drivability. The timing diagram is shown in Fig. 13(b). Due to the very small I_{BIAS} for the I/Q-DBMs, a LO amplitude of around 0.4 V_{pp} is found to be more optimized in terms of NF and gain as simulated and shown in Fig. 14(a). To gain benefits from it C_{LO} is added to realize a capacitor divider with $C_{MIX,in}$ (input capacitance of the mixer) as shown in Fig. 14(b). This act brings down the equivalent load ($C_{L,eq}$) of Buf_{1-4} by $\sim$33%.

IV. Experimental Results

The ZigBee receiver was fabricated in 65 nm CMOS (Fig. 15) and optimized with dual supplies (1.2 V: Blixer + hybrid filter, 0.6 V: LO and BB circuitries). The die area is 0.24 mm^2 (0.3 mm^2) without (with) counting the LC-tank VCO. Since there is no frequency synthesizer integrated, the results in Fig. 16(a)–(d) were measured under LO_{ext} for accuracy and data repeatability. The S_{11}-BW (<-10 dB) is $\sim$1.3 GHz for both chip-on-board (CoB) and CQFP-packaged tests [Fig. 16(a)], which proves its immunity to board parasitics and packaging variations. The gain (55 to 57 dB) and NF (8.3 to 11.3 dB) are also wideband consistent [Fig. 16(b)]. The gain peak at around 2.4 to 2.5 GHz is from the passive pre-gain. Following the linearity test profile of [7], two tones

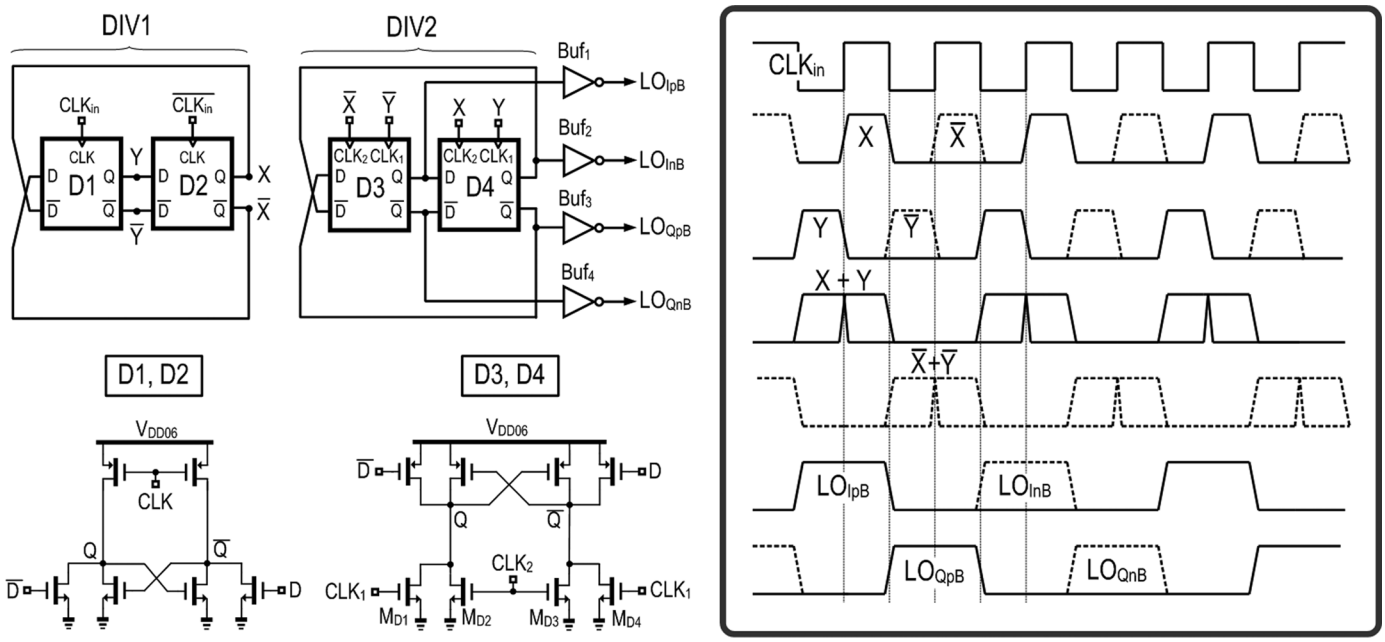


Fig. 13. (a) Schematics of DIV1 and DIV2, and (b) their timing diagrams.

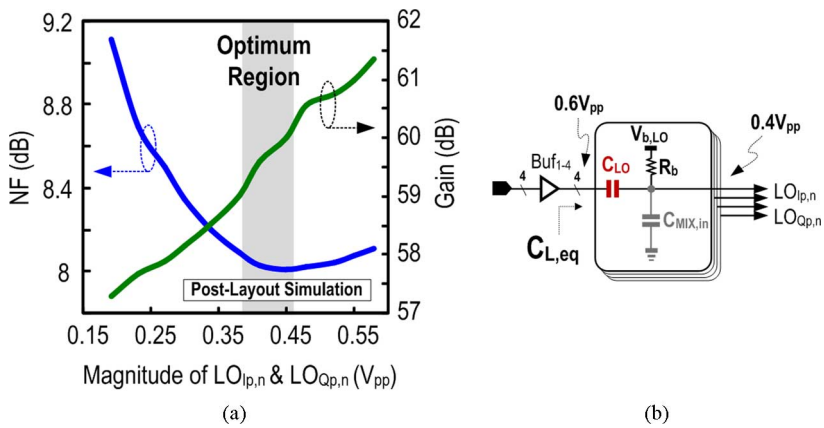


Fig. 14. (a) Post-layout simulation of NF and gain versus LO's amplitude, and (b) additional C_{LO} generates the optimum LO's amplitude.

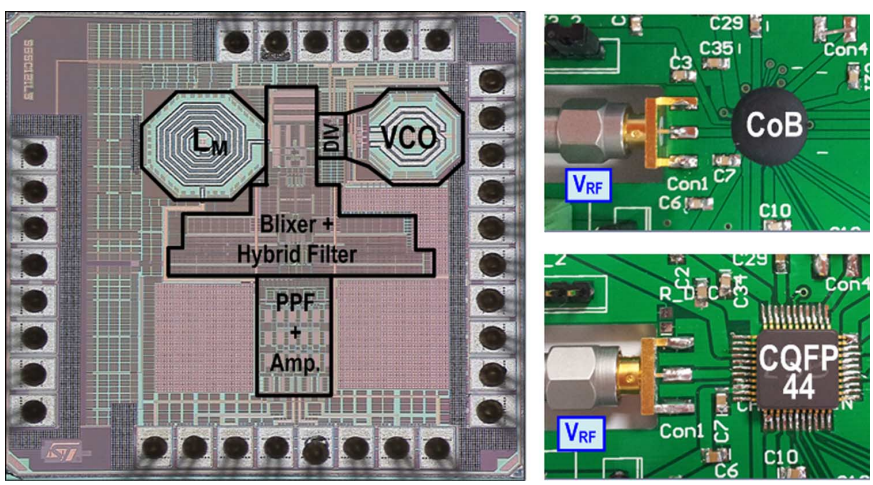


Fig. 15. Chip micrograph of the receiver. It was tested under CoB and CQFP44 packaging. No external component is entailed for input matching.

at $[\mathrm{LO} + 12\ \mathrm{MHz}, \mathrm{LO} + 22\ \mathrm{MHz}]$ are applied, measuring an $\mathrm{IIP3}_{\text{out-band}}$ of -6 dBm [Fig. 16(c)] at the maximum gain of 57 dB (there is 24 dB gain loss in Fig. 16(c) associated with the test buffer and used 1:8 transformer). This high IIP3 is due to the direct current-mode filtering at the mixer's output before signal amplification. The asymmetric IF response [Fig. 16(d)] shows

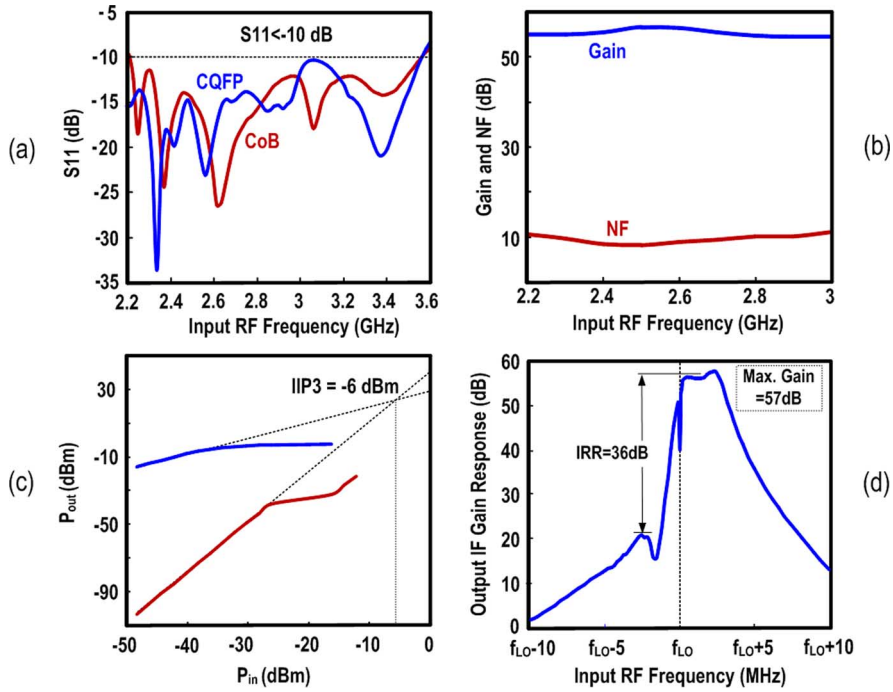


Fig. 16. Measured (a) S_{11}, (b) wideband gain and NF, (c) $\mathrm{IIP3_{out\text{-}band}}$, and (d) low-IF filtering profile.

TABLE I
KEY PERFORMANCES OF THE RECEIVER AT DIFFERENT SUPPLY VOLTAGES

Supply Voltage (V)	0.6/1.2	0.6/1	0.5/1
Power (mW)	1.7	1.2	0.8
Gain (dB)	57	58	57.5
$\mathrm{IIP3_{out\text{-}band}}$ (dBm)	–6	–4	–8
NF (dB)	8.5	11.3	12
IRR (dB)	36	38	35

22 dB (43 dB) rejection at the adjacent (alternate) channel, and 36 dB IRR. Differing from the simulated IF frequency response that has three notches at the image band under an ideal LO, the measured notches are merged. Similar to [18], this discrepancy is likely due to the LO gain and phase mismatches, and the matching and variations of the RC-CR networks. The layout design is similar to [18] that uses dummy to balance the parasitic capacitances. The filtering rejection profile is around 80 dB/decade. The spurious-free dynamic range (SFDR) is close to 60 dB according to [7], [21],

$$\mathrm{SFDR} = \frac{2(\mathrm{P_{IIP3}} + 174\ \mathrm{dBm} - \mathrm{NF} - 10\log \mathrm{BW})}{3} - \mathrm{SNR_{min}} \tag{5}$$

where $\mathrm{SNR_{min}} = 4$ dB is the minimum signal-to-noise ratio required by the application, and $\mathrm{BW} = 2$ MHz is the channel bandwidth.

The receiver was further tested at lower voltage supplies, as summarized in Table I. Only the NF degrades more noticeably; the IIP3, IRR, and BB gain are almost secured. The better IIP3 for 0.6 V/1 V operation is mainly due to the narrower -3 dB bandwidth of the hybrid filter. For the 0.5 V/1 V operation, the degradation of $\mathrm{IIP3_{out\text{-}band}}$ is likely due to the distortion generated by $\mathrm{A_{GB}}$. Both cases draw very low power down to 0.8 mW, being comparable with other ULP designs such as [4].

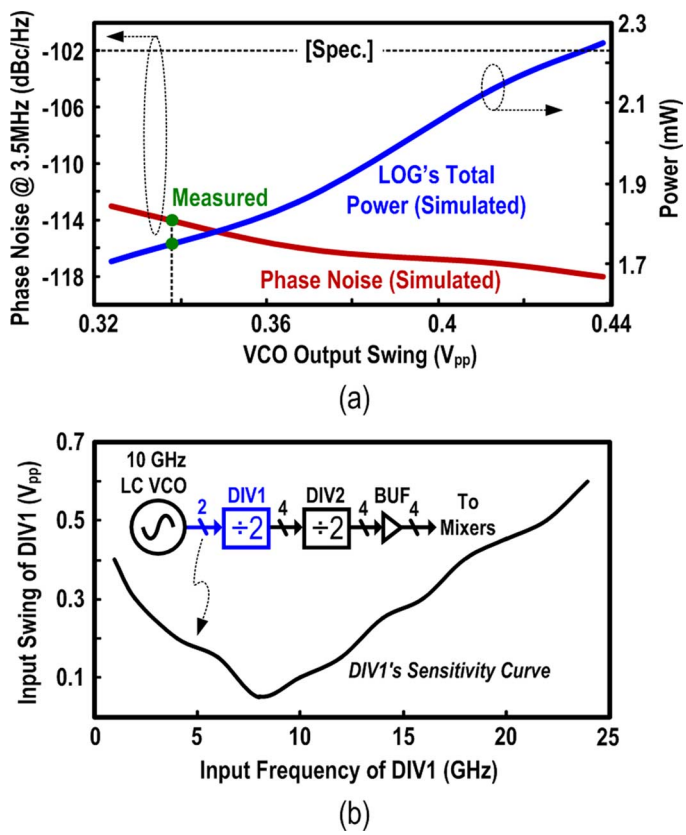


Fig. 17. (a) The measured phase noise has enough margin to the specifications. From simulations, it can be shown that it is a tradeoff with the power budget according to the VCO's output swing. (b) Simulated sensitivity curve of DIV1 showing its small input-voltage requirement at ~10 GHz.

The LC-tank VCO was tested separately. Its power budget is related with its output swing and is a tradeoff with the phase noise, which measures -114 dBc/Hz at 3.5 MHz which has enough margin to the specifications [22] [Fig. 17(a)]. Porting it

TABLE II
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART

	This Work		JSSC'10 [7]	JSSC'10 [8]	JSSC'10 [23]	ISSCC'13 [5]
Application	ZigBee		ZigBee	GPS	ZigBee/Bluetooth	Energy Harvesting
Architecture	Blixer + Hybrid-Filter + Passive RC-CR PPF		LMV Cell + Complex Filter	QLMV Cell + Complex Filter	LNA + Mixer + Complex Filter	LNA + Mixer + Frequency-translated IF Filter
BB Filtering	***1 Biquad + 4 complex poles***		3 complex poles	2 complex poles	3 complex poles	2 real poles
External I/P Matching Components	***zero***		1 inductor, 1 capacitor	1 passive balun	1 inductor, 1 capacitor	2 capacitors, 1 inductor
S_{11} < –10dB Bandwidth (MHz)	***1300 (2.25 to 3.55 GHz)***		< 300 (2.3 to 2.6 GHz)	100 (1.55 to 1.65 GHz)	> 400 (< 2.2 to 2.6 GHz)	> 600 (< 2 to 2.6 GHz)
Integrated VCO	No	Yes	Yes	Yes	No	Yes
Gain (dB)	57	55	75	42.5	67	83
Phase Noise (dBc/Hz)	NA	–115 @ 3.5 MHz	–116 @ 3.5 MHz	–110 @ 1 MHz	NA	–112.8 @ 1 MHz
NF (dB)	8.5	9	9	6.5	16	6.1
$IIP3_{out\text{-}band}$ (dBm)	***–6***	***–6***	–12.5	N/A	–10.5	–21.5
IRR (dB)	36 (worst of 5 chips)	28	35	37	32	N/A
SFDR (dB)	***60.3***	***60***	55.5	N/A	53.6	51.6
LO-to-RF Leak (dBm)	–61	–61	–60	–75	N/A	N/A
Power (mW)	***1.7 ****	***2.7***	3.6	6.2 (inc. ADC)	20	1.6
Active Area (mm^2)	***0.24***	***0.3***	0.35	1.5 (inc. ADC)	1.45	2.5
Supply Voltage (V)	0.6/1.2		1.2	1	0.6	0.3
Technology	65 nm CMOS		90 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS

* Breakdown: 1 mW: Blixer + hybrid filter + BB circuitry, 0.7 mW: DIV1 + LO Buffers

to the simulation results, it can be found that the corresponding VCO's output swing is 0.34 V_{pp} and the total LO-path power is 1.7 mW (VCO + dividers + BUFs). Such an output swing is adequate to lock DIV1 as shown in its simulated sensitivity curve [Fig. 17(b)].

The chip summary and performance benchmarks are given in Table II, where [7] and [8] are current-reuse architectures, [23] is a classical architecture with cascade of building blocks, and [5] is an ultra-low-voltage design. For this work, the results measured under a 10 GHz on-chip VCO are also included for completeness, but they are more sensitive to test uncertainties. The degraded NF and IRR are mainly due to the phase noise of the free-running VCO. In both cases, this work succeeds in advancing the $IIP3_{out\text{-}band}$, power and area efficiencies, while achieving a wideband S_{11} with zero external components. Particularly, when comparing with the most recent work [5], this work achieves 8× less area and 15.5 dBm higher IIP3, together with stronger BB channel selectivity.

V. CONCLUSIONS

A number of ULP circuits and optimization techniques have been applied to the design of a 2.4 GHz ZigBee receiver in 65 nm CMOS. The extensive-current-reuse RF-to-BB path is based on a Blixer + hybrid filter topology, which improves not only the power and area efficiencies, but also the out-band linearity due to more current-domain signal processing. Specifically, the Blixer features: 1) a low-Q input matching network realizing wideband S_{11} and robust passive pre-gain, 2) a balun-LNA with active-gain boosting and partial-noise-canceling improving the gain and NF, and 3) I/Q-DBMs driven by a 4-phase 25% LO inherently offering output balancing. For the hybrid filter, an IF-noise-shaping Biquad together with a complex-pole load synthesize third-order channel selection and first-order image rejection. All of these render current-reuse topologies with great potential for developing ULP radios in advanced CMOS processes.

APPENDIX A
$S_{11}<-10$ dB BANDWIDTH VERSUS THE Q FACTOR (Q_n) OF THE INPUT-MATCHING NETWORK [FIG. 4(A)]

At the resonant frequency ω_0, L_M can resonate perfectly with C_{EQ} and R'_{in} for an exact 50 Ω. However, at a lower frequency $\omega = \omega_0 - \Delta\omega_L$ ($\Delta\omega_L > 0$), the imaginary part of $L_M//C_{EQ}$ is non-zero, making $R'_{in} < 50\,\Omega$. This imaginary part is expressed as L_{eff} and derived as follows:

$$sL_M//sC_{EQ} = \frac{sL_M}{1+s^2C_{EQ}L_M}. \tag{A-1}$$

Let $\omega = \omega_0 - \Delta\omega_L$, where $\omega_0 = 1/\sqrt{L_M C_{EQ}}$, and if substituted into (A-1), we will have

$$\frac{j(\omega_0-\Delta\omega_L)L_M}{1-\dfrac{(\omega_0-\Delta\omega_L)^2}{{\omega_0}^2}} \approx \frac{j(\omega_0-\Delta\omega_L)L_M}{2\dfrac{\Delta\omega_L}{\omega_0}} = L_{eff} \tag{A-2}$$

where $\Delta\omega_{\rm L}/\omega_0 \ll 2$ is assumed. Here, the parallel of $|{\rm L_{eff}}| \parallel {\rm R_T}$ is down-converted to ${\rm R'_{in}} = 26\,\omega$ by $\rm C_M$ and $\rm C_p$, thus,

$$\frac{|{\rm L_{eff}}|{\rm R_T}}{|{\rm L_{eff}}| + {\rm R_T}}\left(\frac{\rm C_M}{\rm C_M + C_p}\right)^2 = 26\ \Omega. \tag{A-3}$$

Substituting (A-2) into (A-3) and simplifying them, the normalized low-side frequency is obtained:

$$\frac{\Delta\omega_{\rm L}}{\omega_0} = \frac{1}{1 + \dfrac{4{\rm a}{\rm Q_n}}{\rm R_T - a}} \tag{A-4}$$

where ${\rm a} = 26(({\rm C_M} + {\rm C_p})/{\rm C_M})^2$. Then, the whole matching bandwidth is close to twice the value derived in (A-1) if the upper side is included. Equation (A-4) confirms that the $\rm S_{11}$ bandwidth can be significantly extended by designing a low $\rm Q_n$.

Appendix B
NF of the Balun-LNA Versus the Gain ($\rm G_{m,CS}$) of the CS Branch With $\rm A_{GB}$ [Fig. 4(a)]

The ${\rm NF_{total}}$ can be reduced by increasing ${\rm g_{m,AGB}}$ under fixed ${\rm g_{m,CG}}$ and ${\rm g_{m,CS}}$, under matched input impedance. The noises from the I/Q-DBMs and their harmonic-folding terms, and the resistor $\rm R_p$, are excluded for simplicity. Also, the conversion gain of the active mixers is assumed to be unity. Here ${\rm G_{m,CS}}$ is upsized from ${\rm G_{m0,CS}}$ to ${\rm G_{m,CS}} = {\rm G_{m0,CS}} + \Delta{\rm G_{m,CS}}$, where ${\rm G_{m0\_CS}}$ is the value for full noise cancellation of CG branch, i.e., ${\rm R_{in}G_{m0,CS}} = 1$. The four major noise sources considered here are the thermal noises from ${\rm R_S}({\rm V^2_{n,Rs}} = 4{\rm kT}R_{\rm s})$, ${\rm M_1}({\rm I^2_{n,CG}} = 4{\rm kT}\gamma{\rm g_{m,CG}})$, ${\rm M_2} + {\rm A_{GB}}({\rm I^2_{n,CS}} = 4{\rm kT}\gamma G_{\rm m,CS})$ and ${\rm R_L}({\rm V^2_{n,L}} = 4{\rm kT}R_{\rm L})$, where γ is the bias-dependent coefficient of the channel thermal noise. The noise contributed by the CG branch can be deduced as

$$\begin{aligned}
&{\rm NF_{g_{m,CG}}} \\
&= \frac{\rm V^2_{n,out,CG}}{\rm V^2_{n,out,R_s}} \\
&= \frac{\frac{1}{4}{\rm I^2_{n,CG}}\left[{\rm R_L} - {\rm R_{in}}\left({\rm G_{m0,CS}} + \Delta{\rm G_{m,CS}}\right){\rm R_L}\right]^2}{4{\rm kTR_S}{\rm A^2_{pre,amp}} \times \frac{1}{4} \times \left[\frac{\rm R_L}{\rm R_{in}} + \left({\rm G_{m0,CS}} + \Delta{\rm G_{m,CS}}\right){\rm R_L}\right]^2} \\
&= \frac{\gamma{\rm g_{m,CG}}\left({\rm R_{in}R_L}\Delta{\rm G_{m,CS}}\right)^2}{{\rm R_S}{\rm A^2_{pre,amp}}\left(\frac{2{\rm R_L}}{\rm R_{in}} + \Delta{\rm G_{m,CS}}{\rm R_L}\right)^2} \\
&\approx \frac{\gamma{\rm g_{m,CG}}{\rm R_{in}}^4\left(\Delta{\rm G_{m,CS}}\right)^2}{4{\rm A^2_{pre,amp}}{\rm R_S}} \\
&\quad \Delta{\rm G_{m,CS}}
\end{aligned} \tag{B-1}$$

where $2{\rm R_L}/{\rm R_{in}} \gg \Delta{\rm G_{m,CS}}{\rm R_L}$. if $\Delta{\rm G_{m,CS}}$ is increased, the noise from $\rm M_1$ also moves up. However, for the noise contribution of the CS branch, we can derive its TF to the output ($\rm V_{out}$) as

$$\begin{aligned}
{\rm TF_{G_{m,CS}\to V_{out}}} &= \frac{\rm R_L}{1+{\rm T}}\left[\frac{\rm T}{{\rm R_{in}}\left({\rm G_{m0,CS}} + \Delta{\rm G_{m,CS}}\right)} + 1\right] \\
&\approx {\rm R_L}\left(1 - \Delta{\rm G_{m,CS}}{\rm R_{in}}\right)
\end{aligned}$$

where T is the loop gain $\gg 1$. With it, the NF of Q and NF of $\rm G_{m,CS}$ can be derived:

$$\begin{aligned}
&{\rm NF_{G_{m,CS}}} \\
&= \frac{\rm V^2_{n,out,CS}}{\rm V^2_{n,out,R_s}} \\
&= \frac{4{\rm kT}\gamma\left({\rm G_{m,CS}} + \Delta{\rm G_{m,CS}}\right)\left({\rm TF_{G_{m,CS}\to V_{out}}}\right)^2}{4{\rm kTR_S}{\rm A^2_{pre,amp}} \times \frac{1}{4} \times \left(\frac{2{\rm R_L}}{\rm R_{in}} + \Delta{\rm G_{m,CS}}{\rm R_L}\right)^2} \\
&\approx \frac{\gamma{\rm R^2_{in}}\left({\rm G_{m0,CS}} + \Delta{\rm G_{m,CS}}\right)\left(1 - \Delta{\rm G_{m,CS}}{\rm R_{in}}\right)^2}{{\rm R_S}{\rm A^2_{pre,amp}}} \\
&\approx \frac{\gamma{\rm R_{in}}\left(1 - \Delta{\rm G_{m,cs}}{\rm R_{in}}\right)}{{\rm R_S}{\rm A^2_{pre,amp}}}
\end{aligned} \tag{B-2}$$

$$\begin{aligned}
&{\rm NF_{R_L}} \\
&= \frac{4{\rm kTR_L}}{4{\rm kTR_S}{\rm A^2_{pre,amp}} \times \frac{1}{4} \times \left[\frac{\rm R_L}{\rm R_{in}} + \left({\rm G_{m,CS}} + \Delta{\rm G_{m,CS}}\right){\rm R_L}\right]^2} \\
&\approx \frac{4{\rm R_L}}{{\rm R_S}{\rm A^2_{pre,amp}}} \frac{1}{\left(\frac{4{\rm R_L^2}}{\rm R^2_{in}} + \frac{2\Delta{\rm G_{m,CS}}{\rm R_L^2}}{\rm R_{in}}\right)} \\
&\approx \frac{\rm R^2_{in}}{{\rm R_L}{\rm R_S}{\rm A^2_{pre,amp}}}\left(1 - \frac{\Delta{\rm G_{m,CS}}{\rm R_{in}}}{2}\right).
\end{aligned} \tag{B-3}$$

As expected, when $\Delta{\rm G_{m,CS}}$ is increased, the noise contribution of $\rm G_{m,CS}$ and $\rm R_L$ can be reduced. The optimal $\Delta{\rm G_{m,CS}}$ can be derived from $\partial{\rm NF_{total}}/\partial\Delta{\rm G_{m,CS}} = 0$, where ${\rm NF_{total}} = 1 + {\rm NF_{G_{m,CG}}} + {\rm NF_{G_{m,CS}}} + 2{\rm NF_{R_L}}$.

References

[1] P. Choi, H. Park, S. Kim, S. Park, I. Nam, T. W. Kim, S. Park, S. Shin, M. S. Kim, K. Kang, Y. Ku, H. Choi, S. M. Park, and K. Lee, "An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4 GHz," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2258–2268, Dec. 2003.

[2] C.-H. Li, Y.-L. Liu, and C.-N. Kuo, "A 0.6-V 0.33-mW 5.5-GHz receiver front-end using resonator coupling technique," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 6, pp. 1629–1638, Jun. 2011.

[3] B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. Pister, "Low-power, 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2767–2775, Dec. 2006.

[4] A. C. Herberg, T. W. Brown, T. S. Fiez, and K. Mayaram, "A 250-mV, 352-μW GPS receiver RF front-end in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 938–949, Apr. 2011.

[5] F. Zhang, K. Wang, J. Koo, Y. Miyahara, and B. Otis, "A 1.6 mW 300 mV supply 2.4 GHz receiver with −94 dBm sensitivity for energy-harvesting applications," in *2013 IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 456–457.

[6] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "The Blixer, a wideband balun-LNA-I/Q-mixer topology," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2706–2715, Dec. 2008.

[7] M. Tedeschi, A. Liscidini, and R. Castello, "Low-power quadrature receivers for ZigBee (IEEE 802.15.4) applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1710–1719, Sep. 2010.

[8] K.-W. Cheng, K. Natarajan, and D. Allstot, "A current reuse quadrature GPS receiver in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 510–523, Mar. 2010.

[9] D. Ghosh and R. Gharpurey, "A power-efficient receiver architecture employing bias-current-shared RF and baseband with merged supply voltage domains and 1/f noise reduction," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 381–391, Feb. 2012.

[10] Z. Lin, P.-I. Mak, and R. P. Martins, "A 1.7 mW 0.22 mm^2 2.4 GHz ZigBee RX exploiting a current-reuse Blixer + hybrid filter topology in 65 nm CMOS," in *2013 IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 448–449.

[11] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.
[12] P.-I. Mak and R. P. Martins, "A 0.46-mm^2 4-dB NF unified receiver front-end for full-band mobile TV in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1970–1984, Sep. 2011.
[13] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.
[14] A. Pirola, A. Liscidini, and R. Castello, "Current-mode, WCDMA channel filter with in-band noise shaping," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1770–1780, Sep. 2010.
[15] C. L. Ler, A. K. A'ain, and A. V. Kordesh, "CMOS source degenerated differential active inductor," *IET Electronics Lett.*, vol. 44, pp. 196–197, Jan. 2008.
[16] Y. Chen, P.-I. Mak, L. Zhang, and Y. Wang, "A 0.07 mm^2, 2 mW, 75 MHz-IF, 4th-Order BPF using a source-follower-based resonator in 90 nm CMOS," *IET Electronics Lett.*, vol. 48, pp. 552–554, May 2012.
[17] J. Kaykovuori, K. Stadius, and J. Ryynanen, "Analysis and design of passive polyphase filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3023–3037, Nov. 2008.
[18] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 9, pp. 873–887, Sep. 2001.
[19] M. Camus, B. Butaye, L. Garcia, M. Sie, B. Pellat, and T. Parra, "A 5.4 mW/0.007 mm^2 2.4 GHz front-end receiver in 90 nm CMOS for IEEE 802.15.4 WPAN standard," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1372–1383, Jun. 2008.
[20] B. Razavi, K. F. Lee, and R. H. Yan, "Design of high-speed, low-power frequency dividers and phase-locked loops in deep submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 30, no. 2, pp. 101–109, Feb. 1995.
[21] B. Razavi, *RF Microelectronics*, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2011.
[22] A. Liscidini, M. Tedeschi, and R. Castello, "A 2.4 GHz 3.6 mW 0.35 mm^2 quadrature front-end RX for ZigBee and WPAN applications," in *2008 IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 370–371.
[23] A. Balankutty, S. A. Yu, Y. Feng, and P. Kinget, "A 0.6 V zero-IF/low-IF receiver with integrated fractional-N synthesizer for 2.4 GHz ISM-band applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 538–553, Mar. 2010.

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