A Nonrecursive Digital Calibration Technique for Joint Elimination of Transmitter and Receiver I/Q Imbalances With Minimized Add-On Hardware

Wei-Han Yu, Chak-Fong Cheang, Pui-In Mak, *Senior Member, IEEE*, Weng-Fai Cheng, Ka-Fai Un, U-Wai Lok, and Rui P. Martins, *Fellow, IEEE*

***Abstract*—A nonrecursive digital calibration technique, namely, local oscillator (LO) switching, is proposed for jointly eliminating transmitter (TX) and receiver (RX) I/Q imbalances in one combined process. The add-on analog parts are limited to a set of source followers (0.00228 mm^2) and metal–oxide–semiconductor (MOS) switches (0.00017 mm^2) for reusing the 90° phase shift property of the reference LO, avoiding the sinusoidal test tone, loop-back detector, high-speed analog-to-digital converter, and 2-D iterative search algorithm, mostly required in the prior art. A 65-nm complementary MOS transceiver, which is codesigned with a field-programmable-gate-array-based coordinate rotation digital computer algorithm, measures a 10-dB improvement in the image rejection ratio of both the TX (27.8 → 37.2 dB) and the RX (31.2 → 42 dB). The required digital circuitry for the algorithm is also assessed and simulated.**

***Index Terms*—Algorithm, calibration, coordinate rotation digital computer (CORDIC), I/Q imbalance, local oscillator (LO), receiver (RX), transceiver, transmitter (TX).**

I. Introduction

QUADRATURE modulation is fundamental in nearly all wireless transceivers for its high spectral efficiency; however, mismatches of components and the physical layout can always lead to gain and phase mismatches between the I and Q signals [1], [2]. The resultant image effect can significantly degrade the error vector magnitude (EVM), particularly for very dense signal constellations, such as 16-quadrature amplitude modulation (QAM) and 64-QAM [3]. Since I/Q imbalances can happen in the receiver (RX), the transmitter (TX), and the local oscillator (LO), the desired calibration algorithm should be able to correct them with minimum add-on hardware for better cost and area efficiencies.

A number of techniques have been reported to deal with the I/Q-imbalance problem. Examples are the loop-back detector with a recursive algorithm [4], [5], a 2-D iterative search algorithm [6], [7], and a blind estimation algorithm [8], [9]. The first two are still demanding in hardware and computation, inducing a long calibration time and would be power and area hungry in its implementation. For the third, although no training sequence is entailed, the estimation process still involves heavy computation (e.g., inverse matrix) and can suffer from the instability issue in the recursive loop. This brief introduces a nonrecursive digital calibration technique for joint correction of RX and TX I/Q imbalances under a reference LO. The technique is named *LO switching*. The add-on analog parts are limited to a set of source followers and metal–oxide–semiconductor (MOS) switches. The latter is to employ the 90° phase shift property of the LO available in most quadrature transceivers, generating adequate conditions to estimate the I/Q-imbalance parameters nonrecursively. The experimental verification is based on a 65-nm complementary MOS (CMOS) transceiver chip codesigned with a coordinate rotation digital computer (CORDIC) algorithm [10] implemented in the field-programmable gate array (FPGA).

Section II overviews the system codesign, including the transceiver chip and the calibration algorithm implemented in the FPGA. Section III describes the principle of the algorithm, highlighting its joint estimation capability for both TX and RX I/Q imbalances in a combined process. The measurement results are given in Section IV. Section V concludes this brief.

II. Transceiver–FPGA System Codesign

A. Transceiver Chip (Fig. 1, Right)

Fig. 1 shows the block schematic of the system. In the calibration mode, the RF output from the TX mixers is looped back to the RX via the TX–RX switch, such that the calibration process can be moved to the digital domain, reusing the existing hardware while, more importantly, linking up together the I/Q imbalances of both the RX and the TX for joint calibration. The integrated TX consists of two first-order passive-RC low-pass filters (LPFs) for reconstructing the I and Q inputs generated by the off-chip digital-to-analog converters (DACs). After I/Q

Manuscript received March 18, 2013; accepted May 31, 2013. Date of publication June 27, 2013; date of current version August 10, 2013. This work was supported in part by the Research Committee of the University of Macau, Macau, China, and in part by the Macao Science and Technology Development Fund (FDCT). This brief was recommended by Associate Editor C. H. Heng.

W.-H. Yu, C.-F. Cheang, P.-I. Mak, W.-F. Cheng, and K.-F. Un are with the State Key Laboratory of Analog and Mixed-Signal VLSI and the Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau, China (e-mail: pimak@umac.mo).

U.-W. Lok was with the State Key Laboratory of Analog and Mixed-Signal VLSI and the Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau, China. He is now with National Taiwan University, Taipei 106, Taiwan.

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI and the Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau, China, and also with the Instituto Superior Técnico, Technical University of Lisbon, Lisbon 1049-001, Portugal (e-mail: rmartins@umac.mo).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2013.2268412

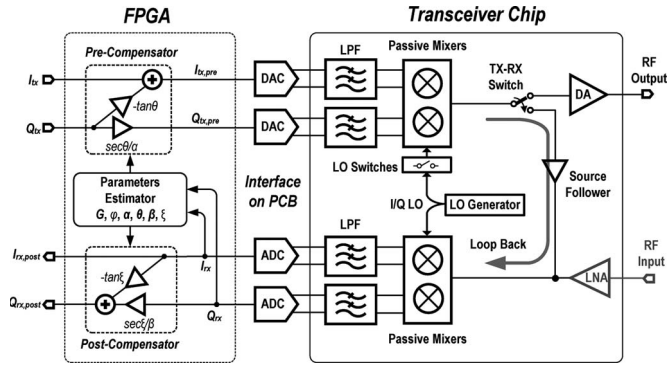

Fig. 1. CMOS transceiver chip codesigned with an FPGA implementing the proposed I/Q-imbalance digital calibration algorithm.

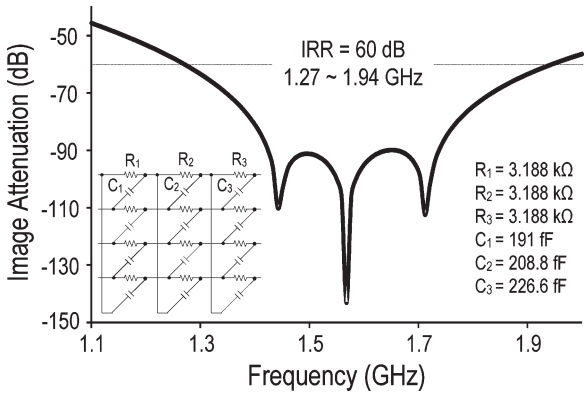

Fig. 2. Three-stage $RC-CR$ network is robust enough (IRR $= 60$ dB) as a PPF for generating a high I/Q-accuracy LO against process variations.

upconversion by the passive mixers, a single-ended class-B driver amplifier (DA) with an inductive load delivers the RF output for 50-Ω measurements.

Focused on the calibration mode, the on-chip RX path is a simplified solution for rapid prototyping. In the baseband, only first-order active-RC LPFs are employed to suppress the image at $2\times$ LO frequency generated by the TX, which is already adequate to minimize the calibration error due to aliasing in the analog-to-digital converters (ADCs).

Unlike in [7], where a high-speed subsampling ADC (e.g., 200 MHz) was required to serve as the loop-back RX, here, we simply reuse the existing RX mixers, LPFs, and ADCs that are much relaxed in speed (e.g., 80 MHz). The source follower is to isolate the passive mixers between the TX and the RX. The low-noise amplifier was not integrated as our interest is on I/Q-imbalance calibration.

The proposed I/Q-imbalance calibration employs the LO as the reference such that joint calibration of the RX and the TX can be achieved. Thus, the I/Q accuracy of the LO is crucial and must be robust over process variations. Here, the LO path is led by an active balun implemented with a cascaded differential amplifier and followed by an $RC-CR$ network as the polyphase filter (PPF) for four-phase sine-LO generation at $\sim$1.4 GHz (a frequency that is convenient for this design). As shown in Fig. 2 from simulations, for an image rejection ratio (IRR) of 60 dB, a three-stage $RC-CR$ network with properly positioned poles is adequate to cover a broad spectrum (1.27–1.94 GHz), such that the worst RC variations can still be tolerated.

At the circuit level, before driving the four-phase LO to the I/Q passive mixers, logic operation is applied to transform them from sine-LO into a set of 25% duty cycle square-LO with guard intervals, avoiding I/Q crosstalk, while saturating the LO amplitude to improve gain balancing. The circuit details are omitted here due to the space limit.

B. FPGA (Fig. 1, Left)

For the TX digital baseband, the imbalanced baseband output can be modeled as $x_{\mathrm{tx,imb}}(t) = 1_{\mathrm{tx,imb}} + jQ_{\mathrm{tx,imb}}$, such that

$$\begin{bmatrix} I_{\mathrm{tx,imb}} \\ Q_{\mathrm{tx,imb}} \end{bmatrix} = \begin{bmatrix} 1 & \alpha \sin\theta \\ 0 & \alpha \cos\theta \end{bmatrix} \begin{bmatrix} I_{\mathrm{tx}} \\ Q_{\mathrm{tx}} \end{bmatrix} \tag{1}$$

where the gain and phase imbalances are represented by α and θ, respectively. Similarly, for the RX, the imbalanced baseband output is given by

$$\begin{bmatrix} I_{\mathrm{rx,imb}} \\ Q_{\mathrm{rx,imb}} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \beta \sin\xi & \beta \cos\xi \end{bmatrix} \begin{bmatrix} I_{\mathrm{rx,ideal}} \\ Q_{\mathrm{rx,ideal}} \end{bmatrix} \tag{2}$$

where the gain and phase imbalances are represented by β and ξ, respectively. $I_{\mathrm{rx,ideal}}$ and $Q_{\mathrm{rx,ideal}}$ refer to the down-converted output with an ideal RF input with no I/Q imbalance.Such an RF model is used as the basis for the following estimation process. With a reference LO mixed with the digital baseband signals, we obtain the RF signal as

$$s_{\mathrm{RF}} = (I_{\mathrm{tx}} + \alpha \sin\theta\, Q_{\mathrm{tx}}) \cos\omega t + \alpha \cos\theta\, Q_{\mathrm{tx}} \sin\omega t. \tag{3}$$

The precompensation of the TX and the postcompensation of the RX are operated by directly inversing the baseband system model between the TX and the RX, in which both matrices can be represented as*Compensation for TX*

$$\begin{bmatrix} I_{\mathrm{tx,pre}} \\ Q_{\mathrm{tx,pre}} \end{bmatrix} = \begin{bmatrix} 1 & -\tan\theta \\ 0 & \sec\ \theta/\alpha \end{bmatrix} \begin{bmatrix} I_{\mathrm{tx}} \\ Q_{\mathrm{tx}} \end{bmatrix}. \tag{4}$$

Compensation for RX

$$\begin{bmatrix} I_{\mathrm{rx,post}} \\ Q_{\mathrm{rx,post}} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\tan\xi & \sec\ \xi/\beta \end{bmatrix} \begin{bmatrix} I_{\mathrm{rx}} \\ Q_{\mathrm{rx}} \end{bmatrix}. \tag{5}$$

III. Proposed LO Switching I/Q-Imbalance Calibration

The I/Q imbalance model is shown in Fig. 3(a). The overall gains of the TX and the RX are denoted by A and B, respectively, and the overall phase shift passing through them is denoted by φ. The outputs for the TX baseband are I_{tx} and Q_{tx}, and the inputs for the RX baseband are I_{rx} and Q_{rx}. As shown in Fig. 3(a), if a dc training signal is sent from I_{tx} and Q_{tx} separately into the system, only four equations are available to estimate the wanted I/Q-imbalance parameters. Consequently, only the conventional least mean squares method can be applied, which is slow [11], [12] and has limited accuracy [12]. The LO switching technique presented here has the objective of

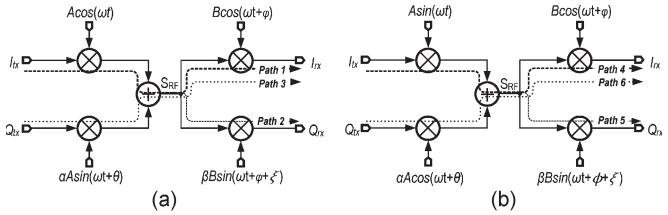

Fig. 3. (a) Typical transceiver system model with I/Q imbalances, from which three equations can be obtained from paths 1–3. (b) With the proposed LO switching technique in the TX, three more independent equations can be obtained from paths 4–6.

finding more independent equations. The procedure is twofold: 1) transmit a dc training signal from $I_{\rm tx}$ and $Q_{\rm tx}$ to the system; and 2) switch the LO such that an extra 90° phase shift can be set between the two input channels, offering more equations to solve the desired I/Q-imbalance parameters. Specifically, if a dc training signal with amplitude c at $I_{\rm tx}$ and $Q_{\rm tx}$ is separately injected into the I/Q imbalance model, the output signals can be represented as

The output signal through Path 1

$$\begin{aligned} I_{\rm rx,Path1} &= \text{LPF}\{cA\cos(\omega t)B\cos(\omega t+\phi)\} \\ &= \frac{cAB}{2}\cos\phi. \end{aligned} \tag{6}$$

The output signal through Path 2

$$\begin{aligned} Q_{\rm rx,Path2} &= \text{LPF}\{cA\cos(\omega t)\beta B\sin(\omega t+\phi+\xi)\} \\ &= \frac{c\beta AB}{2}\sin(\phi+\xi). \end{aligned} \tag{7}$$

The output signal through Path 3

$$\begin{aligned} I_{\rm rx,Path3} &= \text{LPF}\{c\alpha A\sin(\omega t+\phi)B\cos(\omega t+\phi)\} \\ &= \frac{c\alpha AB}{2}\sin(\theta-\phi). \end{aligned} \tag{8}$$

Then, considering Fig. 3(b), the phase of the LO is switched for a phase shift of 90°. In this case, if we transmit a dc training signal at $I_{\rm tx}$ and $Q_{\rm tx}$, the output signals can be represented as

The output signal through Path 4

$$\begin{aligned} I_{\rm rx,Path4} &= \text{LPF}\{cA\sin(\omega t)B\cos(\omega t+\phi)\} \\ &= -\frac{cAB}{2}\sin\phi. \end{aligned} \tag{9}$$

The output signal through Path 5

$$\begin{aligned} Q_{\rm rx,Path5} &= \text{LPF}\{cA\sin(\omega t)\beta B\sin(\omega t+\phi+\xi)\} \\ &= \frac{c\beta AB}{2}\cos(\phi+\xi). \end{aligned} \tag{10}$$

The output signal through Path 6

$$\begin{aligned} I_{\rm rx,Path6} &= \text{LPF}\{c\alpha A\cos(\omega t+\theta)B\cos(\omega t+\phi)\} \\ &= \frac{c\alpha AB}{2}\cos(\theta-\phi). \end{aligned} \tag{11}$$

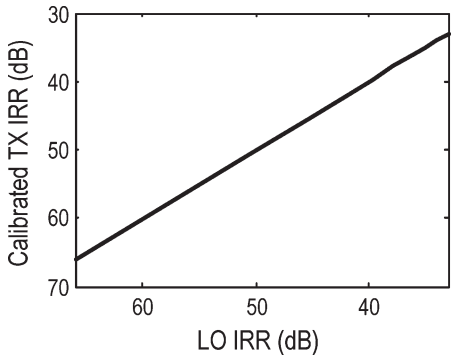

Fig. 4. Calibrated TX IRR with respect to LO IRR.

Thus, the overall gain $G = AB/2$ and the overall phase shift ϕ can be computed as

$$G = \sqrt{(I_{\rm rx,Path1}/c)^2 + (I_{\rm rx,Path4}/c)^2} \tag{12}$$

$$\phi = \tan^{-1}(I_{\rm rx,Path4}/I_{\rm rx,Path1}). \tag{13}$$

Finally, the gain and phase mismatches of the TX and the RX are solved, leading to

$$\alpha = G^{-1}\sqrt{(I_{\rm rx,Path6}/c)^2 + (I_{\rm rx,Path3}/c)^2} \tag{14}$$

$$\theta = \tan^{-1}(I_{\rm rx,Path3}/I_{\rm rx,Path6}) + \phi \tag{15}$$

$$\beta = G^{-1}\sqrt{(Q_{\rm rx,Path2}/c)^2 + (Q_{\rm rx,Path5}/c)^2} \tag{16}$$

$$\xi = \tan^{-1}(Q_{\rm rx,Path2}/Q_{\rm rx,Path5}) - \phi. \tag{17}$$

The feasibility of the above algorithm can be limited by 1) the numerical estimation accuracy and 2) the LO's gain and phase errors. For the former, Verilog simulations show a maximum gain error of 8×10^{-4} and a phase error of $\pm0.1°$ in number estimation under 10^5 time runs, which correspond to an IRR of 65 dB. Thus, the former should not be the limiting factor for most transceivers.

For the latter, we can consider a nonideal LO as $LO = \gamma e^{j\omega t+\eta}$, where γ (η) denotes the LO gain (phase) error. The achievable IRR in the TX with respect to that of the LO is plotted in Fig. 4. They are linearly related. Thus, for an IRR of 60 dB in the LO (see Fig. 2), the IRR of the TX and the RX should only be limited by themselves.

IV. Measurement Results

A. Transceiver Chip and Test Setup

The transceiver was fabricated in a 65-nm CMOS process, and the chip micrograph is shown in Fig. 5. The active die area is 0.82×0.5 mm^2, of which only 0.00245 mm^2 is due to the LO switches and source followers added to assist the calibration. The experimental setup is shown in Fig. 6. The baseband I/Q signals are generated by the ALTERA DE4 FPGA. It interfaces with the RX and the TX through the Texas Instrument DACs (5662) and ADCs (ADS62P23). Both

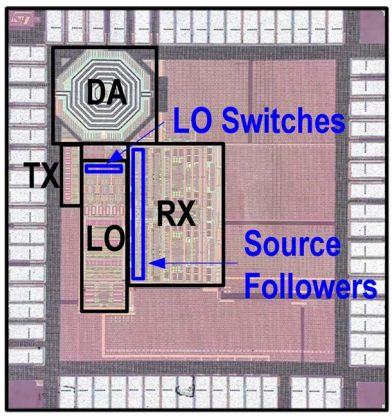

Fig. 5. Chip micrograph of the fabricated 65-nm CMOS transceiver. The only add-on analog parts for calibration are the LO switches and source followers.

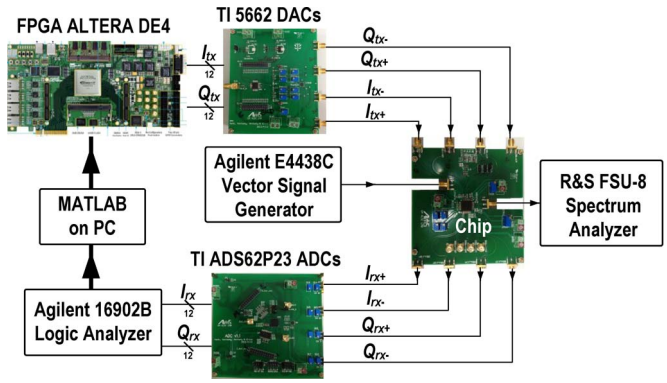

Fig. 6. Experimental setup.

have a 12-bit resolution and an 80-MHz conversion rate. The master clock is generated by the FPGA for synchronization. All RF and LO switches are driven by the FPGA through digital level shifters downscaling the control signal from 3.3 to 1.2 V, befitting the employed 65-nm CMOS devices. The output signal from the DA is measured by the R&S FSU-8 spectrum analyzer for the single-tone test. The digital outputs from the FPGA are captured by the Agilent 16902B logic analyzer for the RX postcompensation test.

B. Algorithm Implemented in the FPGA and Simulated in ASIC

Fig. 7 shows the time diagram of the data picking process. The preread phase learns the dc offsets. A dc signal with amplitude c ($\sim$0.2 V, to uphold the linearity) is then transmitted at $I_{\rm tx}$, to obtain $I_{\rm rx}$ and $Q_{\rm rx}$. Afterward, transmit data are exchanged, i.e., $I_{\rm tx} = 0$ and $Q_{\rm tx} = c$ to obtain $I_{\rm rx}$, where $Q_{\rm rx}$ is ignored. The process is repeated once after creating the 90° phase shift via LO switching. After data collection, the I/Q-imbalance parameters are computed in the FPGA with (12)–(17) in Section III. The computation employs a CORDIC algorithm, in which only shift bits and adders are required in the entire computation, rendering it very power and area efficient. For example, after picking $I_{\rm rx,Path1}$ and $I_{\rm rx,Path4}$, (12) and (13) can be solved by the CORDIC after 25 clock cycles under a 100-MHz clock rate. Since there are three sets of equations,

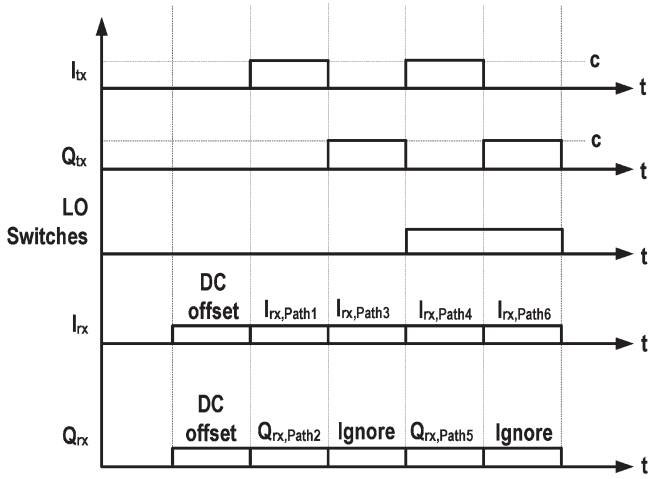

Fig. 7. Calibration time diagram.

TABLE I
POWER CONSUMPTION AND AREA SIMULATED WITH STANDARD 65-nm CMOS PROCESS AT 1.1 V AND 25 °C

FPGA Operation	Algorithm	Number of Operators Used	Power		No. of Gate	Area (μm^2)	No. of Clock Cycle
			Leakage (nW)	Switching (nW)			
Parameter Estimator	CORDIC	1	55282.87	214631.06	2104	8107.32	25x3
Compensator	Secant	2	12209.07	62558.95	241	1055.6	1
	Division	2	19533.42	73553.22	421	1597.44	9
	Multiplication	4	22362.89	68595.1	371	1714.44	1
	Addition	2	1814.31	9544.43	36	149.76	1

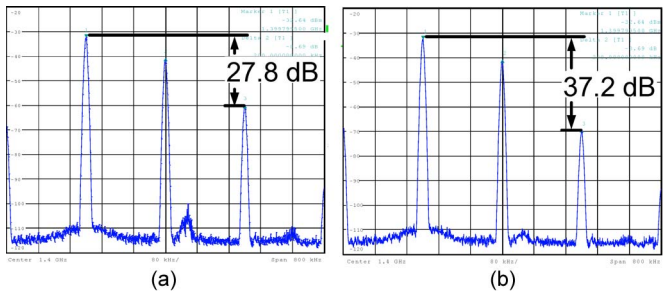

Fig. 8. TX output (a) before and (b) after calibration.

75 clock cycles are entailed totally. There is one more clock cycle for the computation of the parameters in (4) and (5).

The algorithm is also converted into a 65-nm CMOS application-specific integrated circuit (ASIC) under the Cadence Encounter, the required power, area, and calibration time are estimated, as summarized in Table I. The simulated digital power during compensation is 366.55 μW, and the entire calibration process takes 760 ns and consumes 206 pJ of energy to complete at a 100-MHz clock rate. The entailed digital area is $\sim$0.02 mm^2.

C. IRR Before and After Calibration

Fig. 8(a) and (b) shows the TX output spectra for a single-tone test before and after calibration, respectively. The IRR is improved from 27.8 to 37.5 dB. The calculated I/Q-imbalance parameters are shown in Table II. The results of the RX before

TABLE II
CALCULATED I/Q IMBALANCE PARAMETERS

G	φ	α	θ	β	ξ
0.3055	44.7003°	1.0281	-3.2828°	1.0823	1.9306°

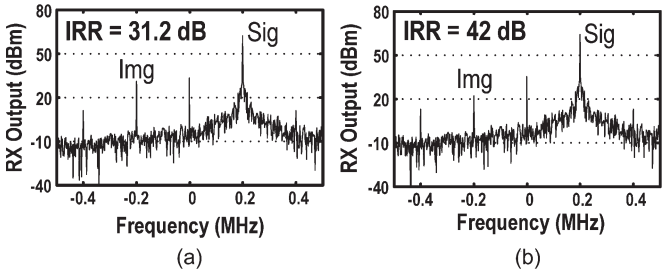

Fig. 9. RX output (a) before and (b) after calibration.

TABLE III
CHIP SUMMARY

Technology		65 nm CMOS
Transceiver Chip Area		0.41 mm^2
Analog Area for Calibration		0.00245 mm^2
Operation Frequency		1.4 GHz
Power Consumption	RX Path	18 mW
	LO Generator	22 mW
	DA	20 mW
TX IRR Before and after Calibration		27.8 dB → 37.2 dB
RX IRR Before and after Calibration		31.2 dB → 42 dB

and after postcompensation are shown in Fig. 9(a) and (b), respectively. The IRR is improved from 31.2 to 42 dB. For a 64-QAM orthogonal frequency-division multiplexing signal, these results correspond to 4% improvement of EVM from 6% to 2% for the TX and 2.86% improvement of EVM from 3.84% to 0.98% for the RX.

For wideband applications [5], the proposed method can be extended using different sets of I/Q-imbalance parameters trained under a number of selected frequencies in the baseband bandwidth. A preliminary study shows that a digital baseband detector is required to add, and the compensator has to be transformed into a finite-impulse response filter.

D. Summary and Architectural Comparison

The measurement summary is given in Table III. The add-on analog area is extremely small (0.00245 mm^2) as most circuitry is reused between the TX and the RX.

As the hardware between this work and [4], [6], and [7] can be very different, they should not be directly compared. Nevertheless, we can summarize their features in Table IV. Note that only [4] and this work can jointly calibrate the TX and the RX. Although the achieved 37.2–42-dB IRRs are suboptimal, this work exhibits attractive advantages, such as nonrecursive operation, joint-calibration capability of the TX and the RX in one combined process, and low requirement on the analog and digital parts. Indeed, the achieved IRR is fairly adequate for many wireless applications but should be improvable when implementing in a monolithic ASIC.

TABLE IV
COMPARISON WITH THE STATE OF THE ART

	2-D Search	Sine Test Tone	Dedicated Detector	High-Speed ADC	TX IRR Improved	RX IRR Improved
This Work [1]	×	×	×	×	10 dB	10 dB
[4] [2]	✓	✓	✓	×	12 dB	12 dB
[6]	✓	✓	✓	×	15.6 dB	No
[7]	✓	✓	×	✓	24 dB	No

[1] Reuse of RX mixers, LPFs and ADCs. The only add-on hardware is a set of source followers and MOS switches.

[2] Result is extracted from the gain and phase mismatches

V. CONCLUSION

A nonrecursive digital calibration technique for joint elimination of TX–RX I/Q imbalances has been described. The only add-on analog hardware is a set of source followers and MOS switches for generating an extra 90° phase shift in the reference LO, which is shared among the TX and the RX. The I/Q accuracy of the LO is optimized at the circuit level via employing a three-stage $RC-CR$ network to achieve adequate I/Q accuracy over process variations. This work avoids the sinusoidal test tone, loop-back detector, high-speed ADC, and 2-D recursive search algorithm that were commonly required in the prior art. A 65-nm CMOS transceiver prototype codesigned with an FPGA-implemented algorithm shows a 10-dB improvement in the IRR of both the TX and the RX in one combined process.

REFERENCES

[1] M. Valkama and M. Renfors, "A novel image rejection architecture for quadrature radio receivers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 2, pp. 61–68, Feb. 2004.
[2] J. Yim, T. Kim, S. Ko, W. Ko, H. Shin, I. Ryu, S.-G. Yang, J.-D. Bae, and H. Park, "Design and analysis of an ultra-wideband automatic self-calibrating upconverter in 65-nm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 7, pp. 2178–2191, Jul. 2012.
[3] A. Georgiadis, "Gain, phase imbalance, and phase noise effects on error vector magnitude," *IEEE Trans. Veh. Technol.*, vol. 53, no. 2, pp. 443–449, Mar. 2004.
[4] Y.-H. Hsieh, W.-Y. Hu, S.-M. Lin, C.-L. Chen, W.-K. Li, S.-J. Chen, and D. J. Chen, "An auto-I/Q calibrated CMOS transceiver for 802.11g," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2187–2192, Nov. 2005.
[5] L. Yu and W. M. Snelgrove, "A novel adaptive mismatch cancellation system for quadrature IF radio receivers," *IEEE Trans. Circuits Syst. II, Analog Digital Process.*, vol. 46, no. 6, pp. 789–801, Jun. 1999.
[6] C. P. Lee, A. Behzad, D. Ojo, M. Kappes, S. Au, M.-A. Pan, K. Carter, and S. Tian, "A highly linear direct-conversion transmit mixer transconductance stage with local oscillation feedthrough and I/Q imbalance cancellation scheme," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 1450–1459.
[7] E. Lopelli, S. Spiridon, and J. van der Tang, "A 40 nm wideband direct-conversion transmitter with sub-sampling-based output power, LO feedthrough and I/Q imbalance calibration," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 424–426.
[8] L. Anttila, M. Valkama, and M. Renfors, "Frequency-selective I/Q mismatch calibration of wideband direct-conversion transmitters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 4, pp. 359–363, Apr. 2008.
[9] M. Valkama, M. Renfors, and V. Koivunen, "Blind I/Q signal separation-based solutions for receiver signal processing," *EURASIP J. Adv. Signal Process.*, vol. 2005, no. 16, pp. 2708–2718, Jan. 2005.
[10] R. Andraka, "A survey of CORDIC algorithms for FPGA based computers," in *Proc. ACM/SIGDA Conf.*, 1998, pp. 191–200.
[11] I. Elahi, K. Muhammad, and P. T. Balsara, "Parallel correction and adaptation engines for I/Q mismatch compensation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 1, pp. 86–90, Jan. 2009.
[12] J. K. Cavers and M. W. Liao, "Adaptive compensation for imbalance and offset losses in direct conversion transceivers," *IEEE Trans. Veh. Technol.*, vol. 42, no. 4, pp. 581–588, Nov. 1993.