A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC

Si-Seng Wong, U-Fat Chio, *Member, IEEE*, Yan Zhu, *Member, IEEE*, Sai-Weng Sin, *Senior Member, IEEE*, Seng-Pan U, *Senior Member, IEEE*, and Rui Paulo Martins, *Fellow, IEEE*

***Abstract*—This paper presents the architecture of a 10b 170 MS/s two-step binary-search assisted time-interleaved SAR ADC. The front-end stage of this ADC is built with a 5b binary-search ADC, which is shared by two time-interleaved 6b SAR ADCs in the second-stage. The design does not use any static component such as op-amp or preamplifier that causes large dissipation of static power. DAC settling speed and power are also relaxed thanks to this architecture. Besides, the process insensitive asynchronous logic further reduces the delay of SA loop rather than using worst case delay cells to compensate the process variation problem. The ADC was fabricated in 65 nm CMOS and achieves 54.6 dB SNDR at 170 MS/s with only 2.3 mW of power consumption, leading to a FoM of 30.8 fJ/conversion-step.**

***Index Terms*—Analog-to-digital converter (ADC), binary-search ADC, SAR ADC, time-interleaved, two-step ADC.**

I. Introduction

TRADITIONAL pipelined ADCs [1]–[4] require multiple op-amps that consume large amounts of static power and become challenge for design with technology scaling. In recent years pipelined-SAR ADCs [5]–[8] were proposed to achieve both high-speed and low-power specifications by reducing the number of op-amps. This was done by taking advantage of SAR ADC benefits. However, the requirement of interstage gain in the architecture of pipelined-SARs still required at least one op-amp, which still consumed static power [5]–[8].

The SAR ADCs only use fully dynamic elements to achieve low power consumption [9]–[12]. Pipelined-SAR [5]–[8], time-interleaved SAR [13], [14] and flash-SAR [15], [16] ADCs were reported to partially employ SAR as their sub ADCs to overcome the speed bottleneck while retaining the benefits of low power consumption in SAR. The binary-search ADCs [17]–[19] achieve both low-power and high-speed using the binary-search algorithm. The main problem of this architecture is its limited resolution caused by comparators' offsets and exponential growth of switch matrixes and decoders [18], [19].

This paper presents a two-step binary-search assisted time-interleaved (TI) SAR ADC architecture, which takes the advantages of speed, resolution, and power offered by the two types of ADCs. Through an analysis of energy consumption, it is demonstrated that the selected bit allocation of the binary-search TI SAR ADC is the most energy efficient when compared to other high-speed dynamic SAR based ADC architectures. A $(5 + 6 - 1)$-bit binary-search TI SAR ADC can reduce 48% of energy consumed when compared to a 10b dual-channel TI SAR ADC. Furthermore, a process insensitive asynchronous SAR logic is also presented that auto-detects the logic delay of each cycling bit, instead of using a worst case delay control as [20].

II. Dynamic SAR Based ADCs

SAR ADCs benefit from their simple structure, the analog part whereof only includes one DAC array and one comparator. However, the implementation of single comparator always requires full resolution quantization for all bits, which in turn slows down the SA loop and consumes more power. For instance, the first 9 bits quantization of a 10b SAR ADC requires a $>$10b comparator. Thus, the comparator consumes 10b comparator power for all 10 clock cycles.

With the help of subranging quantization using digital error correction, the accuracy of the components is relaxed. For instance, the tolerated error of a M-bit coarse stage in a two-step $(\mathrm{M} + \mathrm{N} - 1)$-bit subranging ADC with 1b digital error correction overlapping can be expressed as

$$\varepsilon_{\mathrm{C}} = \frac{V_{\mathrm{FS}}}{2^{\mathrm{M}+1}} \tag{1}$$

and the tolerated error of the N-bit fine stage becomes

$$\varepsilon_{\mathrm{F}} = \frac{V_{\mathrm{FS}}}{2^{\mathrm{M}+\mathrm{N}}} \tag{2}$$

where V_{FS} is the input full scale. Only considering the nonlinearity from the comparator, (1) reveals that the offset and noise requirement of coarse-stage comparator can be mitigated as M-bit. Assuming that there is a $(5{+}6{-}1)$-bit subranging SAR ADC, the 5b coarse comparator power can be reduced drastically compared to a full 10b implementation. There is only a little drawback on speed as one more bit must be quantized in fine stage. The flash-SAR and pipelined-SAR ADCs also benefit from subranging quantization that reduces the coarse-stage power.

Manuscript received December 05, 2012; revised March 28, 2013; accepted March 28, 2013. Date of publication May 20, 2013; date of current version July 19, 2013. This paper was approved by Guest Editor Ken Suyama. This work was supported in part by Research Grants from University of Macau and Macao Science and Technology Fund (FDCT).

S.-S. Wong and S.-P. U are with the State Key Laboratory of Analog and Mixed Signal VLSI and the Faculty of Science and Technology, University of Macau, Macao, China, and also with Synopsys Macau Ltd., Macao, China (e-mail: dickywongis@gmail.com).

U.-F. Chio, Y. Zhu, and S.-W. Sin are with the State Key Laboratory of Analog and Mixed Signal VLSI and the Faculty of Science and Technology, University of Macau, Macao, China.

R. P. Martins is with the State Key Laboratory of Analog and Mixed Signal VLSI and the Faculty of Science and Technology, University of Macau, Macao, China. He is on leave from Instituto Superior Técnico/TU, Lisbon, Portugal.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2013.2258832

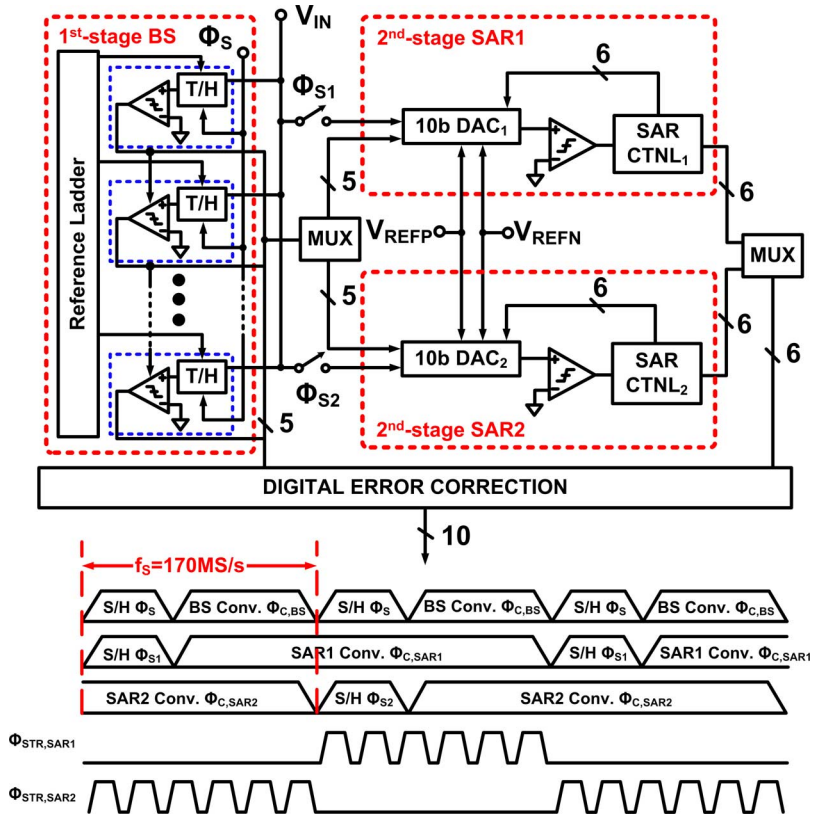


Fig. 1. Block diagram of the proposed 10b two-step ADC.

Fig. 1 shows the ADC architecture, together with its timing diagram. The design is composed of a high-speed binary-search ADC shared by two interleaved lower-speed SAR ADCs. The first-stage uses the architecture of [19] rather than [17] and [18] because it resolves the kickback noise problem with minimum number of comparators. The second-stage TI SAR ADCs convert the rest 6b fine code. Each SAR ADC consists of a 10b capacitive DAC array, a dynamic comparator, and SAR control logic. Two stages have 1b overlapping for digital error correction.

From the timing diagram shown in Fig. 1, we see that the T/Hs of the first-stage binary-search ADC and the second-stage DAC_1 sample the input signal simultaneously at the sampling phase ($\Phi_{\mathrm{S1}} = $ '1'). In the conversion phase ($\Phi_{\mathrm{C,BS}} = $ '1'), the first-stage quantizes the coarse code and passes to the second-stage SAR1. The DAC_1 then subtracts the reference voltage from the sampled-input according to the coarse code. Meanwhile the first-stage together with the DAC_2 in SAR2 samples the input again. Therefore, the use of binary-search ADC exhibits an optimized trade-off between speed and power with the two SAR ADCs.

III. Energy Analysis

In this prototype design a 5b resolution is selected for the first-stage binary-search ADC while 6b resolution is allocated to the second-stage TI SAR ADCs. Through energy analysis the comparison will demonstrate that the bit allocation selected for the binary-search TI SAR ADC is the most energy efficient when comparing to other bit allocations as well as other high-speed dynamic SAR based ADC architectures. For purpose of high-speed comparison binary-search TI SAR, flash TI SAR and dual-channel TI SAR ADCs are chosen to develop the energy theoretical models. This is taking into consideration of resolution, speed, input swing, supply voltage, and process parameters. A dynamic comparator is employed in the energy model development and digital calibration is assumed to alleviate the comparators' offset mismatch under 10b resolution.

A. Binary-Search TI SAR Energy Model

The energy model is developed using a $(\mathrm{M}+\mathrm{N}-1)$-bit binary-search TI (BS-TI) SAR ADC. The first-stage binary-search ADC is M-bit resolution, whereas the second-stage TI SAR ADC is N-bit, with 1-bit overlapping for digital error correction. The basic BS-TI SAR ADC includes M comparators, reference ladder, and decoder for coarse stage, together with two comparators, N-bit SAR logic control block, SA loop, and $(\mathrm{M}+\mathrm{N}-1)$-bit capacitor DAC array for fine stage.

1) Binary-Search Comparator: The size of the dynamic comparator is determined by the thermal noise. After digital error correction the tolerated error of M-bit coarse stage is alleviated within M-bit from (1). To simplify the estimation, the thermal noise of the comparator is set equal to M-bit quantization noise level. Thus, according to [22], the loading capacitance of the binary-search comparator, $\mathrm{C_{BL}}$, is given as follows:

$$\mathrm{C_{BL}} \approx \frac{\mathrm{k}\cdot\mathrm{T}\cdot\gamma}{V^2_{n\_q,M-bit}}\cdot\frac{V_{\mathrm{ov}}}{V_{\mathrm{DD}}} = \frac{3\cdot 2^{2(\mathrm{M}+1)}\cdot\mathrm{k}\cdot\mathrm{T}\cdot\gamma}{V^2_{\mathrm{FS}}}\cdot\frac{V_{\mathrm{ov}}}{V_{\mathrm{DD}}} \quad (3)$$

where $V^2_{n\_q,\mathrm{M-bit}}$ is the thermal noise of the comparator, γ is the noise coefficient and V_{ov} is the over-drive voltage of the input transistors. Therefore, the energy per conversion of the binary-search comparators becomes

$$E_{\mathrm{BSTI,comp}} = \mathrm{M} \cdot \mathrm{C_{BL}} \cdot V^2_{\mathrm{DD}}. \tag{4}$$

2) SAR Comparator: The tolerated nonlinear error of N-bit SAR ADC is $(\mathrm{M+N-1})$-bit as seen in (2). To simplify the estimation the thermal noise of comparator is set to $(\mathrm{M+N-1})$-bit quantization noise level (i.e. the energy of the ADCs is compared under the 0.5b ENOB performance drop from the ideal). Therefore, the loading capacitance of SAR comparator, $\mathrm{C_{SL}}$, is given as follows:

$$\mathrm{C_{SL}} \approx \frac{\mathrm{k \cdot T \cdot \gamma}}{V^2_{n\_q,M+N-1\text{-bit}}} \cdot \frac{V_{\mathrm{ov}}}{V_{\mathrm{DD}}} = \frac{3 \cdot 2^{2(\mathrm{M+N})} \cdot \mathrm{k \cdot T \cdot \gamma}}{V^2_{\mathrm{FS}}} \frac{V_{\mathrm{ov}}}{V_{\mathrm{DD}}}. \tag{5}$$

Hence, the energy per conversion of the SAR comparators becomes

$$E_{\mathrm{SA,comp}} = \mathrm{N} \cdot \mathrm{C_{SL}} \cdot V^2_{\mathrm{DD}}. \tag{6}$$

B. Flash TI SAR Energy Model

This energy model is developed using an $(\mathrm{M+N-1})$-bit flash TI (FL-TI) SAR ADC. The first-stage flash ADC is M-bit resolution, and the second-stage TI SAR ADC is N-bit, with 1-bit overlap between the two step quantization. The FL-TI SAR ADC includes $2^{\mathrm{M}}-1$ comparators, reference ladder, and encoder for coarse stage, with the configuration for the same fine stage as above.

1) Flash Comparator: In terms of the architecture the noise and accuracy requirements of flash comparators in FL-TI SAR ADC is the same as binary-research comparators in BS-TI SAR ADC using (1). Therefore, the required loading capacitance of flash comparator, $\mathrm{C_{FL}}$, is equal to $\mathrm{C_{BL}}$.

Therefore, the energy per conversion of the flash comparators becomes

$$E_{\mathrm{FLTI,comp}} = (2^{\mathrm{M}}-1) \cdot \mathrm{C_{FL}} \cdot V^2_{\mathrm{DD}}. \tag{7}$$

C. Dual-Channel TI SAR Energy Model

This energy model is developed using a $(\mathrm{M+N-1})$-bit dual-channel TI SAR ADC. Because the TI SAR ADC does not get the merit of subranging quantization, it has to be utilized to full resolution requirement. The tolerated nonlinearity error of N-bit SAR ADC is $(\mathrm{M+N-1})$-bit as in (2). Therefore, the required loading capacitance of SAR comparator by thermal noise is the same as (5). The energy per conversion of the dual-channel TI SAR comparators becomes

$$E_{\mathrm{TISA,comp}} = (\mathrm{M+N-1}) \cdot \mathrm{C_{SL}} \cdot V^2_{\mathrm{DD}}. \tag{8}$$

In order to achieve the most efficient performance for 10b resolution while operating with 1 V supply-voltage, the theoretical energy is estimated versus allocated resolutions of the binary-search (flash) and the TI SAR as shown in Fig. 2. The curves from Fig. 2 are derived and obtained from the theoretical energy model in (4), (6), (7), and (8), and the power equations (binary-search ADC decoder, SAR DAC array, SAR logic, and flash ADC encoder) are derived in the Appendix with the process parameters from a 65 nm CMOS technology. There is also a resistor reference ladder in the binary-search ADC. In practice the resistor reference ladder is just meant to provide static reference voltage to the comparator. Its energy scale can be ignored when compared to the total consumption as the reference ladder only consumes 9% of the overall ADC power. The binary-search TI SAR ADC achieves the best energy efficiency while the first-stage binary-search is at 5b resolution and the second-stage TI SAR is at 6b resolution. Compared with the 10b dual-channel TI SAR ADC a $(5+6-1)$-bit binary-search TI SAR ADC can reduce 48% of energy. On the other hand the best bit allocation of flash TI SAR is to assign 4b flash and 7 b TI SAR for lower energy consumption. The energy versus output code for TI and subranging ADCs are estimated according to the switching sequence of each code with 5b first-stage and 6b second-stage configuration as shown in Fig. 3.

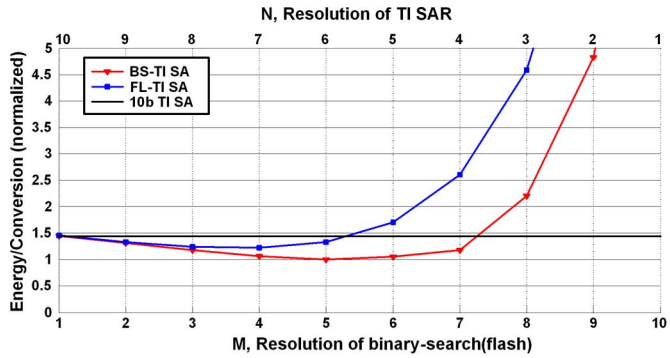


Fig. 2. Energy efficiencies of binary-search TI SAR, flash TI SAR and dual-channel TI SAR ADCs with 10b resolutions (All normalized to the $(5+6-1)$-bit binary-search TI SAR ADC).

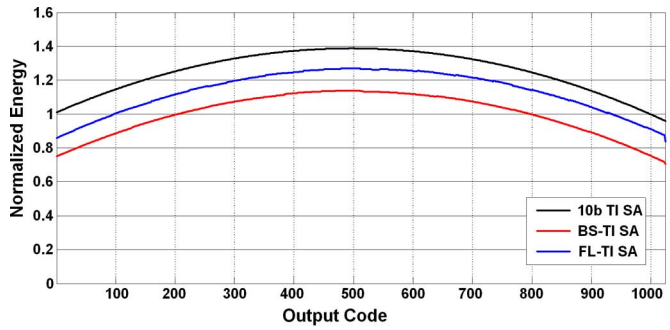


Fig. 3. Energy efficiency versus ADC output code with 5b first-stage and 6b second-stage (All normalized to average energy of binary-search TI SAR ADC).

IV. Design Considerations

The design considerations of the proposed architecture includes interstage error (errors between first and second stage), time-interleaved (mismatching between TI SAR), and DAC nonlinearity. The first-stage conversion accuracy is relaxed to 6b (including comparator offset, noise, reference, and time error between the first and second stage) because of the 1b overlapping by error correction. For the second-stage, the conversion accuracy is 11b because of unity interstage gain.

A. Inter-Stage Errors

Both first and second stage use bottom plate sampling, and the second-stage residue is generated by digital code together

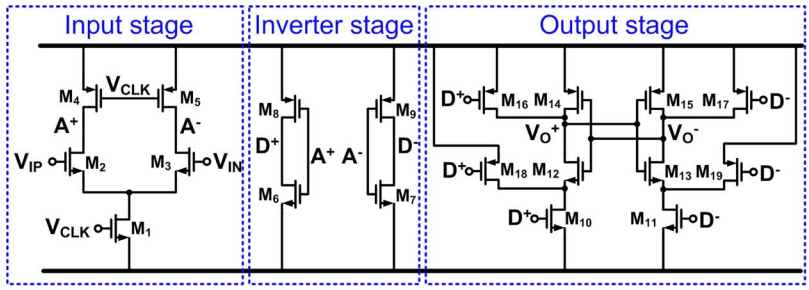


Fig. 4. Implemented three-stage dynamic comparator.

with input signal at the DAC arrays rather than the analog-signal alone. Therefore, the interstage gain error caused by the parasitic capacitances at the top-plates of the several T/Hs and DAC arrays can be avoid. The resistive reference ladder, which can be easily designed at a matching level of >6b, is implemented for the binary-search ADC.

The offset requirement of first-stage is 25 mV according to (1). The offset is corrected by offset calibration through unbalanced capacitive loading [21]. Besides, the full-scale voltage ($V_{\rm FS}$) of second-stage is $\pm 25\ {\rm mV_{P-P}}$ since input range of the ADC is $\pm 0.8\ {\rm V_{P-P}}$. If the offset of second-stage is larger than 25 mV, the error correction range and the input of second-stage will be saturated. Thus, a high-resolution, low-noise, and low-offset comparator is required for the second-stage as there is no amplification between the stages. A three-stage dynamic comparator [23] is utilized for this implementation, as shown in Fig. 4, because of its low-noise, low-offset, and high-resolution performance. During the reset phase ($\rm V_{CLK}$ = '0') the intermediate nodes ($\rm A^+, A^-$) and output nodes ($\rm V_O^+, V_O^-$) are charged to $V_{\rm DD}$ to clear the memory of previous data. Once the comparator is activated ($\rm V_{CLK}$ = '1'), the input and inverter stages amplify the input difference to suppress noise and offset. The output stage latches the amplified signal to the output by regeneration of the back-to-back inverters. In this implementation the comparator achieves 11b resolution, which is clocked at 600 MHz by the SA loop, and consumes 132 μW of power. From simulation results, the 3σ offset voltage is obtained as 12.8 mV. This addresses the design constrain.

The timing error between the first and second stage can be tolerated by the error correction. The timing mismatch between the stages is 32 ps for the proposed architecture. The clock generator is placed between the binary-search ADC and the two SAR ADCs as shown in Fig. 5 in order to match the routing distances between stages. It is not difficult to optimize the timing error by balancing the wire length (75 μm), width (0.1 μm), and loading between the stages. As observed in post-layout simulation results, the 3σ timing error between the stages is only 6.2 ps.

B. Time-Interleaved Mismatches

The matching requirement of the reference voltages between the TI second-stage SARs can be calculated as according to [24]

$$\mathrm{SNDR_{gain,mis}} = 20 \cdot \log\left(\frac{a}{\sigma_{\rm gmis}}\right) - 10 \cdot \log\left(1 - \frac{1}{\rm M}\right) \quad (9)$$

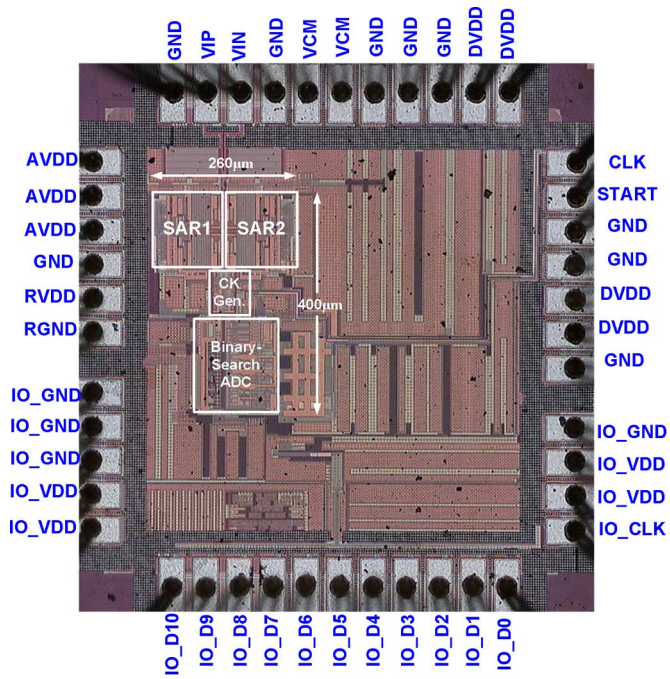


Fig. 5. Chip micrograph.

where a is the input range and the matching requirement σ_{gmis} is 0.11% for the proposed design aimed at achieving 62 dB SNDR. This matching is decided by capacitor matching of the DAC array, and this can be achieved using symmetry and common-centroid layout technique.

The offset mismatch between the channels of the second-stage requires a 1σ of 0.7 mV to get 62 dB SNDR as according to [24]

$$\mathrm{SNDR_{off,mis}} = 10 \cdot \log\left(\frac{V_{\rm FS}^2}{2\sigma_0^2}\right). \quad (10)$$

In this design, the second-stage's comparators offset is cancelled in the digital domain by subtracting the mean code between channels using off-chip calibration as [8]. The calibration topology obtains the offset information of each channel by averaging the output code, where the mean codes do not contain any information about timing skew, gain error, or noise. The offset difference between channels can be calculated by subtracting the mean codes of the channels, and thus the calibrated ADC output code is also obtained by subtracting this offset difference from a channel's output.

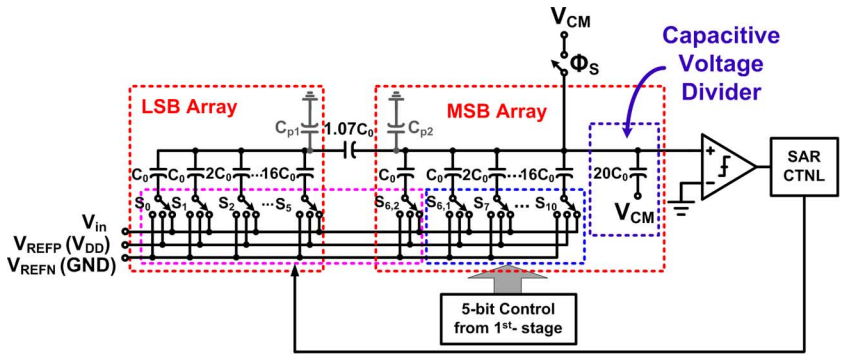


Fig. 6. Split capacitive DAC array.

Since the second-stage SARs are using different DAC arrays to sample the interleaved input signal as shown in Fig. 1, the timing skew requirement of the second-stage SARs can be calculated as according to [24]

$$\mathrm{SNDR}_{\mathrm{time,mis}} = 20\cdot\log\left(\frac{1}{\sigma_t 2\pi f_{\mathrm{in}}}\right) - 10\cdot\log\left(1-\frac{1}{\mathrm{M}}\right) \quad (11)$$

where M is the number of interleaving channels. From (11), when the interleaving channel is more than two, the timing skew requirement is strengthened. So using two time-interleaved channels for the proposed architecture can achieve optimal performance. For a two-channel 10b 170 MS/s ADC the matching requirement of the interleaved signal must be $<$2.1 ps at Nyquist input frequency. Therefore, the interleaved clocks are generated by the master clock through a divide-by-2 low-skew clock generator [25]. From the post-layout simulation results, we see that the 3σ timing skew between the channels is 1.33 ps, which can address the design constrain.

C. DAC Nonlinearity

Fig. 6 shows the split DAC structure which is implemented due to its low total capacitance and small area. The reference voltages of the DAC array are connected to the ground and analog supply V_{DD}, since there is a capacitive voltage divider $(20\mathrm{C}_0)$. This in turn is determined by the full-scale input of $1.6\mathrm{V}_{\mathrm{p-p}}$. The output of a split capacitive DAC array can be expressed as in (12), shown at the bottom of the page, where M represents the number of bits in MSB array and L represents the LSB array. C_{p1} and C_{p2} are the total top-plate parasitic of LSB array and MSB array, respectively. From (12) it is seen that the parasitic C_{p2} only causes gain error because it only affects the denominator of the overall equation. This is not problematic because of bottom-plate sampling. However, parasitic C_{p1}, brings nonlinearity to the DAC array because there is a nominator difference between the MSB and LSB switching. In order

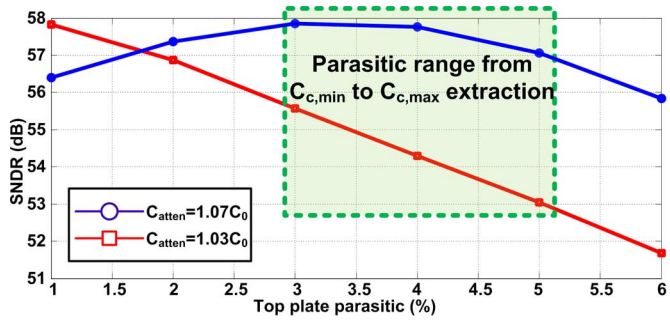


Fig. 7. SNDR versus top-plate parasitic in the implemented split capacitive DAC array w/& w/o attenuation compensation.

to compensate for this error, we can equalize the nominators by enlarging the $\mathrm{C}_{\mathrm{atten}}$ as follows:

$$\mathrm{C}_{\mathrm{atten}} \approx \frac{\mathrm{C}_{\mathrm{TotalLSB}} + \mathrm{C}_{\mathrm{P1}}}{\mathrm{C}_{\mathrm{TotalLSB}} - \mathrm{C}_0}\cdot \mathrm{C}_0. \quad (13)$$

The unit capacitor C_0 is formed by Metal–Oxide–Metal (MOM) fringing structure, which results in a unit value of 20 fF. From the layout extraction results we see that the top-plate parasitic capacitance of a 20 fF capacitor varies from 3% to 5%. $\mathrm{C}_{\mathrm{atten}}$ on the other hand is designed to $1.07\mathrm{C}_0$ rather than conventional value of $1.03\mathrm{C}_0$. The SNDR versus top-plate parasitic with and without $\mathrm{C}_{\mathrm{atten}}$ compensation is shown in Fig. 7. From the graph it is observed that the compensated $\mathrm{C}_{\mathrm{atten}}$ is able to cover the ranges of top-plate parasitic over corner, while the SNDR drops within 1 dB rather than $>$5 dB drop as conventional case (shown in the highlighted area of Fig. 7). Besides the parasitic variation, the $\mathrm{C}_{\mathrm{atten}}$ mismatch also affects the linearity of the DAC. Fig. 8 shows the SNDR versus $\mathrm{C}_{\mathrm{atten}}$ mismatch. The SNDR of the ADC drops within 1 dB while there is $\pm 1\%$ of $\mathrm{C}_{\mathrm{atten}}$ mismatch. Therefore, the compensated split capacitor array can achieve medium resolution without any calibration.

$$V_{\mathrm{out}}(X) = \frac{(\mathrm{C}_{\mathrm{TotalLSB}} + \mathrm{C}_{\mathrm{atten}} + \mathrm{C}_{\mathrm{p1}})\left[\sum_{\mathrm{n}=1}^{\mathrm{M}}(2^{\mathrm{n}-1}\mathrm{C}_0)\cdot \mathrm{S}_{\mathrm{n}} + \mathrm{C}_0\mathrm{S}_{6,1}\right] + \mathrm{C}_{\mathrm{atten}}\left[\sum_{\mathrm{n}=1}^{\mathrm{L}}(2^{\mathrm{n}-1}\mathrm{C}_0)\cdot \mathrm{S}_{\mathrm{n}}\right]}{(\mathrm{C}_{\mathrm{TotalLSB}} + \mathrm{C}_{\mathrm{atten}} + \mathrm{C}_{\mathrm{p1}})(\mathrm{C}_{\mathrm{TotalMSB}} + \mathrm{C}_{\mathrm{atten}} + \mathrm{C}_{\mathrm{p2}}) - \mathrm{C}_{\mathrm{atten}}^2} V_{\mathrm{REF}} \quad (12)$$

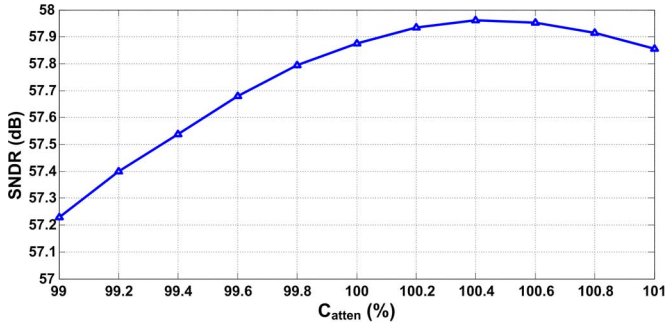


Fig. 8. SNDR versus C_{atten} mismatch at 4% top-plate parasitic.

V. Circuit Implementation

A. MSB Settling Relaxation

Since the MSB array is settled before SAR starts quantization, the requirement of MSB settling time is relaxed [15] compared to conventional SAR. In the proposed scheme the resistance of the reference switch can be six times smaller compared to conventional dual-channel SAR ADCs for 170 MS/s implementation. This reduces the size of the reference switches and parasitic dramatically, which leads to less buffers implementation for power saving.

B. First-Stage Binary-Search ADC

Fig. 9 shows the 5b binary-search ADC for the first-stage, which is modified from [19]. There are five substages and each substage has its own comparator and distributed T/Hs. In total nine T/Hs are used and the unit capacitance of each T/H is 50 fF. The comparators of the substages are activated one-by-one asynchronously without any feedback loop to achieve both low power and high speed. The static reference ladder power is minimized by starting the reference voltage settling at (M-2)-bit quantization steps before the M-bit quantizes [18] [19].

A code overflow occurs when the output code of the first-stage is "11111." In general flash sub-ADCs one comparator must be removed, so that the maximum output code can be "11110." However, in the implemented binary-search ADC, if the comparator of the last substage is removed, the LSB code is lost. Therefore, when the first 4b code is "1111" the supply voltage is selected as residue rather than a reference voltage for the last substage. Also, the input voltage is never larger than the supply voltage such that the comparator of the last substage will quantize an output bit of "0," and the maximum code can only be "11110."

C. Process Insensitive Asynchronous Logic

The main dominating delays of the SA loop are comparator delay, digital logic delay, and DAC settling delay. In conventional SAR ADC design approaches, the worst case delay cells are implemented for all of these delays to ensure that the SA loop is clocked properly. In response to this the asynchronous SAR logic was invented with a view to reduce the worst case comparator delay, which uses a fixed delay of comparator ready signal to trigger the asynchronous logic as indicated in Fig. 10(a) [20]. However, there is a logic delay variation including the SAR control logic and switch

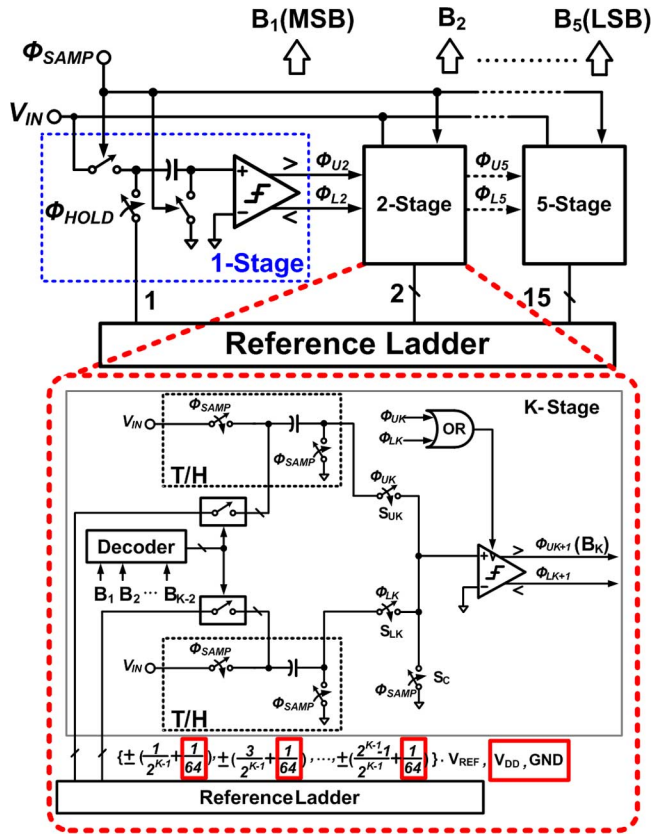


Fig. 9. Implemented 5b binary-search ADC with redundant references.

buffers delay $(\Delta t_{logic,1}, \Delta t_{logic,2}, \ldots, \Delta t_{logic,K})$ because of the process variation, which causes incorrect quantization. This happens when the comparator is clocked before switching signals $(S_{P,1}, S_{N,1} \ldots S_{P,k}, S_{N,k})$. So comparator strobe delay cell must provide a delay larger than the total delay from comparator to the switching signals. With process variation of switching logic delay and strobe delay cell, it is difficult to guarantee that the delay cell can generate an accurate delay. To address this worst case logic delay was implemented for the logic delay path to ensure the comparator is always clocked properly [20]. Besides, the worst case logic delay is mainly depends on the MSB control logic and buffers, the SA loop speed is not optimized since there is significantly less delay for the LSB control logic and buffers.

The proposed process insensitive asynchronous logic solves both comparator and logic delay variations. This is shown in Fig. 10(b), together with its timing diagram. The proposed scheme uses switching signals to trigger the asynchronous loop instead of a fixed delay of comparator ready signal, so that it does not require any tunable or worst case delay cells to overcome the process variation problem caused by the control logic and buffers. Since the MSB capacitors are settled before second-stage conversion, the DAC settling delay is significantly reduced. Therefore, the DAC settling delay is not the dominant delay of the SA loop.

The operation of the proposed logic is separated into five steps. During the reset phase (Φ_R = '0'), the logic is reset to V_{DD} at node B_i such that the SA loop is disabled (1). Once the SAR starts quantization (2), the comparator is clocked, and the

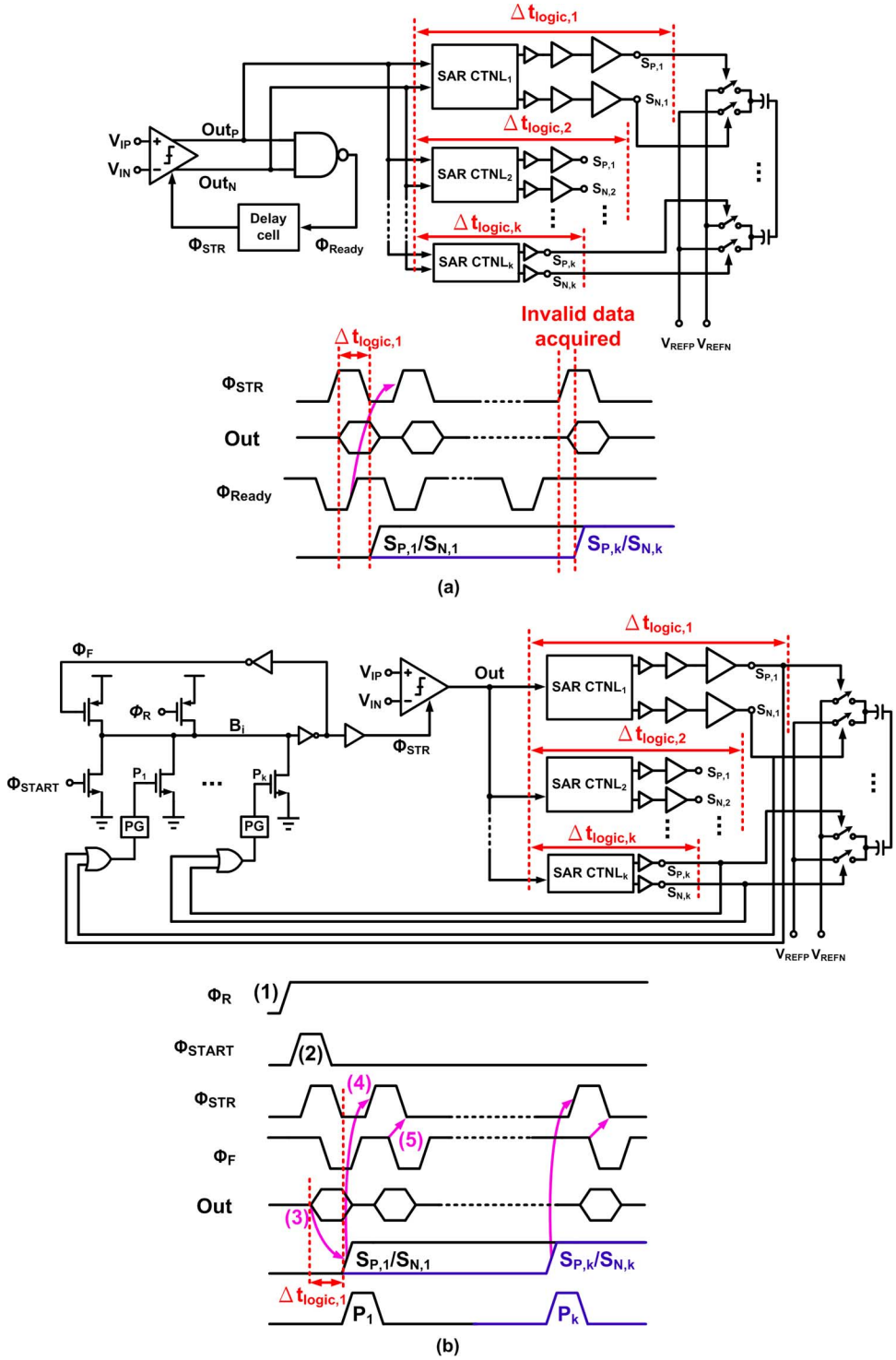


Fig. 10. (a) Traditional SAR asynchronous logic and timing diagram. (b) Proposed process insensitive asynchronous logic scheme.

control logic provides a switching signal (3) to select an appropriate reference voltage (V_{REFP}/V_{REFN}) connecting to the DAC. The switching signal ($\mathrm{S_{P,1}/S_{N,1}} \ldots \mathrm{S_{P,k}/S_{N,k}}$ = '1') discharges the dynamic node $\mathrm{B_i}$ to clock the comparator (4). The pulse generator (PG) logic limits the pulse width of the digital output signal ($\mathrm{P_1} \ldots \mathrm{P_k}$), so the feedback signal (Φ_F = '0') can charge the dynamic node again to pull down the comparator clock (5). The asynchronous logic repeats (3) to (5) until the last bit is quantized wherein the comparator is always clocked after the switching signal and the SA loop speed is not limited by the worst case delay path (MSB control logic and buffers) as the delay of control logic and buffers are automatically detected. In this way, the SA loop is clocking itself at its optimized frequency. At the same time, it is insensitive to the process variation from comparator delay and logic delay by the proposed asynchronous logic.

VI. Measurement Results

The prototype ADC was fabricated in 1P7M 65 nm CMOS. The active area of ADC core is 0.104 mm^2 (260 μm $\times$ 400 μm).

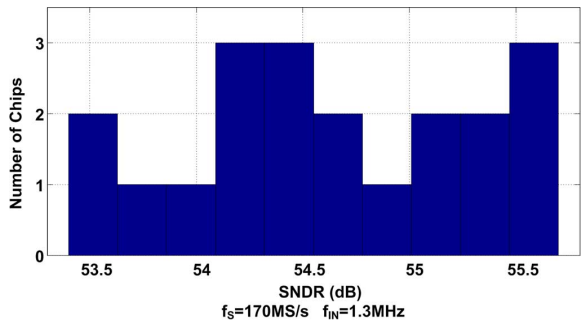


Fig. 11. Measured SNDR histogram.

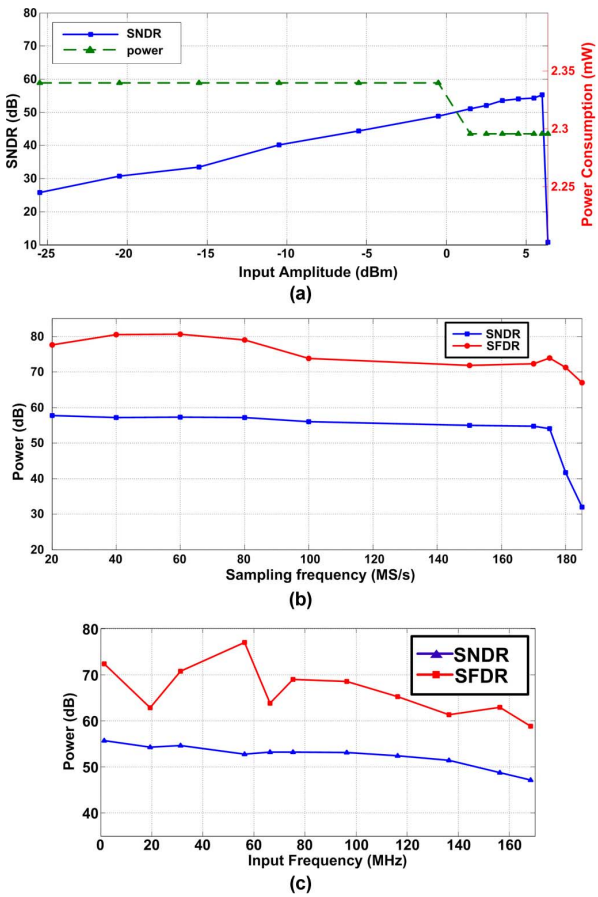


Fig. 12. (a) SNDR, SFDR, and power consumption versus input amplitude at 1.31512 MHz. (b) SNDR and SFDR versus sampling frequency at fixed normalized frequency ($f_{in}/f_s = 0.1934$). (c) SNDR and SFDR versus input frequency.

The prototype ADC consumes 2.3 mW of power operating at 170 MS/s including 0.2 mW reference ladder power (9% of total power), 0.57 mW analog power (25% of total power including T/Hs, DACs, and comparators) and 1.52 mW digital power (66% of total power including clock generator, SAR logic, and binary-search ADC decoder). The speed of the ADC is dominated by the interleaved SAR channels. However, since the speed of the ADC is fully optimized for sampling and first-stage quantization equals to the second-stage quantization, there is no improvement in speed whatsoever. This is in spite of further interleaving the second-stage channels.

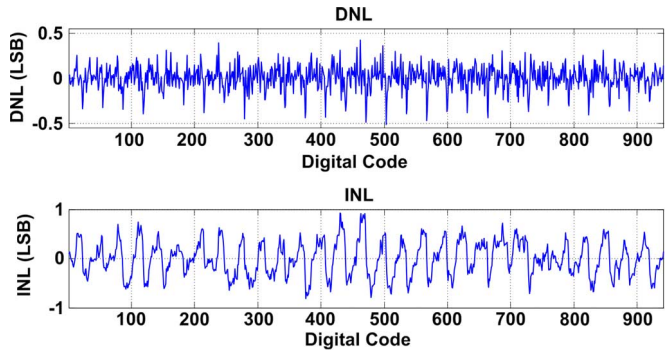


Fig. 13. Measured DNL/INL.

Fig. 11 shows the measurement result among 20 chips. No offset and timing skew tones are observed within the chips. Based on the mean performance among the chips, the measured SNDR at 1.31512 MHz input is 54.6 dB. The FoM, defined as $\mathrm{FoM} = \mathrm{Power}/(2^{\mathrm{ENOB}} \cdot f_s)$ is 30.8 fJ/conv.-step. The SNDR at Nyquist input frequency is 53.2 dB, with a resulting FoM of 36.4 fJ/conv.-step. The SNDR, SFDR, and power consumption versus input amplitude are shown in Fig. 12(a). Fig. 12(b) and (c) shows the SNDR and SFDR versus sampling frequency at fixed normalized frequency ($f_{in}/f_s = 0.1934$) and input frequency respectively, and the ERBW is 116 MHz. Fig. 13 shows the measured DNL/INL. The DNL is $+0.42/-0.52$ LSB and the INL is $+0.93/-0.81$ LSB. Fig. 14 shows both the measured FFT spectrum at DC and near Nyquist input. The performance summary and comparison with state-of-the-art pipelined-SAR, pipelined, and flash-SAR ADCs are shown in Table I.

VII. Conclusions

This paper presents a 10b 170 MS/s two-step binary-search assisted time-interleaved SAR ADC architecture, where the ADC's front-end is built with a 5b binary-search ADC, shared by two time-interleaved 6b SAR ADCs in the second-stage. The bit allocation of the $(5{+}6{-}1)$-bit binary-search TI SAR ADC is the most energy efficient as observed in the energy analysis and comparison with other high-speed dynamic SAR based ADC architectures. As well, a process insensitive asynchronous logic is proposed to further reduce the delay of the SA loop. The ADC was fabricated in 65 nm CMOS, occupying 0.104 mm^2 of active area. It achieves 54.6 dB SNDR at 170 MS/s, consuming 2.3 mW of power and with a FoM of 30.8 fJ/conversion-step. At Nyquist input frequency, the SNDR is 53.2 dB with FoM of 36.4 fJ/conversion-step.

Appendix

The following subsections provide the detailed calculations of the binary-search decoder, SAR DAC energy, SAR logic, and flash encoder energies in order to compute the total ADC energy and the architecture curve modeling.

1) Binary-Search ADC Decoder: The decoder design for the binary-search ADC is shown in Fig. 15. The energy per conver-

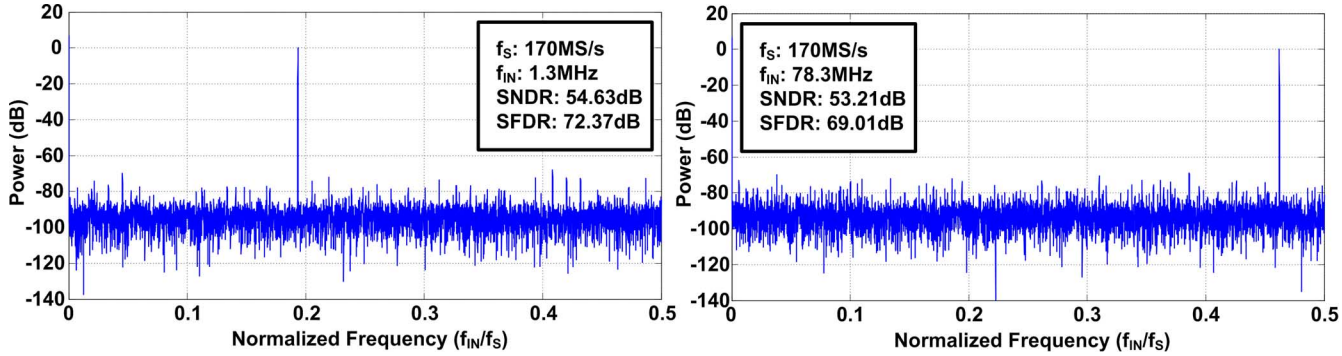


Fig. 14. 16,384 point FFT at 1.31512 MHz and 78.3984 MHz input (decimated by 25).

TABLE I
PERFORMANCE SUMMARY AND BENCHMARK WITH STATE-OF-THE-ART

		CICC'11 [3]	ISSCC'10 [4]	CICC'10 [5]	A-SSCC'11 [6]	VLSI'10 [15]	This work	
Technology		65	90	65	65	90	65	nm
Architecture		Pipeline	Pipeline	Pipelined-SAR	Pipelined-SAR	FL-SAR	BS-TI SAR	
Resolution		12	10	10	10	9	10	bit
Sampling Rate		150	100	204	160	150	170	MS/s
Supply Voltage		1.2	1	1	1.1	1.2	1	V
Input Range		1.5	N/A	N/A	1.1	N/A	1.6	$V_{p\text{-}p}$
SNDR	DC	67	55	55.2	55.4	54.07	54.6	dB
	Nyquist	55	53.9	53.2	52.2	53.4	53.2	
DNL/INL		0.3/1.02	0.81/1	0.74/0.9	0.46/1.7	0.48/0.48	0.52/0.93	LSB
Power		48	4.5	9.15	2.72	1.53	2.3	mW
FoM	DC	194	98	95.4	35	24.7	30.8	fJ/step
	Nyquist	697	111.2	120.5	51.4	26.65	36.4	
Active Area		0.99	0.058	0.22	0.21	0.028	0.104	mm^2

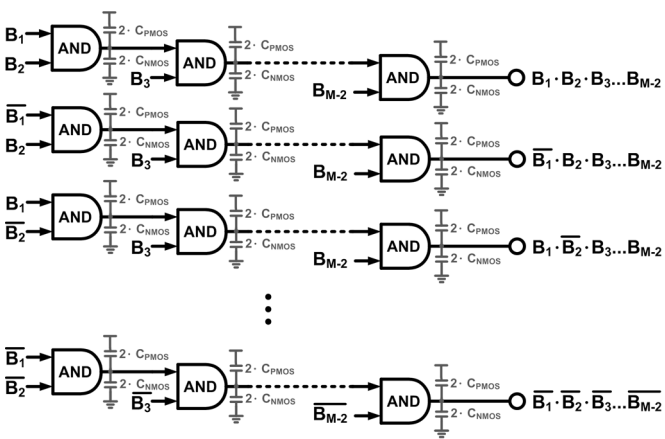


Fig. 15. Mth-bit stage decoder design for binary-search ADC.

sion of the M-bit binary-search ADC decoder can be expressed as follows:

$$E_{\mathrm{BSTI,deco}} = \left[\sum_{\mathrm{i}=4}^{\mathrm{M}} (2^{\mathrm{i}-1}) \cdot (\mathrm{i}-3)\right] \cdot (\mathrm{C_{PMOS}} + \mathrm{C_{NMOS}}) \cdot V_{\mathrm{DD}}^2 \tag{A1}$$

where $\mathrm{C_{PMOS}}$ and $\mathrm{C_{NMOS}}$ are total junction capacitances of the PMOS and NMOS transistors, respectively.

2) SAR DAC Array: Assuming the $(\mathrm{M}+\mathrm{N}-1)$-bit DAC are formed by split M bit MSB and N bit LSB capacitive array, the switching energy of SAR DAC array can be calculated as [11], [26]

$$E_{DAC} \approx \left[\sum_{\mathrm{i}=1}^{\mathrm{M}} (2^{\mathrm{M}+1-2\mathrm{i}}) \cdot (2^{\mathrm{i}}-1) + \sum_{\mathrm{i}=1}^{\mathrm{N}} (2^{\mathrm{N}-\mathrm{M}+1-2\mathrm{i}}) \cdot (2^{\mathrm{i}}-1)\right] \cdot \mathrm{C}_0 \cdot V_{\mathrm{REF}}^2 \tag{A5}$$

where V_{REF} is the reference voltage charging to DAC array.

3) SAR Logic: The implemented SAR control logic is dynamic logic rather than static flip-flop as shown in Fig. 16(a), and Fig. 16(b) shows the asynchronous SA loop. The energy of the SAR control logic with the asynchronous SA loop can be expressed as follows:

$$E_{\mathrm{SA,log\,ic}} = [7 \cdot \mathrm{N} \cdot \mathrm{C_{PMOS}} + \mathrm{N} \cdot (\mathrm{N}+8) \cdot \mathrm{C_{NMOS}}] \cdot V_{\mathrm{DD}}^2. \tag{A6}$$

4) Flash ADC Encoder: Fig. 17 shows the general thermometer-to-binary encoder for M-bit flash ADC. The energy per conversion of the M-bit flash ADC encoder can be expressed as follows:

$$E_{\mathrm{FLTI,enco}} = \left[(\mathrm{M}+8) \cdot 2^{\mathrm{M}-2} - 2\right] \cdot (\mathrm{C_{PMOS}} + \mathrm{C_{NMOS}}) \cdot V_{\mathrm{DD}}^2. \tag{A7}$$

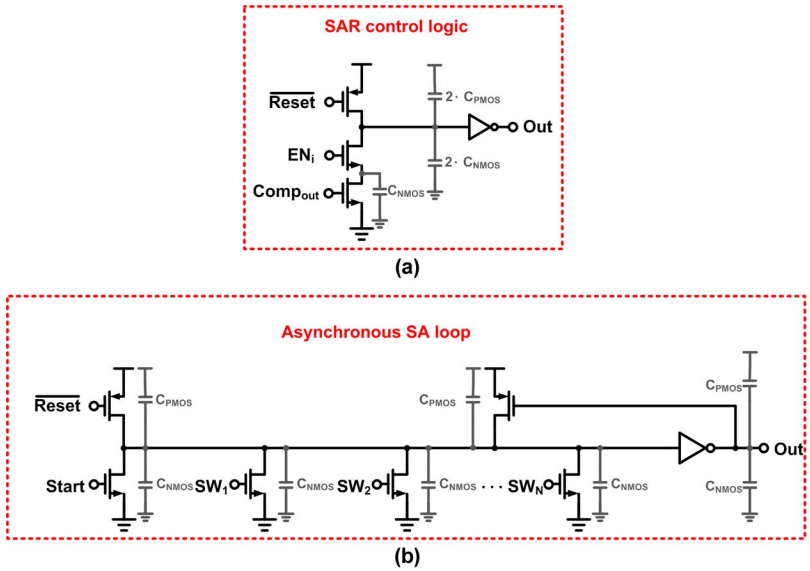


Fig. 16. (a) SAR control logic scheme. (b) Asynchronous SAR loop scheme.

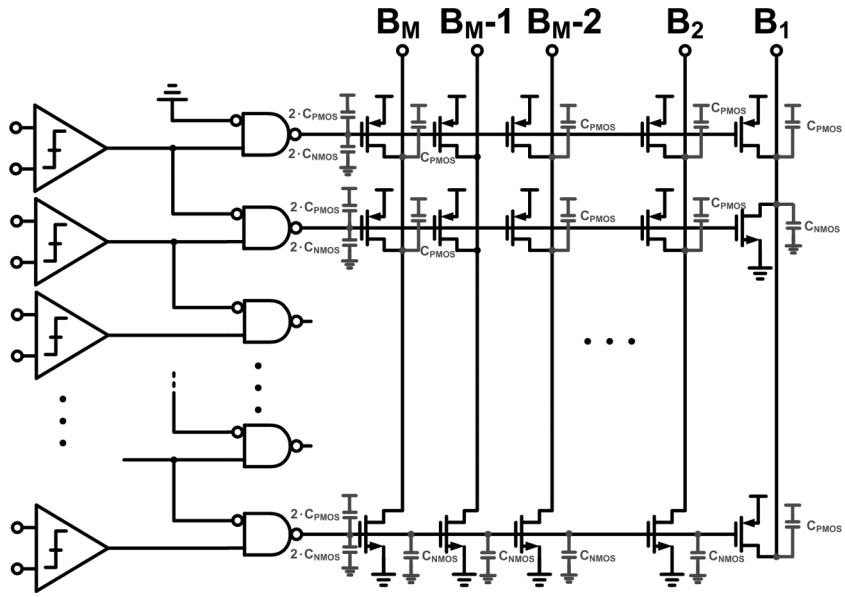


Fig. 17. M-bit flash ADC encoder.

5) SAR Logic for Dual-Channel TI SAR: By using the same SA control logic and loop shown in Fig. 16, the energy of the control logic and SA loop for $(\mathrm{M}+\mathrm{N}-1)$-bit dual-channel TI SAR can be calculated as:

$$E_{\mathrm{TISA,log\,ic}} = [5\cdot(\mathrm{M}+\mathrm{N}-1)\cdot \mathrm{C_{PMOS}} + (\mathrm{M}+\mathrm{N}-1) \cdot(\mathrm{M}+\mathrm{N}+5)\cdot \mathrm{C_{NMOS}}]\cdot V_{\mathrm{DD}}^2. \quad \text{(A8)}$$

ACKNOWLEDGMENT

The authors would also like to express their sincere appreciation to C.-H. Chan for suggestions, and H. Venkatesan for language editing and proofreading.

REFERENCES

[1] K. Honda, M. Furuta, and S. Kawahito, "A low-power low-voltage 10-bit 100-MSample/s pipeline A/D converter using capacitance coupling techniques," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 757–765, Apr. 2007.

[2] B. Murmann and B. Boser, "A 12b 75 MS/s pipelined ADC using open loop residue amplification," in *IEEE ISSCC Dig. Tech. Papers*, 2003, pp. 328–329.

[3] B. Peng, G.-Z. Huang, H. Li, P.-Y. Wan, and P.-F. Lin, "A 48-mW, 12-bit, 150-MS/s pipelined ADC with digital calibration in 65 nm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2011, pp. 1–4.

[4] Y. C. Huang and T. C. Lee, "A 10b 100 MS/s 4.5 mW pipelined ADC with a time sharing technique," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 300–301.

[5] Y. D. Jeon, Y. K. Cho, J. W. Nam, K. D. Kim, W. Y. Lee, K. T. Hong, and J. K. Kwon, "A 9.15 mW 0.22 mm^2 10b 204 MS/s pipelined SAR ADC in 65 nm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2010, pp. 1–4.

[6] Y. Zhu, C. H. Chan, S. W. Sin, S. P. U, and R. P. Martins, "A 35 fJ 10b 160 MS/s pipelined-SAR ADC with decoupled flip-around MDAC and self-embedded offset cancellation," in *Proc. 2011 IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2011, pp. 61–64.

[7] R. Wang, U. F. Chio, S. W. Sin, S. P. U, Z.-H. Wang, and R. P. Martins, "A 12-bit 110 MS/s 4-stage single-opamp pipelined SAR ADC with ratio-based GEC technique," in *Proc. ESSCIRC*, 2012, pp. 256–278.

[8] S. W. Sin, L. Ding, Y. Zhu, H. G. Wei, C. H. Chan, U. F. Chio, S. P. U, R. P. Martins, and F. Maloberti, "An 11b 60 MS/s 2.1 mW two-step time-interleaved SAR-ADC with reused S&H," in *Proc. ESSCIRC*, 2010, pp. 218–221.

[9] W. Liu, P.-L. Huang, and Y. Chiu, "A 12b 22.5/45 MS/s 3.0 mW 0.059 mm^2 CMOS SAR ADC achieving over 90 dB SFDR," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 380–381.

[10] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 μm CMOS process," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2009, pp. 236–237.

[11] Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, R. P. Martins, and F. Maloberti, "A 10-bit 100 MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[12] C. C. Liu, S. J. Chang, G. Y. Huang, Y. Z. Lin, C. M. Huang, C. H. Huang, L.-K. Bu, and C. C. Tsai, "A 10b 100 MS/s 1.13 mW SAR ADC with binary scaled error compensation," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 368–369.

[13] I. Akita, M. Furuta, J. Matsuno, and T. Itakura, "A 7-bit 1.5-GS/s time interleaved SAR ADC with dynamic track-and-hold amplifier," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2011, pp. 293–296.

[14] K. Doris, E. Janssen, C. Nani, A. Zanikopoulos, and G. van der Weide, "A 480 mW 2.6 GS/s 10b time-interleaved ADC with 48.5 dB SNDR up to Nyquist in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2821–2833, Dec. 2011.

[15] Y. Z. Lin, C. C. Liu, G. Y. Huang, Y. T. Shyu, and S. J. Chang, "A 9-bit 150-MS/s 1.53-mW subranged SAR ADC in 90-nm CMOS," in *IEEE Symp. VLSI Circuits Dig.*, 2010, pp. 243–244.

[16] U. F. Chio, H. G. Wei, Y. Zhu, S. W. Sin, S. P. U, R. P. Martin, and F. Maloberti, "Design and experimental verification of a power effective Flash-SAR subranging ADC," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 57, no. 8, pp. 607–611, Aug. 2010.

[17] G. Van der Plas and B. Verbruggen, "A 150 MS/s 133 μW 7 bit ADC in 90 m digital CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2631–2640, Dec. 2008.

[18] Y. Z. Lin, S. J. Chang, Y. T. Liu, C. C. Liu, and G. Y. Huang, "A 5b 800 MS/s 2 mW asynchronous binary-search ADC in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 80–81.

[19] S. S. Wong, U. F. Chio, C. H. Chan, H. L. Choi, S. W. Sin, S. P. U, and R. P. Martins, "A 4.8-bit ENOB 5-bit 500 MS/s binary-search ADC with minimized number of comparators," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2011, pp. 73–76.

[20] J. Yang, T. L. Naing, and R. W. Brodersen, "A 1 GS/s 6 bit 6.7 mW successive approximation ADC using asynchronous processing," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1469–1478, Aug. 2010.

[21] C. H. Chan, Y. Zhu, U. F. Chio, S. W. Sin, S. P. U, and R. P. Martins, "A voltage-controlled capacitance offset calibration technique for high resolution dynamic comparator," in *Proc. 2009 Int. SoC Design Conf. (ISOCC)*, Nov. 2009, pp. 392–395.

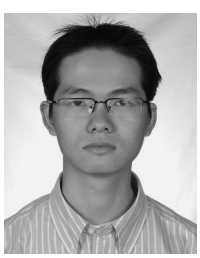
[22] A. Matsuzawa, "Energy efficient ADC design with low voltage operation," in *Proc. 2011 Int. Conf. (ASICON)*, Oct. 2011, pp. 508–511.

[23] H. J. Jeon, Y. B. Kim, and M. Choi, "Offset voltage analysis of dynamic latched comparator," in *Proc. 54th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2011, pp. 1–4.

[24] M. Gustavsson, *CMOS Data Converters for Communications*. Dordrecht, The Netherlands: Kluwer, 2000, ch. 3, sec. 3.9, pp. 75–77.

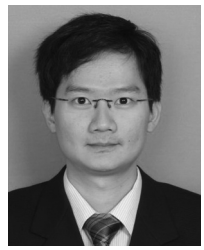
[25] S. W. Sin, S. P. U, and R. P. Martins, "A generalized timing-skewfree, multi-phase clock generation platform for parallel sampled-data systems," in *Proc. IEEE ISCAS*, 2004, vol. 1, pp. I-369–I-372.

[26] D. Zhang, C. Svensson, and A. Alvandpour, "Power consumption bounds for SAR ADCs," in *Proc. 20th Eur. Conf. Circuit Theory and Design (ECCTD)*, Aug. 2011, pp. 556–559.



Si-Seng Wong received the B.S. (Hons.) degree from the University of Texas at Austin, Austin, TX, USA, in 2008, and the M.S. degree from the University of Macau, Macao, China, in 2011.

He is currently an analog design engineer with Synopsys Macau Ltd. His research interest is high-speed, medium-resolution, and low-power Nyquist A/D converters design.



U-Fat Chio (M'09) received the B.Sc. degree in electrical engineering and the M.Sc. degree in communications engineering from the National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2002 and 2004, respectively, and the Ph.D. degree from the University of Macau, Macao, China, in 2012.

From 2004 to 2005, he was with DenMOS Technology, Inc., Hsinchu, Taiwan. He is currently a Postdoctoral Fellow with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. His research interest is high-speed analog-to-digital converters and power management circuit designs.

Yan Zhu (S'10–M'13) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macao, China, in 2009 and 2011, respectively.

She is now a Postdoctoral Researcher with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. Her research interests include low-power and wideband high-speed Nyquist A/D converters, as well as digitally assisted data converter designs.

Sai-Weng Sin (S'98–M'06–SM'13) received the B.Sc., M.Sc., and Ph.D. degrees with the highest honor in electrical and electronics engineering from University of Macau, Macao, China, in 2001, 2003, and 2008 respectively.

He is currently an Assistant Professor in the Faculty of Science and Technology, University of Macau, and is the Coordinator of the Data Conversion and Signal Processing (DCSP) Research Line in State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. He has published one book entitled *Generalized Low-Voltage Circuit Techniques for Very High-Speed Time-Interleaved Analog-to-Digital Converters* (Springer, 2010), holds four U.S. patents, and has over 80 technical journals and conference papers in the field of high-performance data converters and analog mixed-signal integrated circuits.

Dr. Sin has been a member of Technical Program Committee of IEEE Sensors 2011 and IEEE RFIT 2011–2012 Conference, Review Committee Member of PrimeAsia 2009 Conference, Technical Program and Organization Committee of the 2004 IEEJ AVLSI Workshop, and the Special Session co-Chair and Technical Program Committee Member of 2008 IEEE APCCAS Conference. He is currently Secretary of IEEE Solid-State Circuit Society (SSCS) Macau Chapter (with 2012 IEEE SSCS World Chapter of the Year Award) and IEEE Macau CAS/COM Joint Chapter. He was a corecipient of the 2011 ISSCC Silk Road Award, the Student Design Contest winner in A-SSCC 2011, and the recipient of the 2011 State Science and Technology Progress Award (second-class), China.

Seng-Pan (Ben) U (S'94–M'00–SM'05) received the B.Sc. and M.Sc degrees in 1991 and 1997, respectively, and the joint Ph.D. degree with highest honor in the field of high-speed analog IC design from the University of Macau (UM) and the Instituto Superior Técnico, Universidade Técnica de Lisboa (IST/UTL), in 2002.

He has been with the Department of Electrical and Electronic Engineering, Faculty of Science and Technology (FST), UM, since 1994, where he is currently Professor and Deputy Director of State Key Laboratory of Analog and Mixed-Signal VLSI. From 1999 to 2001, he was also on leave to the Integrated CAS Group, Center of Microsystems, IST/UTL, as a Visiting Research Fellow. In 2001, he cofounded and was Engineering Director of the Chipidea Microelectronics (Macau) Ltd., and, since 2003, has been the corporate VP-IP Operations Asia-Pacific and site General Manager of the company for advanced analog and mixed-signal semiconductor IP (SIP) product devel-

opment. The company was acquired in 2009 by the world leading EDA and IP provider Synopsys, Inc. (NASDAQ: SNPS), currently as Synopsys Macau Ltd. He is also the corporate Senior Analog Design Manager and Site General Manager. He coholds seven U.S. patents and has coauthored four books in Springer and China Science Press in the area of VHF SC filters, analog baseband for multistandard wireless transceivers and very high-speed TI ADCs.

Dr. U is currently the Industrial Relationship Officer of IEEE Macau Section and the Chairman for the IEEE SSC and CAS/COMM Macau chapter. He has been on the technical review committees of various international scientific journals and conferences for many years, including IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEICE, and ISCAS. He was the chairman of the local organization committee of IEEJ AVLSIWS'04, the Technical Program co-Chair of IEEE APCCAS'08, ICICS'09, and PRIMEAsia'11. He is currently a Technical Program Committee of RFIT, VLSI-DAT, and A-SSCC, and an Editorial Board member of *Journal of Analog Integrated Circuits and Signal Processing*. He was the founding Chairman of IEEE SSC Macau Chapter. He received The 2012 Best SSC Chapter Award in ISSCC'13. He received both the 2012 Macau Science and Technology Invention and Progress Award. Both at the first time from Macau, he received the Scientific and Technological Innovation Award of Ho Leung Ho Lee Foundation in 2010, and also The State Scientific and Technological Progress Award in 2011. In recognition of his contribution in high-technology research and industrial development in Macau, he was awarded by Macau SAR government the Honorary Title of Value in 2010. He received various scholarships and R&D grants and published more than 120 scientific papers in IEEE/IET journal and conferences. He received over 20 research and academic/teaching awards and is also the advisor for over 20 international student paper award recipients, e.g., ISSCC Silk Road Award, IEEE DAC/ISSCC Student Design Contest, A-SSCC Student Design Contest, ISCAS, MWSCAS, and PRIME.

Rui Paulo Martins (M'88–SM'99–F'08) was born on April 30, 1957. He received the Bachelor (five-years), Master, and Ph.D. degrees, as well as the *Habilitation* for Full Professor in electrical engineering and computers, from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering (DECE)/IST, TU of Lisbon, since October 1980. Since 1992, he has been on leave from IST, TU of Lisbon, and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Full Professor since 1998. In FST, he was the Dean of the Faculty from 1994 to 1997, and has been Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment as Vice-Rector (Research) until August 31, 2013. Within the scope of his teaching and research activities he has taught 21 Bachelor and Master courses and supervised or cosupervised 26 theses (11 Ph.D. dissertations and 15 Masters theses). He has published 12 books, of which he coauthored five and coedited seven, and five book chapters; 261 refereed papers in scientific journals (59) and conference proceedings (202); as well as other 70 academic works, in a total of 343 publications. He has coauthored four U.S. patents (one issued in 2009, two in 2011, and one in 2012) and has four others U.S. patents pending. He created the Analog and Mixed-Signal VLSI Research Laboratory of UM (http://www.fst.umac.mo/en/lab/ans_vlsi/website/index.html), elevated in January 2011 to State Key Lab of China (the first in Engineering in Macao), and is its Founding Director.

Prof. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005, and of the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 "World Chapter of the Year" of the IEEE Circuits And Systems Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on Circuits And Systems—APCCAS'2008, and was the Vice-President for the Region 10 (Asia, Australia, the Pacific) of the IEEE Circuits And Systems Society (CASS), for 2009–2011. He is now the Vice-President (World) Regional Activities and Membership of the IEEE CAS Society for 2012–2013. He is an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS for 2010–2013. He is also a member of the IEEE CASS Fellow Evaluation Committee (Class of 2013). He was the recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010 he was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.