Cascade Switched-Capacitor IIR Decimating Filters

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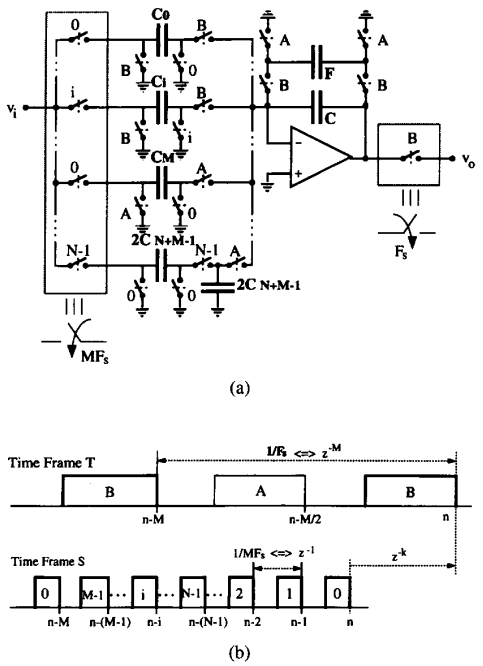
***Abstract*—Comprehensive methodologies are described for the design of infinite impulse response switched-capacitor (SC) decimating filters employing either externally cascaded or internally cascaded structures. The former are more appropriate to achieve high decimating factors but suffer from the effects of unwanted aliasing frequency components associated with the intermediate sampling frequencies. The latter overcome this problem but become more complex to design to attain high decimating factors. Such decimating filters allow not only to relax the requirements of continuous-time pre-filters in the context of traditional SC filter systems but also to realize arbitrary baseband and anti-aliasing amplitude responses employing operational amplifiers with more relaxed speed requirements than their traditional SC filters counterparts. Examples are given to illustrate the proposed methodologies.**

I. Introduction

SWITCHED-CAPACITOR (SC) decimating filters are specialized networks that implement, together with an appropriate filtering function, the alteration of the sampling frequency from a high value MF_s at the input to a lower value F_s at the output [1]. Whereas finite impulse response (FIR) SC decimators can be realized with few operational amplifiers (OA's) but are practically useful only for multinotch stopband responses [2], [3], infinite impulse response (IIR) SC decimators are particularly suitable for realizing wideband high selectivity filtering applications.

Two basic building blocks combining high-speed polyphase SC networks together with slower recursive SC networks have been previously proposed for realizing first- and second-order IIR SC decimating filters. From their schematic representations, respectively indicated in Figs. 1 and 2, we observe that although the input signal is sampled at a frequency M-fold higher than the output sampling frequency, the time determined by switching waveforms A and B for the settling of the amplifiers is similar to that in traditional bi-phase SC filters with sampling frequency F_s. In comparison with such SC filters, the decimating building blocks not only efficiently increase the time for the amplifiers to settle, and thus saving power, but also reduce the capacitance spread and total capacitor area, and thus saving silicon area as well [4], [5]. Higher-order IIR SC decimating filters can be designed by cascading an FIR decimator, for sampling rate reduction from MF_s to F_s, together with an IIR filter operating at the lower output sampling rate F_s. Although attractive for digital implementations [6], such multistage methodology may not be amenable for the SC implementation [7] for reasons of circuit efficiency.



(a)

(b)

Fig. 1. (a) Schematic diagram and (b) switching waveforms of a first-order SC decimator building block combining a polyphase structure, for high-frequency input sampling, together with a damped integrator operating at a lower switching frequency.

In this paper we propose two novel methodologies for designing multistage IIR SC decimating filters. One such methodology consists of *externally* cascading a number of first- and second-order IIR SC decimating sections to meet the desired amplitude response requirements, and whose sampling frequencies are gradually reduced from MF_s to F_s. The resulting SC decimating filters are particularly suitable to achieve high decimating factors M but suffer from the problem of additional unwanted aliasing frequency components associated with the intermediate sampling frequencies of the cascade sections. To overcome such limitation we also consider an alternative methodology that consists of *internally* cascading first- and second-order IIR SC decimating sections, all sampling the input signal at the same higher sampling frequency MF_s, which

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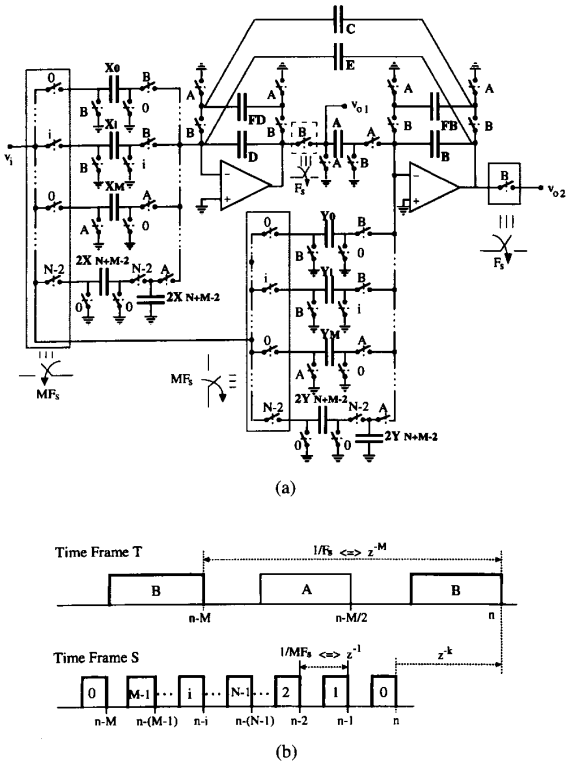

Fig. 2. (a) Schematic diagram and (b) switching waveforms of a second-order SC decimator building block combining two polyphase networks, for input high-frequency sampling, together with a two-integrator loop operating at a lower sampling frequency.

allow the realization of arbitrary baseband and anti-aliasing amplitude responses employing even simpler OA's than their externally cascade counterparts. Such SC decimating filters are, however, more complex to design and therefore their practicality may be restricted to moderate decimating factors M.

After this introduction, the paper comprises three additional sections. Section II discusses the systematic methodology for designing Nth-order SC decimating filters using *externally cascaded* first- and second-order building blocks, and which is illustrated considering a 14th-order SC decimator with a very large decimating factor $M = 120$. A sensitivity analysis is carried out to demonstrate the behavior of the proposed circuit solution under some relevant non-ideal characteristics of the constituting components. Then, in Section III, we consider the alternative design of Nth-order SC decimating filters using *internally cascaded* first- and second-order building blocks. Simple design rules are established to determine the most efficient topology that should be adopted for high-frequency applications and yielding acceptable values of the capacitance spread and total capacitor area in the circuit as well as an adequate performance under nonideal characteristics of the amplifiers. This is illustrated considering the design of a fifth-order SC decimator, with $M = 3$, adequate for video communication front-ends. Section IV draws the conclusions of the paper.

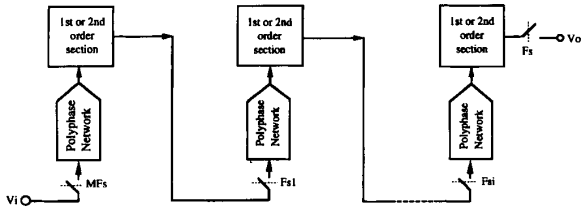

Fig. 3. Block diagram of an externally cascaded SC decimating filter.

II. Externally Cascaded Nth-Order SC Decimators

A. General Design Methodology

The first step in the design of a multistage IIR SC decimating filter employing externally cascaded building blocks consists of obtaining the overall z-transfer function of the corresponding prototype filter that meets the specified baseband and anti-aliasing filtering characteristics. For implementation using a cascade of D second-order building blocks this is initially expressed as

$$H(z) = k \prod_{i=1}^{D} \frac{(1 - 2r_{o_i}\cos(\theta_{o_i}z^{-1} + r_{o_i}^2 z^{-2})}{(1 - 2r_{p_i}\cos(\theta_{p_i})z^{-1} + r_{p_i}^2 z^{-2})} \quad (1)$$

where the unit delay period is referred to the input sampling frequency MF_s of the decimator. The above z-transfer function can not be directly implemented since this would lead to traditional SC filter building blocks operating at the high sampling rate MF_s. Instead, the proposed design methodology assigns appropriate decimating factors to the constituting IIR SC decimator building blocks in order to gradually decrease the sampling frequency and thus achieving the corresponding benefits of more relaxed speed requirements for the amplifiers as well as lower capacitance spreads. This is illustrated in the schematic diagram shown in Fig. 3. The z-transfer function of such externally cascaded SC decimating filter with multiple sampling frequencies can be written in the form

$$H(z) = k \prod_{i=1}^{D} \frac{(1 - 2r_{o_i}\cos(\theta_{o_i}z^{-T_i} + r_{o_i}^2 z^{-2T_i})}{(1 - 2r_{p_i}\cos(\theta_{p_i})z^{-T_i} + r_{p_i}^2 z^{-2T_i})} \quad (2)$$

where i gives the sequence of the decimator stages from the input $i = 1$ to the output $i = D$. If we designate the input sampling frequency of each SC decimator stage as F_i, then the normalized delay periods T_i appearing in the corresponding z-transfer functions are determined by

$$T_i = M(F_s/F_i) = \prod_{j=1}^{i} M_j, \quad (3)$$

where, for a given overall decimation factor M of the multistage structure, M_j represent the factors of sampling rate reduction of the decimator stages from $j = 1$ to $j = i$. The modified poles and zeroes from the original z-transfer functions are obtained using well-known properties of discrete-time transfer functions [8].

B. Strategy for Decimation and Pole-Zero Pairing

The selection of a particular sequence for decimation is determined in conjunction with the assignment of poles and zeroes to each SC decimator building block and by taking into account the corresponding frequency-translated aliasing responses. This makes it possible not only to obtain the desired baseband specifications, as in traditional cascade filter design methods, but also the specified anti-aliasing filtering response. The optimum sequence of decimation and corresponding pole-zero pairing are obtained according to the following design criteria:

1) Decompose M in prime factors by descending order, in order to minimize the speed requirements of the amplifiers.
2) Associate the larger values of the pole and zero frequencies to the lower values of T_i, i.e., minimize F_{si}/F_{pi} and F_{si}/F_{oi}, in order to minimize capacitance spread and total capacitor area.
3) Implement first lowpass decimator stages with low selectivity poles, i.e., low Q_p, and wide transition bands in order to reject the alias frequency components at higher frequency, and also to increase the attenuation of the input high frequency noise.
4) Implement high selectivity lowpass decimator stages, as well as bandpass decimator stages, at the heart of the cascade structure in order to increase the attenuation of those aliasing frequency components closer to the passband, and also to maximize the dynamic range of the overall decimator.
5) Implement all highpass decimator stages at the end of the cascade structure, since they only contribute to the definition of the lower stopband of the baseband response.

Once the appropriate sequence of decimation and pole-zero pairing has been determined, such that resulting amplitude response meets the target specifications both in the baseband and in the aliasing band, we carry-out single stage optimization in order to improve signal handling capability and minimize capacitance spread.

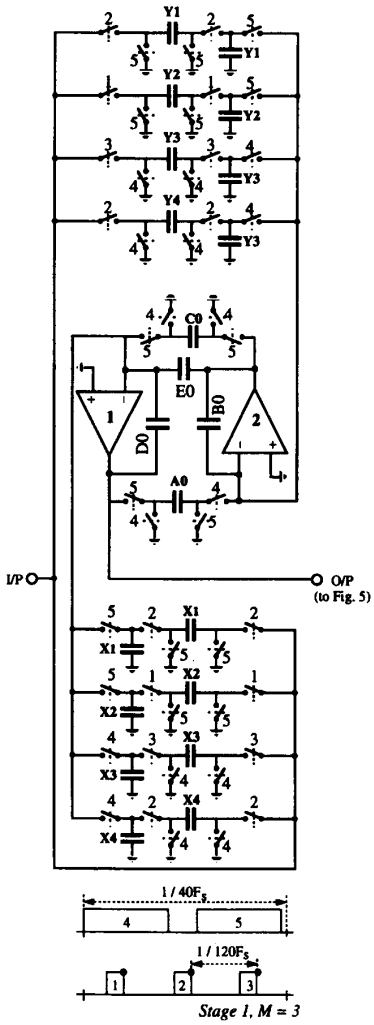

Fig. 4. Schematic diagram and switching waveforms of the front-end SC decimating stage in the externally cascaded bandpass SC decimating filter for telephone channel data communications.

C. Example: Externally Cascaded Bandpass SC Decimating Filter

For illustration, we consider the design of an IIR SC bandpass decimator that meets the front-end filtering requirements in telephone channel data communication. A high selectivity 14th-order SC bandpass decimator with $MF_s = 1.152$ MHz input sampling frequency and a decimating factor of $M = 120$ is designed to meet the baseband specifications together with a minimum 60 dB rejection of the aliasing frequency components up to $120Fs/2$. Because of the very high oversampling ratio with respect to the maximum passband frequency of 3.4 kHz of the telephone channel only a simple first-order RC section would be needed in front of this decimator, thus significantly reducing the corresponding silicon overhead for integrated circuit implementation. Despite such high input sampling, the decimator is designed to allow comfortable settling times for the amplifiers and thus also saving power.

By employing a computer aided filter synthesis procedure we first obtain the bilinear discrete-time coefficients for the 14th-order bandpass decimator prototype filter. Following the methodology described above we then obtain an externally cascaded SC decimating filter comprising, from the input to the output, two second-order lowpass SC decimating filter sections, the first with $M = 3$ and the second with $M = 5$, two second-order lowpass-notch SC decimating filter sections with $M = 2$, one second-order bandpass SC decimating filter section also with $M = 2$, and finally two second-order highpass-notch SC filter sections with $M = 1$. For clarity of the illustration, we represent in Fig. 4 the schematic diagram and switching waveforms of the front-end second-order lowpass decimating filter section with $M = 3$, whereas

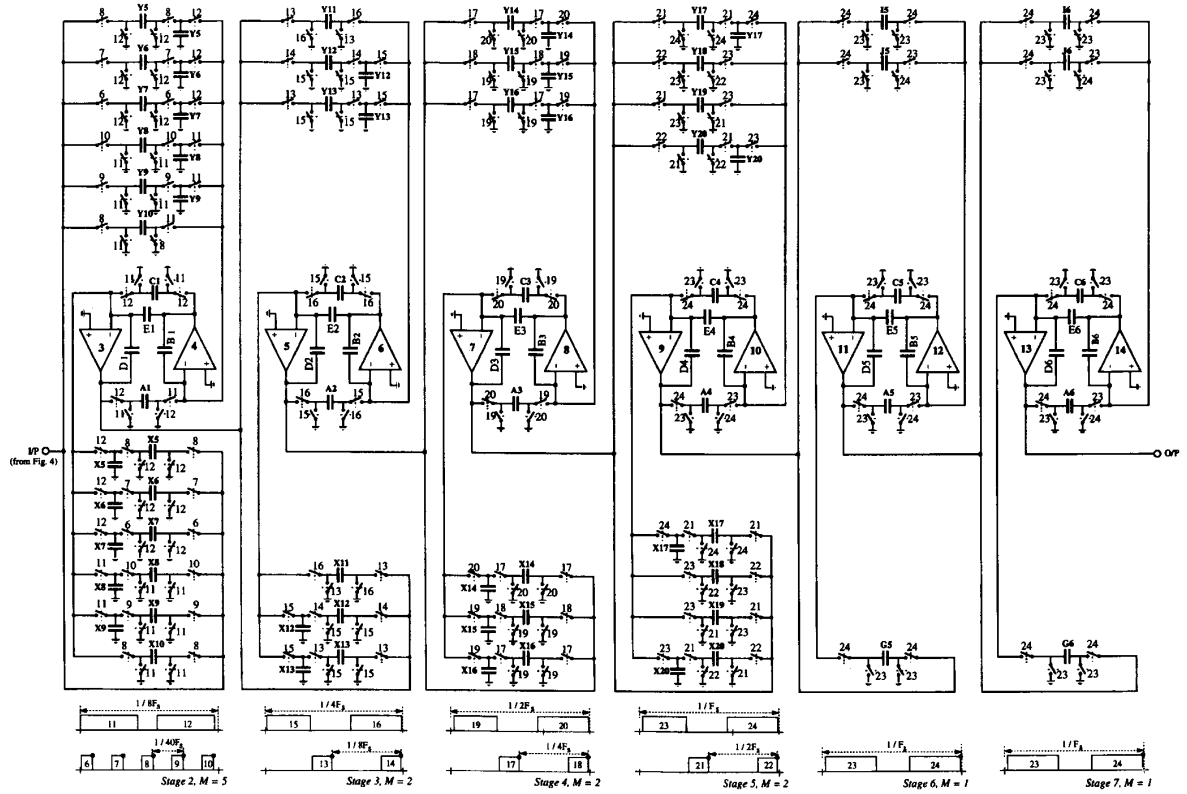

Fig. 5. Schematic diagram and switching waveforms of the externally cascaded bandpass SC decimating filter for telephone channel data communication.

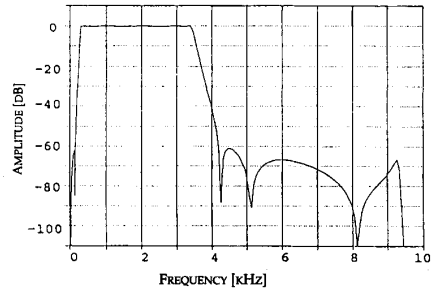

Fig. 6. Nominal computer simulated baseband amplitude response of the bandpass SC decimating filter of Fig. 5.

the schematic diagrams and associated switching waveforms of all the remaining decimating filter sections giving an overall decimation factor of $M = 40$ are represented in Fig. 5. After scaling for maximum signal handling capability we obtain the normalized capacitance values indicated in Table I.

D. Nominal Behavior and Sensitivity Analysis

Since the front-end second-order SC lowpass decimator shown in Fig. 4 has been already demonstrated and experimentally characterized in integrated circuit form [5] we shall present herein the results of the study carried by computer simulations for the multistage SC bandpass decimator represented in Fig. 5, with $M = 40$. In Fig. 6 we can observe the nominal amplitude response obtained from dc to F_s. A detailed computer-based evaluation was also carried out to evaluate the behavior of the multistage SC bandpass decimator under typical non-ideal values of the amplifiers dc gain (of the order of 60 and 80 dB) and matching accuracy of the capacitance ratios (of the order of $\pm 0.1\%$). In the baseband, this is basically identical to the behavior of the more traditional SC filter networks under similar conditions as we can observe from the illustrative results given in Fig. 7 for the case when the SC decimating filter operates with finite dc gain amplifiers. Above the baseband this type of SC decimating filters are known to be more affected than traditional SC filters by such nonideal operating conditions, because of the pole-zero cancellation mechanisms that produce the attenuation of the unwanted aliasing frequency components up to $MF_s/2$ [4]. This is illustrated by the computer simulation results presented in Fig. 8 and which show how the finite dc gain of the amplifiers affects the responses obtained in the aliasing bands around 38.4, 76.8, and 153.6 kHz. Despite the higher sensitivity that is observed in such frequency bands we notice that the worst case attenuation ($\approx$ 55 dB around 153.6 kHz) is still close to the required minimum of 60 dB, and this would be further increased when combined with the additional attenuation provided by the front-end lowpass SC decimator of Fig. 4.

TABLE I
NORMALIZED CAPACITANCE VALUES OF THE SC DECIMATING CIRCUITS IN FIGS. 4 AND 5

OA1	$X_1 = 1.16$	$X_2 = 2.22$	$X_3 = 2.10$	$X_4 = 1.00$	$C_0 = 3.35$	$D_0 = 10.11$	$E_0 = 18.31$		
OA2	$Y_1 = 1.04$	$Y_2 = 2.04$	$Y_3 = 2.04$	$Y_4 = 1.00$	$A_0 = 3.07$	$B_0 = 18.82$			
OA3	$X_5 = 3.33$	$X_6 = 1.04$	$X_7 = 1.03$	$X_8 = 1.01$	$X_9 = 1.00$	$X_{10} = 1.07$	$C_1 = 3.09$	$D_1 = 29.5$	$E_1 = 47.4$
OA4	$Y_5 = 3.17$	$Y_6 = 1.00$	$Y_7 = 1.00$	$Y_8 = 1.00$	$Y_9 = 1.00$	$Y_{10} = 1.08$	$A_1 = 2.62$	$B_1 = 48.0$	
OA5	$X_{11} = 1.00$	$X_{12} = 1.39$	$X_{13} = 3.81$	$C_2 = 2.15$	$D_2 = 4.71$	$E_2 = 1.09$			
OA6	$Y_{11} = 2.40$	$Y_{12} = 1.00$	$Y_{13} = 3.63$	$A_2 = 1.64$	$B_2 = 3.20$				
OA7	$X_{14} = 3.15$	$X_{15} = 3.79$	$X_{16} = 9.07$	$C_3 = 16.01$	$D_3 = 14.44$	$E_3 = 1.00$			
OA8	$Y_{14} = 2.92$	$Y_{15} = 1.60$	$Y_{16} = 1.00$	$A_3 = 3.98$	$B_3 = 4.04$				
OA9	$X_{17} = 4.05$	$X_{18} = 1.00$	$X_{19} = 1.25$	$X_{20} = 4.95$	$C_4 = 3.24$	$D_4 = 2.76$	$E_4 = 1.7$		
OA10	$Y_{17} = 11.4$	$Y_{18} = 1.65$	$Y_{19} = 1.00$	$Y_{20} = 6.08$	$A_4 = 6.04$	$B_4 = 6.08$			
OA11	$G_5 = 4.15$	$C_5 = 1.06$	$D_5 = 5.48$	$E_5 = 1.00$					
OA12	$I_5 = 21.13$	$J_5 = 21.12$	$A_5 = 1.00$	$B_5 = 5.40$					
OA13	$G_6 = 2.06$	$C_6 = 1.00$	$D_6 = 3.77$	$E_6 = 2.52$					
OA14	$I_6 = 8.52$	$J_6 = 8.34$	$A_6 = 1.00$	$B_6 = 4.36$					

TABLE II
COMPARISON OF THREE ALTERNATIVE DESIGN METHODOLOGIES FOR DESIGNING THE 12TH-ORDER SC BANDPASS DECIMATING FILTER WITH $M = 40$

SOLUTION	SAMPLING	CASCADING METHODOLOGY	BUILDING BLOCKS	MAX. C-SPREAD	TOTAL C-AREA	SWITCHING WAVEFORMS	AMPLIFIERS CLOCKING FREQUENCY
Traditional	Uniform at 40 F_S	Simple pole-zero pairing strategy	Simple biquads	≈ 800	≈ 5,000	2	All amplifiers clocked @ 384 kHz
Semi-traditional	Gradually lower from 40 F_S to F_S	Elaborate pole-zero-period pairing strategy	Simple biquads	≈ 500	≈ 1,200	10	2 OAs @ 384 kHz 2 OAs @ 76.8 kHz 2 OAs @ 38.4 kHz 2 OAs @ 19.2 kHz 4 OAs @ 9.6 kHz
Multistage Decimation in this paper	Gradually lower from 40 F_S to F_S	Elaborate pole-zero-period pairing strategy	Decimation building blocks	≈ 48	≈ 530	19	2 OAs @ 76.8 kHz 2 OAs @ 38.4 kHz 2 OAs @ 19.2 kHz 6 OAs @ 9.6 kHz

E. Comparison with Alternative Solutions

For completeness, we have briefly evaluated the maximum capacitance spread, total capacitor area and amplifier settling requirements that would have resulted from two alternative, more traditional solutions for designing an SC bandpass decimator meeting similar specifications as above. The conclusions of this study are briefly summarized in Table II.[1] The most traditional solution employing a cascade of classical SC biquadratic sections with uniform sampling rate of 40 F_s followed by a mere output sampling switch at F_s, is the simplest to design but leads to an unacceptably high value of the capacitance spread (above 800) and a correspondingly unrealistic capacitor area of more than 5000 capacitor units. An alternative solution is also based on the cascade of classical SC biquadratic sections but which are now operating with gradually lower sampling frequencies, from the high value of 40 F_s to the desired lower output sampling frequency of only F_s. The pole-zero-period pairing strategy required in this solution is similar to the one previously described, and hence significantly more elaborated than what is needed for the most traditional solution, but the required SC biquads are simpler to design than the SC decimating sections employed above. The resulting capacitor spread and total capacitor area for this solution, respectively of the order of 500 and 1200, are both still too high for practical integrated circuit implementation. Overall, and despite the more elaborate design procedure and larger number of switching waveforms, the proposed design methodology is clearly superior not only in terms of the resulting maximum capacitance spread and total capacitor area but also in terms of the required speed of the amplifiers.

[1]This comparison is made with respect to the 12th-order SC bandpass decimating filter, with $M = 40$, that is schematically represented in Fig. 5.

III. INTERNALLY CASCADED NTH-ORDER SC DECIMATORS

A. Architecture

In order to overcome the problem discussed above of incomplete cancellation of the unwanted aliasing frequency components associated with intermediate sampling frequencies

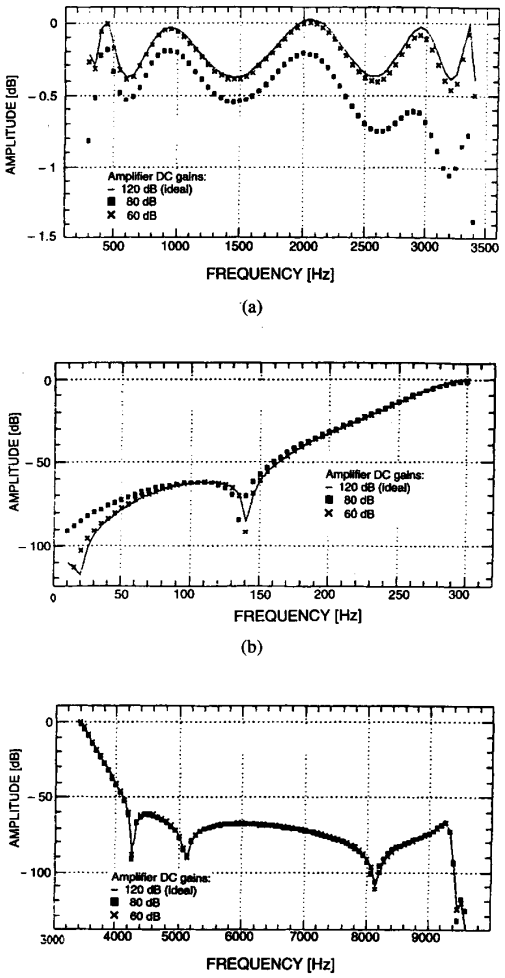

Fig. 7. Computer simulated amplitude responses of the bandpass SC decimating filter with finite dc gain amplifiers. (a) Passband. (b) Lower stopband. (c) Upper stopband.

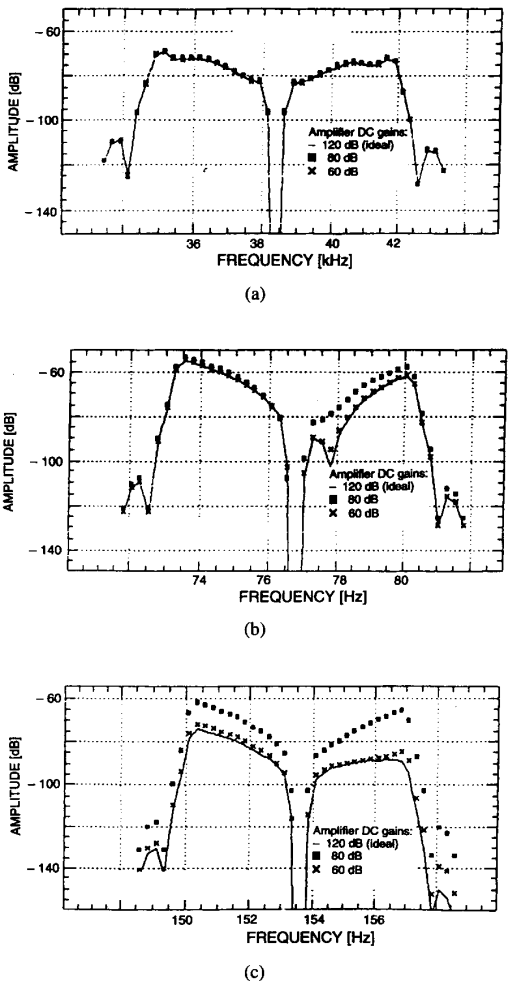

Fig. 8. Computer simulated amplitude responses around the aliased frequency bands at (a) 38.4 kHz, (b) 76.8 kHz, and (c) 153.6 kHz when the bandpass SC decimating filter operates with finite dc gain amplifiers.

between MF_s and F_s, we considered the alternative SC decimating architecture schematically illustrated in Fig. 9 where only the high input sampling frequency MF_s and the lower output sampling frequency F_s are employed. This comprises a varying number of *internally* cascaded first- and second-order SC decimating blocks operating at the lower sampling frequency together with the associated polyphase networks for high frequency input sampling. In such an architecture the SC decimating blocks have two inputs and one output. Input terminal 1 corresponds to the polyphase network connected to the input signal whereas input terminal 2 corresponds to a simple SC coupling branch connected to output of the amplifier in the preceding decimating block (excepting the first block). The overall recursive network is responsible for the implementation of the denominator polynomial function and can realize an arbitrary combination of real and complex conjugate poles according to the required filtering specifications. The polyphase networks are, in turn, responsible for the implementation of the numerator polynomial function and their complexity is related not only to the specified filtering requirements but also to the decimation factor M.

B. Derivation of the z-transfer Functions

The z-transfer function $H(z)$ of the Nth-order decimator can be described by (4) at the bottom of the next page, where the unit delay period corresponds to the sampling period $1/MF_s$ at the input of the decimator. The numerator polynomial function can have an arbitrary order N_p+1 and the order of the denominator polynomial function is $N = 2S+F$, where S and F represent, respectively, the number of first- and second-order decimating blocks. After applying the multirate transformation the above function $H(z)$ can be written in the modified form (5) at the bottom of the next page, where the

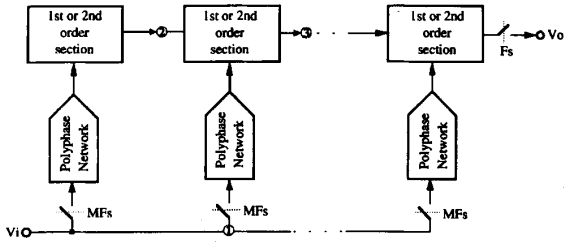

Fig. 9. Block diagram of an internally cascaded SC decimating filter.

numerator polynomial function is expressed by

$$\sum_{m=0}^{N_p+2S(M-1)+F(M-1)} a'_m \cdot z^{-m} = \sum_{j=0}^{N_p}(a_j \cdot z^{-j}) \cdot \prod_{i=1}^{S}\left(\sum_{k=0}^{2(M-1)} \alpha_{k_i} \cdot r_{p_i}^{-k} \cdot z^{-k}\right) \cdot \prod_{i=1}^{F}\left(\sum_{l=0}^{M-1} b_{0_i}^{M-l} \cdot z^{-l}\right). \quad (6)$$

C. SC Implementation and Design Equations

The overall z-transfer function $T(z)$ of an internally cascaded Nth-order SC decimating filter can be obtained from the partial z-transfer functions associated with the constituting blocks. Thus, we can write

$$\frac{V_{3_i}}{V_i}(z) = T_{31_i}(z) + T_{32_i}(z) \cdot \frac{V_{3_{i-1}}}{V_i}(z), \quad (7)$$

where $T_{31_i}(z)$ and $T_{32_i}(z)$ are the z-transfer functions relating the output terminal 3 with, respectively, the input terminal 1 and the input terminal 2 of building block i, and $V_{3_{i-1}}(z)/V_i(z)$ is related to the previous building block. Such expressions can be written as

$$T_{31_i}(z) = \frac{N_{31_i}(z)}{D_i(z)} \quad (8a)$$

and

$$T_{32_i}(z) = W_i(z) \cdot \left(\frac{N_{32_i}(z)}{D_i(z)}\right) \quad (8b)$$

where $D_i(z), N_{31_i}(z)$ and $N_{32_i}(z)$ depend on the order of the building block and $W_i(z)$ is the equivalent transmission factor of the SC coupling branch. For first-order building blocks, and referring to the schematic diagram of Fig. 1, $T_{31_i}(z)$ is expressed as

$$T(z) = z^{-k}\frac{\sum_{}^{N+M-1}(\pm)C_i \cdot z^{-i}}{(C+F) - C \cdot z^{-M}} \quad (9)$$

whereas the numerator polynomial is $N_{32_i}(z) = 1$. For second-order building blocks, and referring now to the schematic diagram of Fig. 2, $T_{31_i}(z)$ is given by expressions (10a) and (10b) (shown at the bottom of the next page), respectively, when output terminal 3 is taken from OA1 and OA2. The numerator polynomial $N_{32_i}(z)$ can have different expressions depending on the amplifier to which the coupling SC branch is connected and on which of the amplifiers is considered for taking the output signal to the following block. When output terminal 3 is taken taken from OA1 we have

$$N_{32_i}(z) = (B_i + FB_i) - z^{-M}, \quad (11a)$$

with the SC coupling branch connected to the amplifier with the integrating capacitor D, and

$$N_{32_i}(z) = E_i \cdot z^{-M} - (C_i + E_i) \quad (11b)$$

with the SC coupling branch connected to amplifier with the integrating capacitor B. When output terminal 3 is taken from OA2 the above expressions become

$$N_{32_i}(z) = A_i \cdot z^{-M} \quad (12a)$$

if the SC coupling branch is connected to amplifier with the integrating capacitor D, and

$$N_{32_i}(z) = (D_i + FD_i) - z^{-M} \quad (12b)$$

$$H(z) = \frac{\sum_{j=0}^{N_p} a_j \cdot z^{-j}}{\prod_{i=1}^{S}(1 - 2 \cdot r_{p_i} \cdot \cos(\theta_{p_i}) \cdot z^{-1} + r_{p_i}^2 \cdot z^{-2}) \cdot \prod_{i=1}^{F}(b_{0_i} - z^{-1})} \quad (4)$$

$$\overline{H}(z) = \frac{\sum_{m=0}^{N_p+2S(M-1)+F(M-1)} a'_m \cdot z^{-m}}{\prod_{i=1}^{S}(1 - 2 \cdot r_{p_i}^M \cdot \cos(M\theta_{p_i}) \cdot z^{-M} + r_{p_i}^{2M} \cdot z^{-2M}) \cdot \prod_{i=1}^{F}(b_{0_i}^M - z^{-M})} \quad (5)$$

TABLE III
NORMALIZED CAPACITANCE VALUES OF THE SC LOWPASS DECIMATING FILTER OF FIG. 10

C-set for OA#1	C-set for OA#2	C-set for OA#3	C-set for OA#4	C-set for OA#5
$A_1 = 4.75$	$C_1 = 7.49$	$C_2 = 1.52$	$A_3 = 6.72$	$C_3 = 8.19$
$B_1 = 5.23$	$D_1 = 2.04$	$F_2 = 2.97$	$B_3 = 5.74$	$D_3 = 3.64$
$Y_{11} = 1.17$	$FD_1 = 4.21$	$W_{12} = 1.22$	$W_{23} = 7.67$	$FD_3 = 1.00$
$Y_{12} = 1.21$	$X_{11} = 1.00$	$C_{21} = 1.95$	$Y_{301} = 1.00$	$X_{31} = 1.65$
$Y_{13} = 1.00$	$X_{121} = 1.05$	$C_{22} = 1.27$	$Y_{302} = 2.15$	$X_{321} = 1.20$
	$X_{122} = 1.04$	$C_{23} = 1.00$	$Y_{31} = 1.00$	$X_{322} = 1.02$
	$X_{131} = 1.00$		$Y_{321} = 1.00$	$X_{331} = 1.00$
	$X_{132} = 1.80$		$Y_{322} = 1.48$	$X_{332} = 1.63$
			$Y_{331} = 1.00$	
			$Y_{332} = 2.47$	

if the SC coupling branch is instead connected to the amplifier with the integrating capacitor B. The transmission factor $W_i(z)$ associated to the SC coupling branch can be expressed as

$$W_i(z) = W_i \cdot z^{-M} \tag{13a}$$

for positive coupling or, alternatively, as

$$W_i(z) = -W_i, \tag{13b}$$

for negative coupling.

Using the above expressions and considering that the first building block only has one input terminal, the overall z-transfer function $T(z)$ of an internally cascaded Nth-order SC decimating filter can be written as

$$T(z) = \frac{V_o = V_{3_{i=S+F}}}{V_i}(z) = \frac{1}{D_{S+F}(z)} \cdot \left[N_{31_{S+F}}(z) + W_{S+F}(z) \cdot N_{32_{S+F}}(z) \cdot \frac{V_{3_{S+F-1}}}{V_i}(z)\right]. \tag{14}$$

This function can be customized according to the topology of each building block and which, in turn, is selected depending on the resulting capacitor area, capacitance spread and also the performance under nonideal characteristics of the amplifiers. The resulting design equations giving the capacitance values of the circuit are determined by equating (5) to (14).

The selection of preferred circuit topologies for the Nth-order SC decimator building block is mainly related to its performance behavior under non-ideal characteristics of the amplifiers, namely the finite dc gain and bandwidth. This can be evaluated by considering the relative weight of the capacitive network connected to each amplifier during the operating phases of the circuit [9]. The choice of a particular topology will be then restricted by some constraints, the most important of which can be briefly summarized: (a) the SC coupling branch represented by $W_i(z)$ must be of type positive to decouple the settling of the amplifiers in the same phase, and (b) the damping of second-order building blocks must be of type resistive (switched-capacitors FB or FD in the diagram of Fig. 2) to decouple the settling of the amplifiers in the two-integrator loop recursive structure [9].

D. Example: Internally Cascaded Lowpass SC Decimating Filter

For illustration, we considered the design of an internally cascaded fifth-order elliptic SC lowpass decimating filter, with $M = 3$. For application in video communication the input and output sampling frequencies are, respectively, $3F_s = 40.5$ MHz and $F_s = 13.5$ MHz. The amplitude response possesses a passband ripple of 0.2 dB, cut-off frequency $f_c = 3.6$ MHz and a minimum 35 dB rejection above 4.44 MHz.

Following the procedure previously described we obtain the internally cascaded SC decimating filter shown in Fig.

$$T_1(z) = z^{-k} \frac{[(B+FB)\cdot X(z) - (C+E)\cdot Y(z)] + [E\cdot Y(z) - X(z)]\cdot z^{-M}}{(B+FB)\cdot(D+FD) - [A\cdot(C+E) - (2\cdot B\cdot D + B\cdot FB + D\cdot FD)]\cdot z^{-M} + [B\cdot D - A\cdot E]\cdot z^{-2M}} \tag{10a}$$

$$T_2(z) = z^{-k} \frac{(D+FD)\cdot Y(z) + [A\cdot X(z) - D\cdot(z)]\cdot z^{-M}}{(B+FB)\cdot(D+FD) - [A\cdot(C+E) - (2\cdot B\cdot D + B\cdot FB + D\cdot FD)]\cdot z^{-M} + [B\cdot D - A\cdot E]\cdot z^{-2M}} \tag{10b}$$

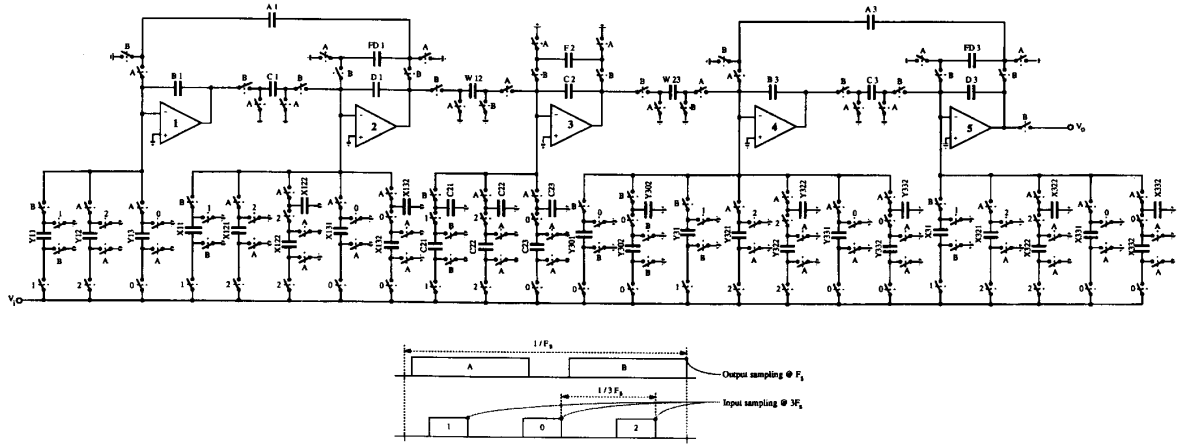

Fig. 10. Schematic diagram and switching waveforms of the internally cascaded lowpass SC decimating filter for video communication.

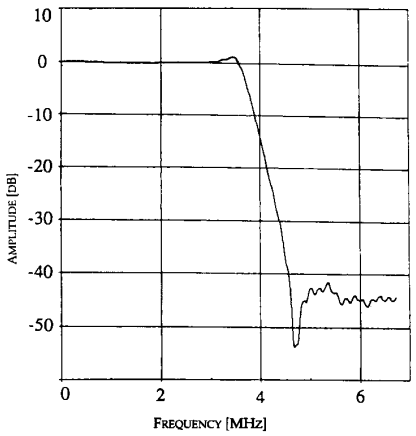

Fig. 11. Electrical simulated amplitude response of the lowpass SC decimating filter of Fig. 10.

10 together with the associated switching waveforms. After scaling for maximum signal handling capability we obtain the normalized capacitance values indicated in Table III yielding a maximum capacitance spread of 8.19 and total capacitor area of 92.48 units, and which compares favorably with more traditional SC filter designs [10]. In Fig. 11 we can observe the computer simulated passband and baseband amplitude responses obtained for this SC decimator considering amplifiers with 100 MHz gain-bandwidth product and 60 dB dc gain as well as realistic characteristics of the capacitance ratios and switches.

IV. Conclusion

This paper described two methodologies for designing Nth-order infinite impulse response switched-capacitor (SC) decimating filters with arbitrary integer decimating factors. The methodology employing *externally* cascaded first- and second-order building blocks is more appropriate to achieve high decimating factors but the resulting SC decimating circuits suffer from the effects of unwanted aliasing frequency components associated with the intermediate sampling frequencies. In the alternative methodology employing *internally* cascaded first- and second-order building blocks the resulting SC decimating circuits are immune to this problem but become more complex to design to attain high decimating factors. In general, such cascade SC decimating IIR filters allow not only to relax the requirements of continuous-time pre-filters in the context of traditional SC filter systems but also to employ operational amplifiers with more relaxed speed requirements than their traditional SC filters counterparts. The proposed methodologies were illustrated giving the design of SC decimating IIR filters for telephone channel data communication and video communication front-ends.

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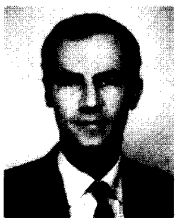

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