A 0.83-μW QRS Detection Processor Using Quadratic Spline Wavelet Transform for Wireless ECG Acquisition in 0.35-μm CMOS

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***Abstract*—Healthcare electronics count on the effectiveness of the on-patient signal preprocessing unit to moderate the wireless data transfer for better power efficiency. In order to reduce the *system power* in long-time ECG acquisition, this work describes an on-patient QRS detection processor for arrhythmia monitoring. It extracts the concerned ECG part, i.e., the *RR*-interval between the QRS complex for evaluating the heart rate variability. The processor is structured by a scale-3 quadratic spline wavelet transform followed by a maxima modulus recognition stage. The former is implemented via a symmetric FIR filter, whereas the latter includes a number of feature extraction steps: zero-crossing detection, peak (zero-derivative) detection, threshold adjustment and two finite state machines for executing the decision rules. Fabricated in 0.35-μm CMOS the 300-Hz processor draws only 0.83 μW, which is favorably comparable with the prior arts. In the system tests, the input data is placed via an on-chip 10-bit SAR analog-to-digital converter, while the output data is emitted via an off-the-shelf wireless transmitter (TI CC2500) that is configurable by the processor for different data transmission modes: 1) QRS detection result, 2) raw ECG data or 3) both. Validated with all recordings from the MIT-BIH arrhythmia database, 99.31% sensitivity and 99.70% predictivity are achieved. Mode 1 with solely the result of QRS detection exhibits 6 $\times$ reduction of system power over modes 2 and 3.**

***Index Terms*—QRS detection, quadratic spline wavelet transform, wavelet transform, wearable electrocardiograph (ECG) device, wireless ECG monitoring.**

I. Introduction

WIRELESS electrocardiogram (ECG) acquisition electronics has emerged as a comfortable low-cost technology for continuous cardiac monitoring. In order to release the patients from bulky devices and heavy wire connection, the on-patient front-end unit must be miniaturized in size and consume very low power. There are essentially three functional blocks: 1) an analog front-end for amplification and filtering, 2) an analog-to-digital converter (ADC) for digitization, and 3) a wireless transmitter for delivering the data to the back-end unit. Among them, as evidenced in other wireless biopotential acquisition systems [1], [2], the wireless transmitter dominates the system power. One effective way to save the wireless energy in Electroencephalography (EEG) seizure detection [1] is to locally compute the frequency-band energies before delivering the data, leading to 14 $\times$ system power saving comparing to full data transmission. For the wireless capsule endoscope reported in [2], local image compression leads to 2 $\times$ system power reduction.

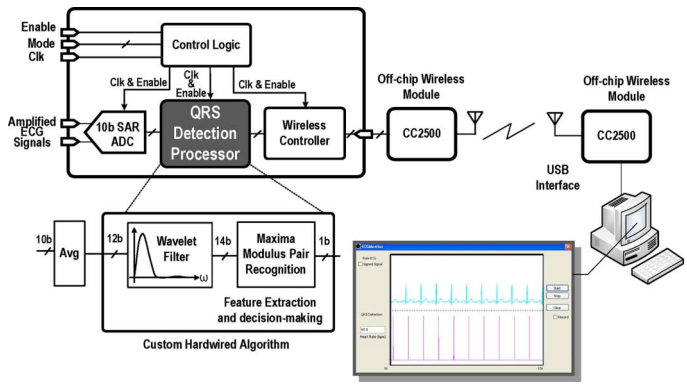

Fig. 1. QRS detection processor for a wireless ECG acquisition system.

For cardiac monitoring, the complete ECG data is normally a surplus in healthcare level. For instance, long-time arrhythmia monitoring is to detect the occurrence of arrhythmia and store an interval of the abnormal ECG, avoiding emitting and storing large amount of data [3]. In fact, just the *RR*-interval between the QRS complex is sufficed to accurately compute the heart rate variability (HRV) [4], [5]. In this respect, local signal preprocessing becomes a prospective way to avoid transmitting the redundant data. This paper describes a customized digital signal processor for *system power* reduction in a wireless ECG acquisition system (Fig. 1). The key attributes of the processor are the Quadratic Spline Wavelet Transform (QSWT), feature extraction and decision-making stages to optimize the detection accuracy of the QRS complex. A 10-bit SAR ADC (over-sampled by 4 to realize an effective resolution of 12 bits) and a wireless controller are co-integrated on chip to allow real-time verification. The wireless module is an off-the-shelf device similar to that in [1], which is managed by the proposed processor to transmit the data under different formats (i.e., the QRS detection result, the raw ECG data or both). With this flexibility, the full ECG data is

Manuscript received September 23, 2011; revised December 04, 2011; accepted February 03, 2012. Date of publication April 05, 2012; date of current version January 14, 2013. This paper was recommended by Associate Editor P. Chiang.

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Digital Object Identifier 10.1109/TBCAS.2012.2188798

also obtainable on demand, and the efficiency of the processor can be evaluated by comparing the power dissipation in each mode. The back-end of the system is a PC terminal that displays the digitized ECG signal, QRS complex occurrence and heart rate in real time. The recorded ECG data can be stored for further analysis.

The fabricated 0.35-μm CMOS processor with parallel- and pipeline-intensive architecture minimizes the clock rate (300 Hz) for achieving a 300-Sa/s throughput, measuring a very low consumption of 0.83 μW that compares much favorably with the available low-power processors; all still draw tens to hundreds of μW at their specified lowest clock rate of 1 MHz [6]–[9].

This paper is organized as follows: Section II introduces the QRS detection, discusses the ways of realization and briefly reviews the principles of wavelet transform (WT). Section III details the stage realization of the proposed QRS detection processor. The experimental results are reported in Section IV. The conclusions are drawn in Section V.

II. QRS Detection for ECG Signal Processing

In this section, the background of QRS detection is reviewed and its implementation method is discussed. The key principles and advantages of WT are briefly summarized.

A. QRS Detection

ECG is the heart biopotential consisting of P, QRS complex, T and U waves. The QRS complex strongly reflects the activity of the heart during ventricular contraction. Due to its detect-friendly characteristic shape, it can be served as the basis for automated determination of heart rate, or further ECG analysis such as the HRV, which is a key indicator of an individual's cardiovascular system. Substantial research effort had been paid on QRS detection [10].

There are two factors making QRS detection challenging: 1) ECG signal is likely contaminated by much noise and artifacts, such as powerline interference, electrode contact noise, patient-electrode motion artifacts, Electromyography (EMG), baseline wandering, data collecting device noise, quantization noise and aliasing, etc. 2) The wide variation of QRS morphologies and rhythms, from abnormal ECGs and interpersonal variations [11], [12]. As a result, a QRS detector must be particularly robust over noise and disturbance.

QRS complex detection algorithms typically consist of a preprocessing stage and a decision stage. The former is mainly based on baseline wandering removal, high frequency noise removal and transform of ECG waveform to specific patterns. The decision stage is to apply decision rules for QRS detection. The sensitivity (Se) and predictivity (Pr) of common software-based QRS detection methods are summarized in Table I. Among them, the WT shows the highest detection accuracy to date. Furthermore, WT can be realized with filter banks [13] which are implementation-friendly with digital circuits. WT method is therefore selected as the basis for this research.

QRS detection can be realized differently. An analog circuit can be low power and compact, but suffering from performance variability and process dependence [14]. Although general-purpose processors can offer re-configurability and excellent accuracy, the power dissipation is still too high for long-time monitoring. As flexibility and efficiency are generally trade-off in processors, avoiding the unnecessary overheads (e.g., extra logic, memory, IO ports) [15], [16] should potentially yield the highest power efficiency. In this work, a tailor-made digital processor is proposed for QRS detection, which allows more design flexibility for performance enhancements.

TABLE I
SUMMARY OF QRS DETECTION METHODS

Method	Se (%)	Pr (%)	Ref
Wavelet Transform	99.90	99.94	[17]
Band Pass Filter	99.69	99.77	[3, 18]
Curve Length Transform	99.65	99.77	[19]
Filter Bank	99.59	99.56	[20]
Genetic Algorithm	99.60	99.51	[21]
Mathematical Morphology	99.38	99.48	[22]

B. Wavelet Transform (WT)

WT is widely employed for singular point detection [17], [23]. It is also simple for digital circuit implementation as finite impulse response (FIR) filter structure can be employed for realization and the required number of gates and registers is normally small. The WT of a signal $f(t)$ is defined as

$$W_s f(u) = \langle f, \psi_{u,s} \rangle = \int_{-\infty}^{+\infty} f(t) \frac{1}{\sqrt{s}} \psi^* \left(\frac{t-u}{s} \right) dt \quad (1)$$

where Wf means wavelet transform of signal f with mother wavelet ψ with translation u and dilation s [24]. Symbol * denotes complex conjugate. Here s is a scale parameter often selected as the power of two, $\mathrm{s} = 2^j$ ($\mathrm{j} \in \mathrm{Z}$), where Z denotes integer. This type of WT is called dyadic WT. The dyadic WT can be calculated with Mallat's algorithm as follows:

$$S_{2^j} f(n) = \sum_{k \in Z} h_k S_{2^{j-1}} f(n - 2^{j-1}k) \quad (2)$$

$$W_{2^j} f(n) = \sum_{k \in Z} g_k S_{2^{j-1}} f(n - 2^{j-1}k). \quad (3)$$

Thus the WT can be computed with FIR filters with coefficients $\overline{h}_k$ and $\overline{g}_k$ ($\overline{h}_k = h_{-k}$ and $\overline{g}_k = g_{-k}$, together with down sampling recursively.

To provide approximate translation invariance which is important for detecting the temporal location of QRS complex, inserting zeros in the filter coefficients are performed instead of performing down sampling in WT. This is the "à trous" algorithm [25], [26] meaning zeros in the filter coefficients. Fig. 2 summarizes the differences of Mallat's and "à trous" algorithms.

III. Stage Realization of the QRS Detection Processor

This section details the realization of each stage: QSWT, feature extraction and decision-making.

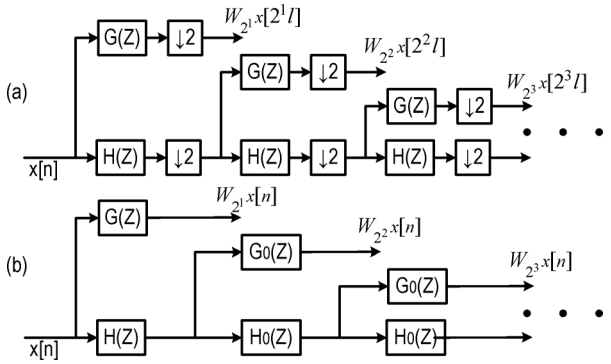


Fig. 2. (a) The Mallat's algorithm for WT. (b) "à trous" algorithm for WT. Here $\mathrm{H}(\mathrm{Z})$ and $\mathrm{G}(\mathrm{Z})$ mean the QSWT filters with coefficients shown in (5). $\mathrm{H}_0(\mathrm{Z})$ and $\mathrm{G}_0(\mathrm{Z})$ are the filters with coefficients inserted zeros.

A. Quadratic Spline Wavelet Transform (QSWT)

We employ the QSWT with compact support, and one vanishing moment as the mother wavelet $\psi(x)$. It is a 1st derivative of the smooth function. The QSWT is introduced in [27] and applied to QRS detection in [17]. Currently this method keeps highest detection accuracy comparing the other methods. Its compact support characteristic enables the FIR filter to be implemented with fewer taps. The Fourier transform characterizing its frequency response is shown as follows:

$$\Psi(\omega) = i\omega \left[\frac{\left(\sin \frac{\omega}{4}\right)}{\frac{\omega}{4}} \right]^4. \tag{4}$$

The corresponding filter coefficients are

$$\begin{aligned} \overline{h}(x) &= [\,\tfrac{1}{8} \quad \tfrac{1}{8} \quad \tfrac{1}{8} \quad \tfrac{1}{8}\,] \\ \overline{g}(x) &= [\,-2 \quad 2\,]. \end{aligned} \tag{5}$$

Fig. 3 shows the frequency responses of QSWT in one to five scales. The signal in various scales after QSWT comparing with the original ones is shown in Fig. 4. The output signal, which is called wavelet coefficients, is corresponding to the smoothed derivative of the input signal. One can read that the triangular waveform similar to R peak is transformed to modulus maxima pair (positive-maximum-negative-minimum pair). The zero-crossing point in modulus maxima pair corresponds to the R peak.

Note that the higher scale computation demands more filter taps and more power. After analysis, scale 3 of the QSWT is chosen for the ECG processing by considering the frequency distribution of the QRS complex, and filter tap number. The baseline wandering removal and 50/60 Hz notch filtering are expected to be provided in the analog front-end [28], [29] for power and area concerns. Besides the attenuation of baseline wandering of QSWT as shown in Fig. 3, further logic resource is not allocated in baseline wandering removal and 50/60 Hz notch filtering.

The input data type of QSWT is in a 12-bit 2's complement format. The bit width is compatible with [30], [31]. After the multiplication and addition computations, the data are truncated into a 14-bit 2's complement format by simulation optimization for power reduction.

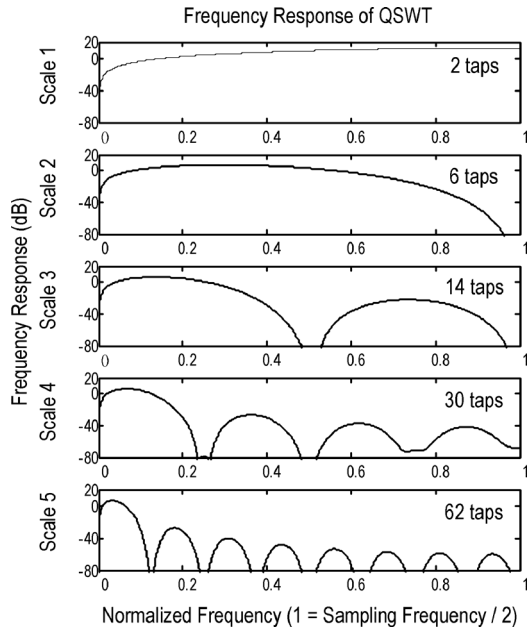


Fig. 3. Frequency responses of QSWT scales.

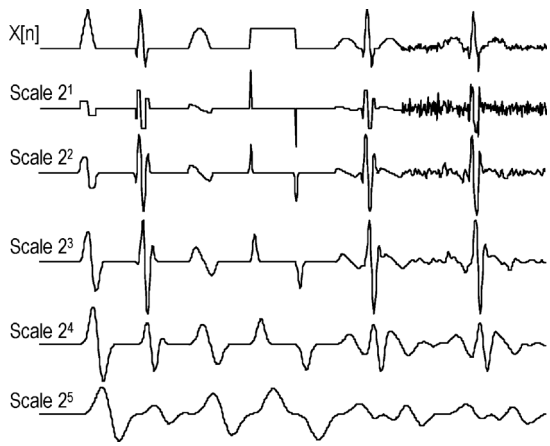


Fig. 4. Various shapes and their QSWT coefficients.

B. Modulus Maxima Pair Recognition Stage

The design of modulus maxima pair recognition (MMPR) stage is based on the principle of divide-and-conquer to solve the problem of recognizing the modulus maxima pair. As shown in Fig. 5 the MMPR structure, these works are attained by several sub-circuits for feature extraction and decision-making. The feature extraction is accomplished by zero-crossing detection, peak (zero-derivative) detection and threshold adjustment. The decision-making is realized by two finite state machines (FSM) for decision rule implementation. The features are extracted in parallel to minimize the clock rate of the circuits. The parallelism can further the power reduction since the circuit can operate slowly for the same computation, leaving much clock-delay margin for voltage supply reduction (i.e., power savings).

According to the information from the three sub-circuits, FSMs change state when finding a positive or negative peak, a zero crossing point and a peak with opposite direction to the previous peak, and output the markings of the temporal locations of QRS complexes.

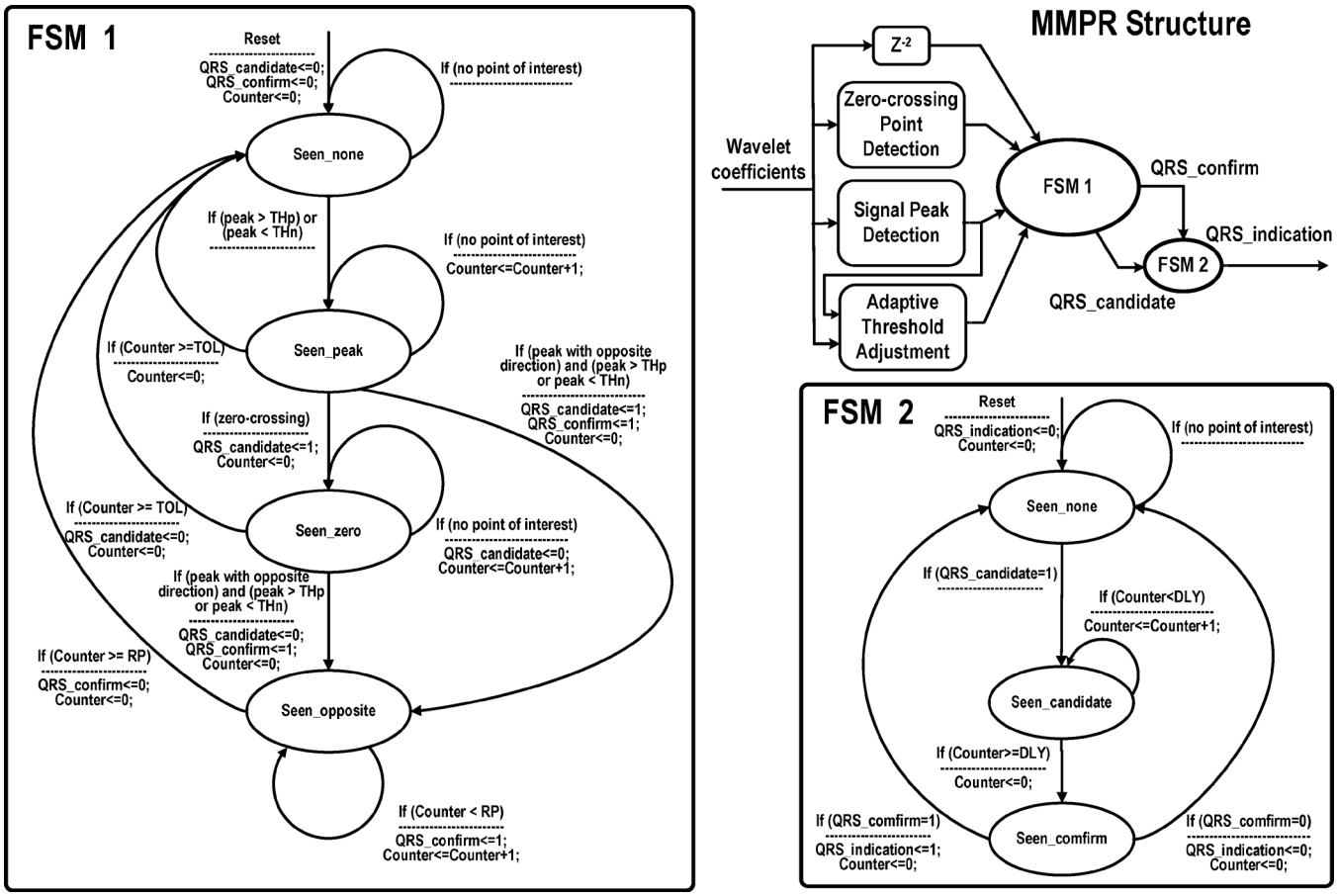


Fig. 5. Modulus Maxima Pair Recognition (MMPR) module and the two corresponding FSM for realizing the decision rules. Here peak means the point with derivative equal to zero. RP is refractory period meaning the blanking period rejecting the coming detection of QRS complex. TOL meaning tolerance is the waiting period for resetting the FSM. DLY is a fixed waiting period for QRS indication output. What under the dashed line are the actions.

1) Zero-Crossing Detection: The zero-crossing detection circuit checks the 14-bit 2's complement formatted wavelet coefficient input, and outputs the 1-bit indication of QRS complex occurrence. If the input wavelet coefficient is zero, the zero-crossing detection circuit directly outputs the indication, specifying the zero point in input data. In another more common condition, if the neighboring two samples of data are with opposite signs, the indication of zero-crossing will be outputted when the latter sample is inputted to the circuit. The equations are shown as follows:

$$\begin{aligned} if\ (x[n] \le 0) and (x[n+1] > 0) &\Rightarrow ZC[x[], n] = 1 \\ if\ (x[n] \ge 0) and (x[n+1] < 0) &\Rightarrow ZC[x[], n] = 2 \\ Others &\Rightarrow ZC[x[], n] = 0 \end{aligned} \quad (6)$$

where x is the input time series; n is the sample number; ZC represents the zero-crossing detection function.

2) Peak Detection: The peak detection circuit checks the 14-bit 2's complement formatted wavelet coefficient input, and outputs the 2-bit indication of the upward or downward peaks by detecting the zero-derivative points, which are the zero-crossing points of the first derivative of input wavelet coefficients. It employs a filter circuit with coefficients of $[\,1 \quad -1\,]$ and the zero-crossing detection circuit to realize this function. The equations that follow show where d approximates the derivative of input signal; ZC is now processing the time series d:

$$\begin{aligned} d[n] &= x[n+1] - x[n] \\ if\ (ZC(d[], n) = 1) &\Rightarrow Upward\ Peak \\ if\ (ZC(d[], n) = 2) &\Rightarrow Downward\ Peak. \end{aligned} \quad (7)$$

3) Threshold Adjustment: The threshold adjustment circuit classifies the peaks (zero-derivative points) of the input wavelet coefficients into peaks induced by noise and peaks induced by QRS complexes, and then stores the amplitudes of these peaks. The inputs of threshold adjustment circuit are the 14-bit 2's complement formatted wavelet coefficients and the 2-bit indication from peak detection circuit. The outputs are two threshold values in 14-bit 2's complement format, positive threshold and negative threshold. According to the amplitudes of recent classified peaks, the threshold adjustment circuit estimates the amplitude of noise signal and the amplitudes of modulus maxima which are induced by the QRS complexes. By multiplying empirical coefficients to estimated noise amplitude and signal amplitude, the thresholds are generated. The equations for threshold calculation follow:

$$\begin{aligned} if\ peak[n] \ge TH &\Rightarrow Signal\ Peak \\ if\ peak[n] < TH &\Rightarrow Noise\ Peak \end{aligned} \quad (8)$$

$$\mathrm{ASPL} = \frac{1}{M}\sum_{m=0}^{M-1} \mathrm{SignalPeak[n-m]} \quad (9)$$

$$\mathrm{ANPL} = \frac{1}{M}\sum_{m=0}^{M-1} \mathrm{NoisePeak[n-m]} \quad (10)$$

$$TH = ANPL + \beta(ASPL - ANPL) \quad (11)$$

where TH is the threshold output from the threshold adjustment circuit. $Signal\ Peak$ is the point with derivative which equals to zero and is classified as induced by the QRS complex. $Noise\ Peak$ means the point with derivative which equals to zero and is classified as induced by noise. Averaged Signal Peak Level (ASPL) is the running estimation of the signal peak (maxima) amplitude. Averaged Noise Peak Level (ANPL) is the running estimation of the noise amplitude. β is a percentage number. The variable M affects the speed of ASPL or ANPL in responding to the new SignalPeak or NoisePeak data. Here M is selected as 8 by simulation.

The calculation of positive and negative thresholds is done by two sets of these variables.

4) Finite State Machine (FSM): The decision-making is based on a temporal relationship of the aforementioned feature points. For preventing large data storage, two finite state machines are employed for decision-making, as shown in Fig. 5. They embody the decision rules in the state transition graph. FSM 1 is for the decision-making and FSM 2 is for marking the QRS complex position according to the signals from FSM 1. Four states are designed for representing the modulus maxima pair in FSM 1. The states follow.

Seen_none	is the starting state.
Seen_peak	means that the FSM has already detected a peak exceeded the threshold (valid peak).
Seen_zero	means that the FSM found the zero-crossing point after finding the valid peak.
Seen_negative	means the FSM found a peak with opposite direction and exceeding the threshold.

The decision rules are:

Classification Case 1: If the Seen_peak, Seen_zero and Seen_opposite states are passed, then the corresponding segment of signal is recognized as valid modulus maxima pair.

Classification Case 2: If the Seen_peak and Seen_opposite states are passed, the corresponding segment of signal is recognized as valid modulus maxima pair.

Waiting Period: If no valid peak or zero-crossing point encountered, the state machine would stay in the same state for a period of time, set as 0.07 s.

Reset Condition: If it stays in the same state for a period (0.07 s), or it is system startup, the state machine goes back to Seen_none state. This rule is helpful for system stability.

Refractory Blanking: After the state machine enters the Seen_opposite state, the state machine will stay in the same state in the coming 25 samples, and then it is directed to Seen_none state. This is because there is a physiological refractory period of about 200 ms after a QRS complex, which is without the occurrence of QRS complex [3]. It is helpful to decrease the possibility of false detection.

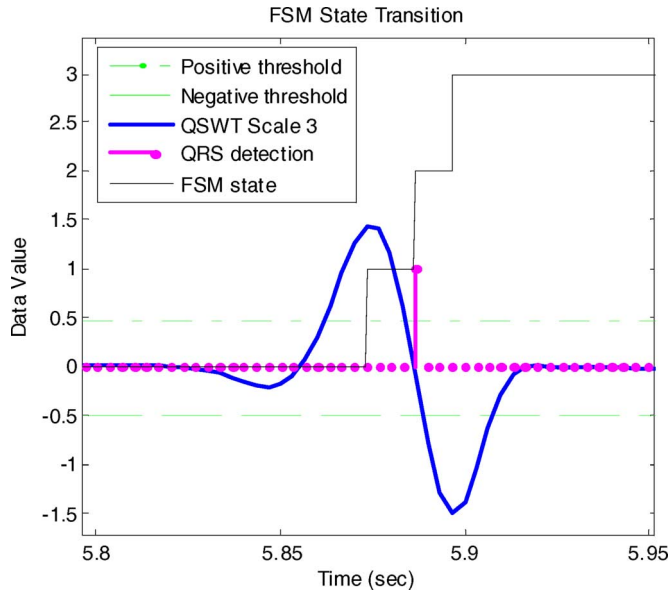


Fig. 6. State transitions (sampling rate = 300 Hz).

Since the temporal location of zero-crossing point within modulus maxima pair corresponds to the temporal location of QRS complex, but the zero-crossing point is inside the modulus maximum pair, the zero-crossing points are considered as potential QRS complex candidates and temporarily marked before finally seeing the whole modulus maxima pair.

The detailed architectures of the two FSMs are shown in Fig. 5. The state transition and corresponding detection signals are shown in Fig. 6. Two QRS detection cases of ECG signals without and with baseline wondering from the MIT-BIH arrhythmia database [30] are shown in Figs. 7 and 8, respectively.

For example, when a detection cycle starts, both FSM 1 and FSM 2 are in Seen_none states. These states keep until a peak with amplitude exceeding the positive or negative threshold according to the signals from Signal Peak Detection circuit and Adaptive Threshold Adjustment circuit. Then FSM 1 transits to Seen_peak state and stays if no zero-crossing point is found, for a waiting period TOL counted by the counter. When a zero-crossing point is found according to Zero-crossing Detection circuit, FSM 1 transits to Seen-zero state and sets the QRS_candidate register to 1 to inform FSM 2 that a potential QRS complex point is found. On the other hand, FSM 2 then transits from Seen_none state to Seen_candidate state and starts counting the time in this state. If FSM 1 sees a peak exceeding the thresholds with opposite direction to the previous found peak, it sets the QRS_confirm register to 1 for confirming the validity of the potential QRS complex point. Then FSM 1 stays in Seen_opposite state for a refractory period (RP) for rejecting the new detection. On the other hand, FSM 2 transits to Check_confirm state after a fixed delay, then it will check the QRS_confirm value and output the QRS_indication value. Finally, FSM 1 and FSM 2 run back to Seen_none states.

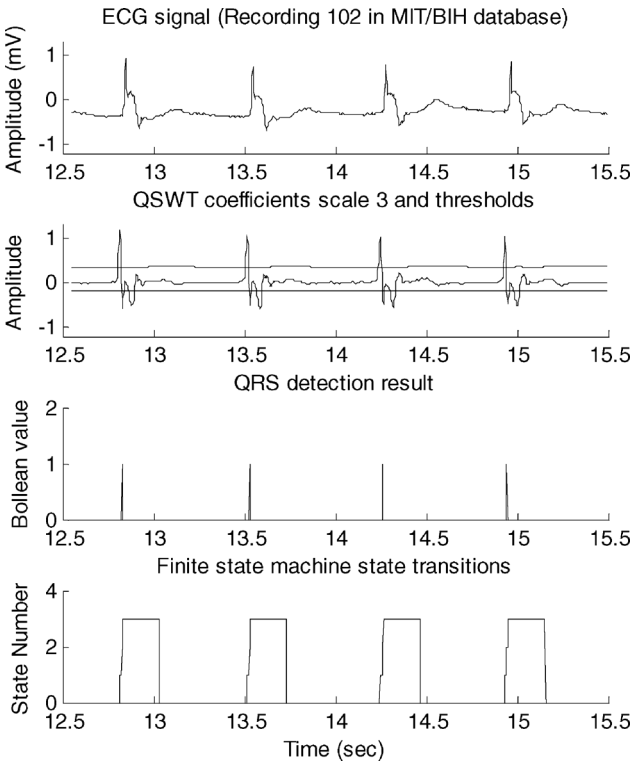


Fig. 7. Case 1: Corresponding signals for QRS detection.

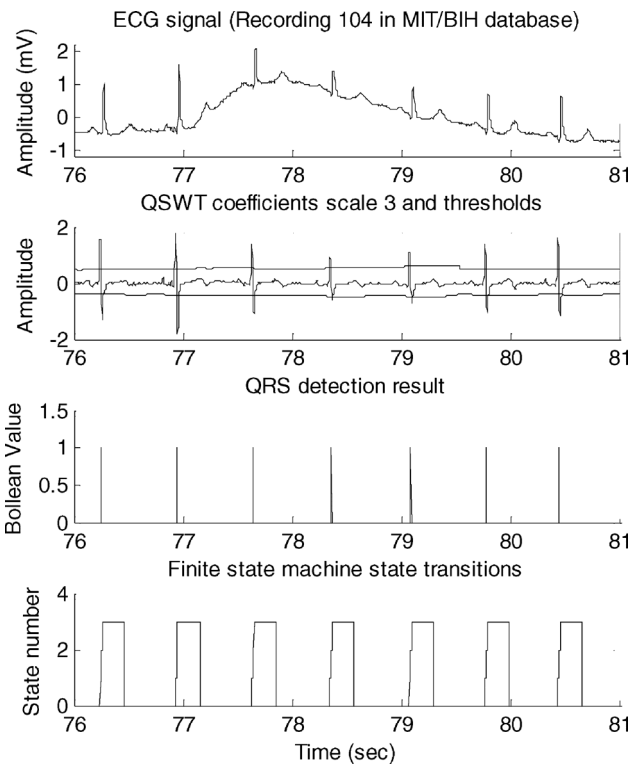


Fig. 8. Case 2: Corresponding signals for QRS detection.

FSM 1 sets the QRS_candidate signal to 1 when it enters the Seen_zero state, and also set the QRS_confirm signal to 1 within the whole Seen_opposite state. According to the QRS_candidate and QRS_confirm signals, FSM 2 can mark the QRS complexes with fixed delay.

C. System Design

A 10-bit SAR ADC and a wireless controller are also incorporated in the design for testing the whole system in real time. The conversion range is given by the voltage references. The key performance metrics are: $|\mathrm{INL_{typ}}| = 0.9\,\mathrm{LSB}$, $|\mathrm{INL}| < 2\,\mathrm{LSB}$, $|\mathrm{DNL_{typ}}| = 0.3\,\mathrm{LSB}$, $|\mathrm{DNL}| < 1\,\mathrm{LSB}$. $\mathrm{ENOB} = 9.4\,\mathrm{bits}$. The ADC oversamples the signal by a factor of 4 to re-produce an equivalent resolution of 12 bits. The clock frequencies of the ADC, QRS detection processor and system controller are 13.2 kHz, 300 Hz and 76.8 kHz respectively. Since the sampling rates of MIT-BIH Arrhythmia database and American Heart Association ECG database are 360 and 250 Hz respectively, the 300-Hz sampling rate within the region is justified [30], [31].

The input of the QRS detection processor is of 12-bit 2's complement format. The output is either a 1-bit indication of the QRS complexes or the raw ECG signal.

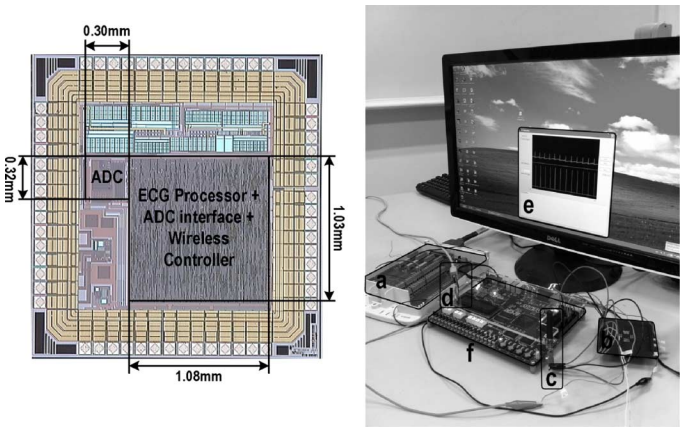
The wireless controller drives the off-chip TI CC2500 module [32]. Three transmission modes are offered: 1) the QRS detection result, 2) the ECG raw data, 3) both. In modes 2 and 3, 2 bytes are utilized per data packet, which includes one raw 12-bit data and one 1-bit QRS detection result and 3 control bits. In mode 1, we use one byte per data packet, which contains 3 control bits and five 1-bit QRS detection results. Therefore, the CC2500 transmits about 10 $\times$ less in mode 1 than in modes 2 and 3, lowering significantly the system power.

The specification of biopotential analog front-end can be found in [33], with programmable gain and signal filtering capability. The expected power consumption of it is 60 μW or lower. Although baseline wandering removal is commonly entailed for signal preconditioning in QRS detection, it is suggested not to realize it digitally because: 1) the baseline wandering can be more power and area efficient when realized in the analog front-end; 2) the QSWT already has a highpass response to attenuate the low frequency noise; 3) baseline wandering removal consumes large amount of logic resource (area) and power in the digital domain as the computational cost of baseline wandering removal is usually large (i.e., the cut-off frequency of the filter must be very low comparing to sampling frequency). For instance, filtering the low frequency noise via multi-scale mathematical morphology has been tried in the layout synthesis, but demanding huge chip area.

The realization of the processor is also speed-optimized to avoid a high frequency clock. The whole processor operates in pipeline and parallel architecture for feature extraction. The clock rate is 300 Hz with 1 sample/clock cycle. This slow-and-parallel technique lowers the logic delay requirement. A single 1.8-V supply is employed to allow reliable operation of all circuitry including the ADC in real-time measurements.

IV. Experimental Results

The processor (including the wireless controller) fabricated in 0.35-μm CMOS occupies $1.03 \times 1.08\ \mathrm{mm}^2$, whereas the ADC occupies $0.25 \times 0.32\ \mathrm{mm}^2$. The entire IC was tested at a single



(a) (b)

Fig. 9. (a) Microphotograph of the chip and testing system. (b) Testing platform of the chip. (a) NI Signal Acquisition/Generation Board for generating corresponding analog signal of MIT-BIH arrhythmia database. (b) The reported IC in a socket. (c) The off-chip RF module. (d) Wireless receiver. (e) Signal display user interface. (f) FPGA board for generating the clock for IC.

TABLE II
POWER CONSUMPTION (WITHOUT THE ACQUISITION ANALOG FRONT-END)

V_{DD}	Mode *	Power			
		ADC (μW)	Digital (μW)	Wireless TX (mW)	**Total (mW)**
	1	2.36	0.83	1.57	**1.58**
1.8V	2	2.38	1.55	9.37	**9.38**
	3	2.66	1.57	9.37	**9.38**

*Mode 1 stands for sending QRS detection result only. Mode 2 stands for sending raw ECG data. Mode 3 stands for sending both raw ECG data and QRS detection result.

1.8-V supply. Fig. 9 shows the chip microphotograph and the testing platform of the chip.

A. Performances of the QRS Processor

Table II summarizes the power consumed by each block in the 3 data transmission modes. Since only the QRS complex occurrence is transmitted in Mode 1, it lowers effectively the system power by 6 ×, verifying the feasibility of the proposed QRS detection processor. The wireless module TI CC2500 operates at 2.4 GHz with an output power of 0 dBm. In the system tests, the ECG signal is transmitted in a room at light-of-sight distance of 10 m. The Baud-rate is set to 250 kBaud and the package size is 12 bytes.

B. Verification With MIT-BIH Arrhythmia Database

The MIT-BIH arrhythmia database [30] is employed to evaluate the detection accuracy of the processor in real time under wireless acquisition. It is with 48 recordings of ambulatory ECG signal from 47 subjects. The signals are with a 360-Hz sampling rate, an 11-bit resolution and a 10-mV amplitude range. The performance indices: Sensitivity (Se) and positive prediction (Pr) can be calculated with the equations given by

$$Se(\%) = \frac{TP}{TP + FN} \tag{12}$$

$$Pr(\%) = \frac{TP}{TP + FP} \tag{13}$$

TABLE III
DETECTION RESULT WITH MIT-BIH DATABASE

record	Total (beat)	FN	FP	Se (%)	Pr (%)
100	2265	0	1	100.00	99.96
101	1860	1	1	99.95	99.95
102	2180	0	0	100.00	100.00
103	2078	0	0	100.00	100.00
104	2222	6	24	99.73	98.93
105	2565	27	48	98.95	98.14
106	2021	62	0	96.93	100.00
107	2131	1	3	99.95	99.86
108	1757	114	100	93.51	94.26
109	2524	5	0	99.80	100.00
111	2118	4	0	99.81	100.00
112	2531	1	1	99.96	99.96
113	1789	0	11	100.00	99.39
114	1872	7	0	99.63	100.00
115	1946	0	0	100.00	100.00
116	2404	19	1	99.21	99.96
117	1530	0	0	100.00	100.00
118	2271	2	6	99.91	99.74
119	1981	0	52	100.00	97.44
121	1856	2	0	99.89	100.00
122	2468	1	1	99.96	99.96
123	1513	0	1	100.00	99.93
124	1613	1	1	99.94	99.94
200	2593	5	4	99.81	99.85
201	1959	77	0	96.07	100.00
202	2128	21	0	99.01	100.00
203	2973	72	17	97.58	99.42
205	2648	12	0	99.55	100.00
207*	1850	17	5	99.08	99.73
208	2946	37	9	98.74	99.69
209	2997	1	3	99.97	99.90
210	2642	135	4	94.89	99.84
212	2740	0	0	100.00	100.00
213	3241	2	1	99.94	99.97
214	2254	6	0	99.73	100.00
215	3353	5	2	99.85	99.94
217	2202	11	2	99.50	99.91
219	2147	0	0	100.00	100.00
220	2041	0	0	100.00	100.00
221	2420	14	0	99.42	100.00
222	2474	12	0	99.51	100.00
223	2581	33	17	98.72	99.34
228	2047	28	11	98.63	99.46
230	2248	0	1	100.00	99.96
231	1565	0	0	100.00	100.00
232	1776	7	2	99.61	99.89
233	3069	5	1	99.84	99.97
234	2745	0	0	100.00	100.00
Total:	109134	753	330	99.31	99.70

* Episodes of ventricular flutter excluded from counts.

where FN meaning false negative is the number of fail detected true beats and FP meaning false positive is the number of false detected points. The detection accuracy is shown in Table III.

TABLE IV
BENCHMARK OF QRS DETECTION PROCESSORS

Ref	Method	Se (%)	Pr (%)	Area (mm^2)	Power (μW)	Tech. (μm)	V_{DD} (V)	Freq. (Hz)
This Work#	Quadratic Spline WT	99.31	99.70	1.11	0.83	0.35	1.8	300
Wang [34]^	Pan-Tompkins	95.65	99.36	0.68	2.21	0.18	N/A	500
Zhang [5]&	Mathematical Morphology	99.81	99.80	N/A	2.7	0.35	3.3	N/A
Phyu [35]	Wavelet Multiscale-Product	99.63	99.89	1.10	176	0.18	1.8	1 M

The power and area are also including the system controller.
^ The sensitivity / predictively results are from 5 records of MIT-BIH database
& Simulation results.

C. Benchmark With the State-of-the-Art

A comparison with prior arts is given in Table IV. The design [34] with the Pan-Tompkins method based on band-pass filtering, nonlinear computations and threshold have limited sensitivity ($\mathrm{Se} = 95.65\%$) and predictivity ($\mathrm{Pr} = 99.36\%$), even the power consumption is impressive (2.21 μW). The wavelet multiscale-product method [35] reports better accuracies ($\mathrm{Se} = 99.63\%$, $\mathrm{Pr} = 99.89\%$), but since RAM block is employed and the clock frequency is high, the power consumption is much higher (176 μW). Mathematical morphology QRS detection has also been reported [5] showing high accuracies ($\mathrm{Se} = 99.81\%$, $\mathrm{Pr} = 99.80\%$) with low power (2.7 μW), but the results are based on simulations. In this work, the employed Quadratic Spline WT achieves $\mathrm{Se} = 99.31\%$, $\mathrm{Pr} = 99.70\%$ and 0.83 μW of power in real-time measurements.

V. CONCLUSIONS

A 0.83-μW QRS detection processor realized in a 0.35-μm CMOS process for real-time wireless ECG monitoring has been presented. Quadratic Spline Wavelet transform provides pre-filtering, whereas the feature extraction circuits and two state machines offer modulus maxima pair recognition. Validated with all recordings in MIT-BIH arrhythmia database, the processor shows high sensitivity (99.31%) and predictivity (99.70%) in real-time tests. The system power is reduced by 6 $\times$ when compared with full-data transmission mode.

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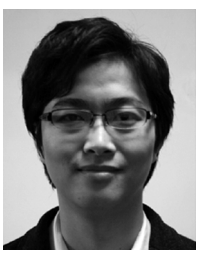

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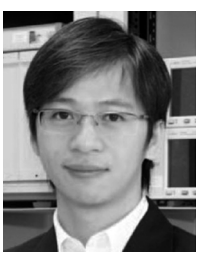

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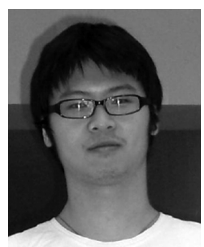

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