INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. (2012)
Published online in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.1875

Enhancing the performances of recycling folded cascode OpAmp in nanoscale CMOS through voltage supply doubling and design for reliability

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ABSTRACT

Current-oriented operational amplifier (OpAmp) design has been common for its orderly current-to-speed tradeoff. However, for high-precision or high-linearity applications, increasing the current does not help much, as the supply voltage (V_{DD}) and intrinsic gain of the MOSFETs in ultra-scaled CMOS technologies are very limited. This paper introduces voltage-oriented circuit techniques to address such limitations. Specifically, a $2xV_{DD}$-enabled recycling folded cascade (RFC) OpAmp is proposed. It features: (1) *current recycling* to enhance the effective trans conductance by 4x with no extra power; (2) *transistor stacking* to boost the output resistance by one to two orders of magnitude; and (3) V_{DD} *elevating* to enlarge the linear output swing by 4x. Comparing with its $1xV_{DD}$ RFC and FC counterparts, the proposed solution achieves 20-dB higher DC gain (i.e. 72.8 dB) in open loop and 20-dB lower IM3 (i.e., –76.5 dB) in closed loop, under the same power budget of 0.6 mW in a 1-V General Purpose 65-nm CMOS process. In many applications, these joint improvements in a single stage are already adequate, being more power efficient (i.e. less current paths), stable (i.e. more phase margin), and compact (i.e. no frequency compensation) than multi-stage OpAmps. Voltage-conscious biasing and node-voltage trajectory check ensure the device reliability in both transient and steady states. No specialized high-voltage device is necessary. Copyright © 2012 John Wiley & Sons, Ltd.

Received 14 December 2011; Revised 8 October 2012; Accepted 12 October 2012

KEY WORDS: operational amplifier; voltage supply; analog circuits; nanoscale CMOS

1. INTRODUCTION

With the rapid reduction of supply voltage (V_{DD}) in nm-length CMOS technologies, high-precision or high-linearity analog circuits (e.g. instrumentation amplifiers [1] and data converters [2]) are getting harder to be realized. Operational amplifier (OpAmp) is an essential building block of them [3, 4]. When speed is the priority, current-oriented OpAmp design is straightforward, i.e. as long as the phase margin is adequate, more current delivers higher gain bandwidth product (GBW) and slew rate (SR). However, increasing the current does not help much on the DC gain and output swing; both are highly relevant to the achievable precision and linearity of an analog circuit. A multi-stage OpAmp [5] has been the practice to alleviate the tradeoff between DC gain and output swing, but penalizing the power, stability and area when comparing with its single-stage counterpart.

Folded cascode (FC) is a single-stage OpAmp widespread for its balanced speed-to-power efficiency. Recently, a recycling FC (RFC) technique is proposed [6]. The currents of the idle devices are effectively re-cycled, improving the effective transconductance with no extra power or adverse effect on other performances. Nevertheless, this technique is still short for high-precision or

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high-linearity applications that essentially entail a high DC gain over a wide output swing [7]. Enhancing the DC gain via transistor stacking will penalize the output swing when the V_{DD} is limited; constituting a hard tradeoff cannot be simply alleviated by burning more current.

In view of that, the voltage-oriented OpAmp becomes more prospective [8], [9]. As shown in Figure 1, a high V_{DD} along with technology downscaling can directly enlarge the voltage headroom with respect to the threshold voltage (V_T), which will not be scaled much due to variability, matching and leakage issues. The key benefits of V_{DD}-elevated OpAmp are illustrated in Figure 2, where three possible output stages are shown. When considering the *output swing* and *DC gain*, transistor stacking is only effective when a high V_{DD} (e.g. double) is applied, given that the minimum overdrive voltage ($V_{ov,min} \approx 0.2$ V) almost does not scale with the technologies. Although the speed of cascode structures is not as fast as the non-cascode one due to the more non-dominant poles, the parasitic improvement of metallization and fine-linewidth interconnects of advanced CMOS technologies can still be fully benefitted. The design-for-reliability can be guided by the technology Design Rule Manual. It offers the essential reliability data related with the absolute maximum rating (AMR), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB) and negative bias temperature instability (NBTI). Managing the terminal voltages (V_{GS}, V_{DS}, V_{GD}) of each device via proper biasing and node-voltage trajectory checks can ensure no device is overstressed at all time.

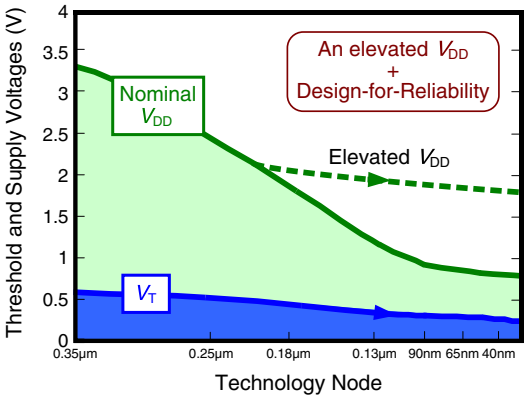


Figure 1. Increasing the design headroom via elevating the V_{DD}. Design for reliability can ensure no device is overstressed at all time.

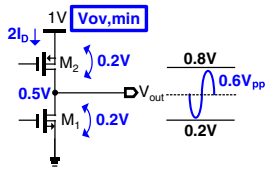
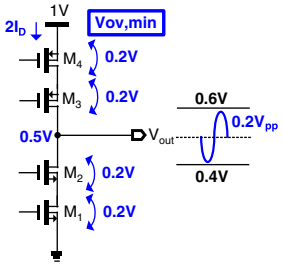
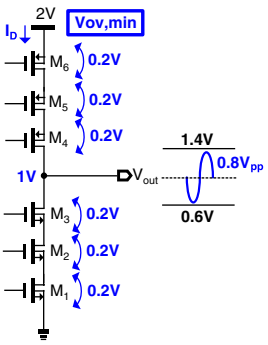
	1V-Non Cascode	1V-Double Cascode	2V-Triple Cascode
			
DC Gain	Low	Medium	High
GBW	High	Medium	Low
Output Swing	Medium	Low	High

Figure 2. Possible output stages of an OpAmp with Vov,min ≈ 0.2 V under the same power budget. The 2-V triple cascode design (right) offers higher DC gain and linear output swing than the 1-V non-cascode (left) and 1-V double cascode (middle) designs.

DOI: 10.1002/cta

In this paper, a voltage-oriented 2xV_{DD}-enabled RFC OpAmp is proposed. It combines *current recycling*, *transistor stacking* and V_{DD} *elevating* to optimize the performances. The merits are justified by comparing it with its 1xV_{DD} RFC counterpart, and its original 1x V_{DD} FC counterpart. Note that the true value of 2xV_{DD} for the employed 1-V General Purpose (GP) 65-nm CMOS process is 2 V, which can be easily generated by a 3.6/3.7-V Li-ion battery in typical portable systems.

2. COMPARATIVE STUDY OF 1XV_{DD} FC, 1XV_{DD} RFC AND 2XV_{DD} RFC OpAmps

For the conventional 1xV_{DD} FC OpAmp (Figure 3), M_3-M_4 operate purely as current sources, not contributing to the transconductance. Differently, the 1xV_{DD} RFC OpAmp (Figure 4) splits the input differential pair M_1–M_2 into two (M_{1a}, M_{1b} and M_{2a}, M_{2b}) which are fixed to conduct a bias current of $I_b/2$. Accordingly, M_3–M_4 can also be spitted into two, forming the current mirrors M_{3a}: M_{3b} and M_{4a}: M_{4b} with a dimension ratio of K : 1. The in-phase signal currents are summed at the source nodes of M_5 and M_6. As such, the effective transconductance of 1xV_{DD} RFC OpAmp is boosted by $1 + K$ times with no extra power when comparing with its 1xV_{DD} FC counterpart. Finally, the addition of M_{11}–M_{12} helps matching the drain voltages of M_{3a}: M_{3b} and M_{4a}: M_{4b}. The main overhead of the RFC technique is certain degradation of phase margin, which will be of more concern if the OpAmp is extended to a multi-stage design.

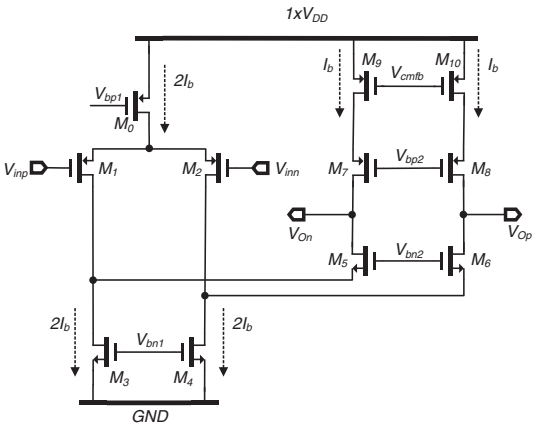


Figure 3. The conventional 1x V_{DD} FC OpAmp.

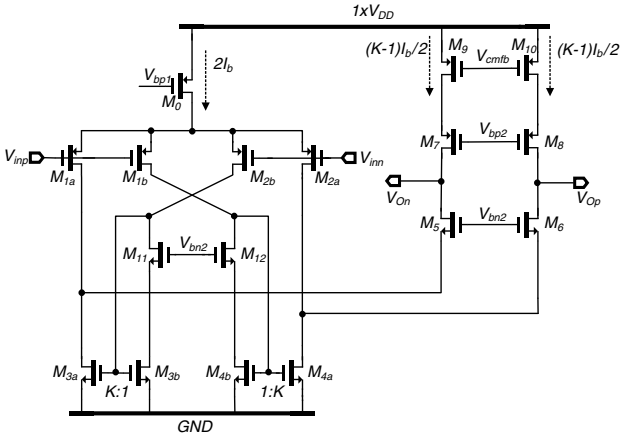


Figure 4. The 1x V_{DD} RFC OpAmp.

DOI: 10.1002/cta

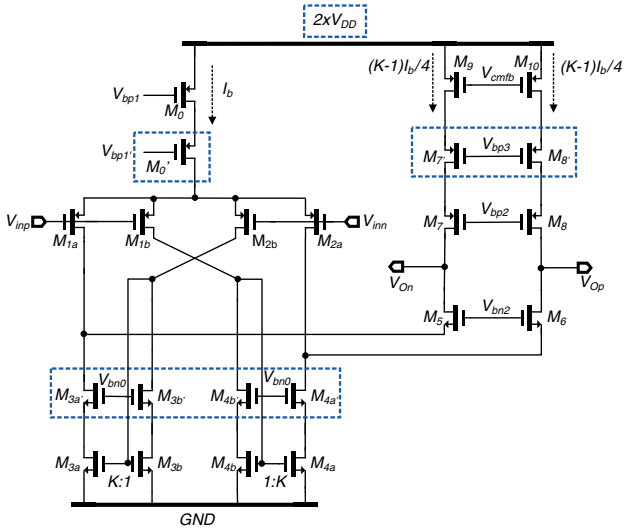


Figure 5. The proposed 2x V_{DD} RFC OpAmp.

Under the same power budget, doubling the supply is highly different from doubling the current. The proposed 2xV_{DD} RFC OpAmp adds only cascode devices as depicted in Figure 5. M_0' is added to boost the output resistance of the current source M_0 and thereby improves the OpAmp's common-mode rejection ratio. Similarly, (M_{3a}, M_{3b}, M_{4a}, M_{4b}) are cascoded with ($M_{3a'}$, $M_{3b'}$, $M_{4a'}$, $M_{4b'}$), and (M_7, M_8) are cascoded with ($M_{7'}$, $M_{8'}$). Thus, the OpAmp's DC gain is significantly enhanced due to the bigger output resistance of each gain node. Unlike the 1xV_{DD} FC and RFC OpAmps, the linear output swing of 2xV_{DD} RFC OpAmp is enlarged, too. The increased voltage stress is shared among the added cascoded devices.

In the following sub-sections, $V_{DD} = 1$ V is set for the employed GP 65-nm CMOS process. The key performances of 1-V FC, 1-V RFC and 2-V RFC OpAmps are compared under the same power budget. For the 1-V and 2-V RFC OpAmps, $K = 3$ is set to ensure the input and output currents are matched for optimum speed. All devices are assumed to be operated in the saturation region with the square-law equation given by,

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \tag{1}$$

where μC_{ox} is the technology constant, *W/L* is the device aspect ratio, V_{GS} is the gate-source voltage and V_T is the threshold voltage.

2.1. Transconductance and GBW

The effective transconductance (G_m) of each OpAmp topology is examined first. By finding the short-circuit current at the output with respect to the input we obtain,

$$G_{m,2\text{-V RFC}} = g_{m1a}(1 + K) \tag{2}$$

$$G_{m,1\text{-V RFC}} = g_{m1a}(1 + K) \tag{3}$$

$$G_{m,1\text{-V FC}} = g_{m1} \tag{4}$$

where g_{m1} (g_{m1a}) is the transconductance of M_1 (M_{1a}). Although the 2-V and 1-V RFC OpAmps show the same G_m expression, $G_{m,2V\text{-RFC}}$ is just 50% of $G_{m,1V\text{-RFC}}$ for its halved bias current. M_1 in FC is twice the size of M_{1a} and draws twice amount of current. Recalling that $K = 3$, G_m of 1-V RFC

DOI: 10.1002/cta

OpAmp is twice that of 2-V RFC and 1-V FC OpAmps under the same power. Thus, when speed is the priority, the 1-V RFC OpAmp should be chosen, as it should show the highest GBW among them.

2.2. DC gain

The DC gain can be expressed as the product of G_m and the output impedance R_O. It has been shown above that $G_{m,1V\text{-}RFC} = 2G_{m,2V\text{-}RFC} = 2G_{m,1V\text{-}FC}$. The 1-V RFC OpAmp, therefore, shows 6-dB higher DC gain compared to the other two under the same output resistance. However, the output resistance of 2-V RFC OpAmp should be bigger by one to two orders of magnitude, due to the smaller bias current and more stacked transistors. The corresponding output impedances of them are given by,

$$R_{O,2\text{-V RFC}} \approx \{(g_{m5} + g_{mb5})r_{o5}[(r_{o1a}||(g_{m3a'} + g_{mb3a'})r_{o3a'}r_{o3a})]\}||(g_{m7}r_{o7}g_{m7'}r_{o7'}r_{o9}) \tag{5}$$

$$R_{O,1\text{-V RFC}} \approx [(g_{m5} + g_{mb5})r_{o5}(r_{o1a}||r_{o3a})]||(g_{m7}r_{o7}r_{o9}) \tag{6}$$

$$R_{O,1\text{-V FC}} \approx [(g_{m5} + g_{mb5})r_{o5}(r_{o1}||r_{o3})]||(g_{m7}r_{o7}r_{o9}) \tag{7}$$

where r_o represents the output resistance of the corresponding transistors. M_{1a} (M_{3a}) in the 1-V RFC OpAmp conduct less current than M_1 (M_3) in the 1-V FC one, showing larger output resistance. As a result, $R_{O,2\text{-V RFC}} >> R_{O,1\text{-V RFC}} > R_{O,1\text{-V FC}}$ is expected.

2.3. Output swing

The output swing is greatly associated with the V_{DD}. Apparently, the 2-V RFC OpAmp has a larger signal swing under the same V_{ov} for all devices as given by,

$$V_{O_Swing,2\text{-V RFC}} = 2 \times [2 - (V_{ov3a'} + V_{ov3a} + V_{ov5} + |V_{ov7}| + |V_{ov7'}| + |V_{ov9}|)] \tag{8}$$

$$V_{O_Swing,1\text{-V RFC}} = 2 \times [1 - (V_{ov3a} + V_{ov5} + |V_{ov7}| + |V_{ov9}|)] \tag{9}$$

$$V_{O_Swing,1-\text{V FC}} = 2 \times [1 - (V_{ov3} + V_{ov5} + |V_{ov7}| + |V_{ov9}|)] \tag{10}$$

For a typical $V_{ov} \approx 0.2$ V, the differential swings are 0.4 V_{pp} (1-V FC), 0.4 V_{pp} (1-V RFC) and 1.6 V_{pp} (2-V RFC). Thus, the 2-V RFC OpAmp should be more superior for high-precision or high-linearity analog circuits.

2.4. SR

SR determines the large-signal response time and linearity of an analog circuit. When driving a capacitive load C_L, the SR of the 2-V RFC OpAmp can be analyzed as follows: when V_{inp} goes high, M_{1a} and M_{1b} will be turned off, forcing M_{4a}: M_{4b} and $M_{4a'}$: $M_{4b'}$ to shut down as well. Consequently, M_6 will be turned off whereas M_{2a} is driven into the deep triode region. All the tail current I_b goes through M_{2b} and is mirrored by a factor of K (M_{3b}: M_{3a}) into M_5. At the same time, the output current goes through M_7, and the two currents subtract at the V_{On} node. Thus, C_L is discharged by $2.5I_b$. For another half of the circuit, when V_{inn} goes down, M_6 is directly shut down so there is no current going through M_6. Thus, C_L is charged by $0.5I_b$ through M_8.

The above analysis is only correct when the circuit does not contain a common-mode feedback (CMFB). However, for a fully differential OpAmp, the CMFB is essential. With the use of CMFB, a symmetrical SR can be obtained. The charge and discharge currents will be averaged to be $1.5I_b$.

Similar analysis can be applied to 1-V FC and RFC OpAmps. The final averaged charge and discharge current for 1-V FC and RFC OpAmps are I_b and $3I_b$, respectively. In this way, the SR for the three OpAmps can be obtained,

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$$SR_{2\text{-V RFC}} = \frac{KI_b}{2C_L} \tag{11}$$

$$SR_{1\text{-V RFC}} = \frac{KI_b}{C_L} \tag{12}$$

$$SR_{1\text{-V FC}} = \frac{I_b}{C_L} \tag{13}$$

From Eqs. (11)–(13), we can show that $SR_{1\text{-V RFC}} = 2\ SR_{2\text{-V RFC}} = 3\ SR_{1\text{-V FC}}$. Note that these are the theoretical values. The accuracy of the current mirror can be degraded by large transients in practice. Indeed, the SR can be restricted by the sizing and bias conditions of M_5 and M_6.

2.5. Phase margin

All OpAmps feature the same dominant pole ω_{p1} associated with the loading capacitor C_L and a non-dominant pole ω_{p2} at the source of M_5 which is approximately located at g_{m5}/C_{gs5}. In addition, the 1-V and 2-V RFC OpAmps have a mirror pole-zero pair: $\omega_{p3} = g_{m3b}/(1+K)C_{gs3b}$ and $\omega_{z1} = (1+K)\omega_{p3}$, in the current mirrors M_{3b}:M_{3a} and M_{4b}:M_{4a}. The 2-V RFC OpAmp exhibits another high-frequency pole ω_{p4} at the source of $M_{3a'}$, locating at $g_{m3a'}/C_{gs3a'}$.

Although the 2-V RFC OpAmp has more non-dominant poles, its device sizes can be halved in comparing with the 1-V FC and RFC OpAmps, inducing less parasitic capacitance. For a reasonably large C_L, all the three OpAmps are safe in terms of stability. The pole-zero locations of the 2-V RFC OpAmp are depicted in Figure 6. It is assumed that all non-dominant poles are beyond the unity gain frequency ω_u for a good phase margin. Also, the locations of ω_{p2} and ω_{p3} may be interchanged depending on the design.

The value of K plays an important role in determining the phase margin of the 1-V and 2-V RFC OpAmps. For high-speed applications, K can be chosen such that $\omega_{p3} > 3\omega_u$ as given by,

$$\boldsymbol{\omega}_{p3} > 3\boldsymbol{\omega}_u \Leftrightarrow \frac{g_{m3b}}{(1+K)C_{gs3b}} > 3\frac{(1+K)g_{m1a}}{C_L} \Rightarrow K < \sqrt{\frac{g_{m3b}C_L}{3g_{m1a}}\,C_{gs3b}{}_{gs3b}{}^{m1a}} - 1 \tag{14}$$

which places an upper limit on K. For low-speed applications, the phase margin will not be restricted by K. A reasonable range for K value that can minimize the phase margin degradation is 2 to 4.

2.6. Noise

The OpAmp's noise can be a limiting factor of analog circuit's sensitivity. The output-referred squared noise current of a MOSFET is given by,

$$\bar{i_o^2} = \left[4k_BT\gamma g_m + \frac{K_F I_D}{C_{ox}L^2 f}\right]\cdot\Delta f \tag{15}$$

where the first and second terms represent the thermal and flicker noise, respectively. k_b is the Boltzmann constant, T is the temperature (Kelvin), γ is the bias-dependent parameter, K_F is a process-dependent constant, I_D is the drain current, C_{ox} is the gate oxide capacitance per unit area,

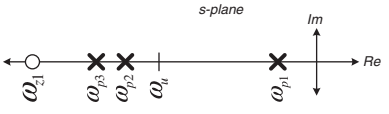

Figure 6. Pole-zero locations of the 2x V_{DD} RFC OpAmp in the s-domain.

DOI: 10.1002/cta

L is the channel length and f is the frequency. Eq. (16) is a simplified form of the complex models [10], [11] to aid the derivation. For comparison, the thermal and flicker noise components are examined individually. The input-referred thermal noise of 2-V RFC OpAmp can be calculated by adding the equivalent noise voltage of M_{1a}, M_{1b}, M_{3a}, M_{3b} and M_9, and doubling them. Similarly, the noises of 1-V FC and 1-V RFC OpAmps can be obtained as well,

$$\begin{aligned}\overline{v_{iT,\text{2-V RFC}}^2} &= \frac{8k_BT\gamma}{[g_{m1a}(1+K)]^2}\cdot\left[g_{m1a}+g_{m2b}\cdot K^2+g_{m3b}\cdot K^2+g_{m3a}+g_{m9}\right]\cdot\Delta f \\ &= \frac{8k_BT\gamma}{[g_{m1a}(1+K)]^2}\cdot\left[g_{m1a}+g_{m1a}\cdot K^2+g_{m3a}\cdot K+g_{m3a}+g_{m9}\right]\cdot\Delta f \\ &= \frac{8k_BT\gamma}{g_{m1a}(1+K)}\cdot\left[\frac{(1+K^2)}{1+K}+\frac{g_{m3a}}{g_{m1a}}+\frac{1}{1+K}\frac{g_{m9}}{g_{m1a}}\right]\cdot\Delta f\end{aligned} \tag{16}$$

$$\overline{v_{iT,\text{1-V RFC}}^2} = \frac{8k_BT\gamma}{g_{m1a}(1+K)}\cdot\left[\frac{(1+K^2)}{1+K}+\frac{g_{m3a}}{g_{m1a}}+\frac{1}{(1+K)}\frac{g_{m9}}{g_{m1a}}\right]\cdot\Delta f \tag{17}$$

$$\overline{v_{1T,\text{1-V FC}}^2} = \frac{8k_BT\gamma}{g_{m1}}\cdot\left[1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m9}}{g_{m1}}\right]\cdot\Delta f \tag{18}$$

At low frequency, the noise contributed by the cascode transistors is minor. Although 2-V RFC and 1-V RFC OpAmps have the same noise expressions, their corresponding transconductance are different and so as their noises. By substituting the following parameter relationships: $g_{\text{m1a}}=g_{\text{m1}}/4$, $g_{\text{m1a}}=3g_{\text{m1}}/8$ and $K=3$ in the 2-V RFC OpAmp, and $g_{\text{m1a}}=g_{\text{m1}}/2$, $g_{\text{m3a}}=3g_{\text{m3}}/4$ and $K=3$ in the 1-V RFC OpAmp, we can re-obtain Eqs. (16) and (17) as,

$$\overline{v_{iT,\text{2-V RFC}}^2} = \frac{8k_BT\gamma}{g_{m1}}\cdot\left[\frac{5}{2}+\frac{3}{2}\frac{g_{m3}}{g_{m1}}+\frac{g_{m9}}{g_{m1}}\right]\cdot\Delta f \tag{19}$$

$$\overline{v_{iT,\text{1-V RFC}}^2} = \frac{8k_BT\gamma}{g_{m1}}\cdot\left[\frac{5}{4}+\frac{3}{4}\frac{g_{m3}}{g_{m1}}+\frac{1}{4}\frac{g_{m9}}{g_{m1}}\right]\cdot\Delta f \tag{20}$$

Comparing Eqs. (18)–(20), one can calculate that $\overline{v_{iT,\text{2-V RFC}}^2}$ is the largest among them, whereas $\overline{v_{iT,\text{1-V FC}}^2}$ and $\overline{v_{iT,\text{1-V RFC}}^2}$ are comparable. The noise penalty of 2-V RFC OpAmp, however, is leveraged by its four-time higher output swing as described in Section 2.3. Thus, the signal-to-noise ratio of the 2-V RFC OpAmp can still be more favorable.

A similar conclusion as the thermal voltages is obtained for the flicker noises as given by,

$$\overline{v_{if,\text{2-V RFC}}^2} = \frac{K_{FP}}{\mu_P C_{ox}^2 W_1 L_1 f}\left[\frac{5}{2}+3\frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_3}\right)^2+\frac{1}{2}\left(\frac{L_1}{L_9}\right)^2\right]\cdot\Delta f \tag{21}$$

$$\overline{v_{if,\text{1-V RFC}}^2} = \frac{K_{FP}}{\mu_P C_{ox}^2 W_1 L_1 f}\left[\frac{5}{4}+\frac{3}{2}\frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_3}\right)^2+\frac{1}{4}\left(\frac{L_1}{L_9}\right)^2\right]\cdot\Delta f \tag{22}$$

DOI: 10.1002/cta

$$\overline{v_{if,1\text{-V RFC}}^2} = \frac{K_{FP}}{\mu_P C_{ox}^2 W_1 L_1 f}\left[1 + 2\frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_9}\right)^2\right]\cdot\Delta f \tag{23}$$

3. DESIGN FOR RELIABILITY

The AMR, HCI, TDDB and NBTI are the key reliability concerns of advanced CMOS technologies. Complying with them in the design phase indeed translates the term 'design for reliability' into 'voltage-conscious design', highly simplifying the design and verification methodologies [12]. Furthermore, in the topology formation phase, their implications to the circuits can be easily identified. Other reliability issues related to interconnects and materials like electromigration, stress-induced voiding and mechanical weakness are beyond the scope of this work.

3.1. AMR

The AMR corresponds to the maximum voltage applied to a minimum-gate-length device with no unrecoverable hard failure. The two primary concerns are the gate-oxide breakdown voltage and junction breakdown voltage. AMR is mainly related with the former: $|V_{GS,rms}|,|V_{GD,rms}| < V_{DD,}$ since they are normally three to four times smaller than the latter. A device biased close to the AMR limit may also lead to a deviation in device parameters, degrading the long-term reliability. The tolerable AMR is continuously reducing with the technologies.

3.2. HCI lifetime

Degradation of MOS device characteristics occurs as a result of exposure to a high V_{DS} with a large drain current. Examples of degradation are a shift of V_T and a shorter gate-oxide breakdown lifetime. HCI normally happens in high-power circuits such as the power amplifier, where the worst HCI bias conditions: $V_{DS} \geq V_{GS} \geq V_T$ and $V_{DS} \geq V_{DD}/2$ are concurrently satisfied. HCI degradation can be reduced by lowering the drain current or increasing the device channel length.

3.3. TDDB

TDDB is the wear-out of insulating properties of silicon dioxide in the CMOS gate, leading to the formation of a conducting path through the oxide to the substrate. In order to protect the circuit against TDDB, the catastrophic destruction of gate oxides induced by the maximum DC gate oxide voltage at different temperatures must be considered. According to the Design Rule Manual, NMOS has a higher voltage standing capability than PMOS for all cases to prevent TDDB.

3.4. NBTI

BTI degradation happens under steady-state conditions. It is design dependent in analog and RF circuits, and primarily only PMOS devices are subjected to BTI stress, namely NBTI. In a V_{DD}-upscaled design, analyzing NBTI involves detecting, in all modes of operation (DC and small signal), which PMOS device is exposed to a peak or rms voltage value exceeding the standard $V_{DD,}$ which is around 1 V in 65-nm CMOS.

3.5. Device stacking

With respect to the above-mentioned reliability concerns, an individual transistor basically can withstand just one V_{DD} for any of the two terminals: $|V_{GS,rms}(t)|$, $|V_{GD,rms}(t)|$, $|V_{DS,rms}(t)| < V_{DD.}$ In order to extend their voltage capability, stacking of devices can be applied. Generally, the voltage capability across the drain and source terminals can be multiplied by the number of stacked transistors. If a triple-well process is available, it will allow the NMOS to have an isolated bulk tied to the source terminal [i.e., $V_{BS,rms}(t) = 0$] to avoid overstressing. The triple well has been a common resource rather than an option in advanced CMOS technologies.

In addition to steady-state overstress, transient-state overstress should not be allowed, too. Depending on the nature of the signal processing, large-signal circuits requires checking the trajectory of all nodes. Alternative

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solutions are to employ voltage-biased and self-biased circuit topologies; both of them have the benefit that the internal node voltages can be easily controlled during power up/down transients.

3.6. Node-voltage trajectory checks

A $2xV_{DD}$ may generate reliability risk if inappropriately designed. Complying with the device reliability guides requires detailed node-voltage trajectory checks. First, the bias circuits should be tailored to include extra cascode devices to ensure all node voltages in steady state are within the reliability limits as shown in Figure 7. Second, transient simulations have to be performed with the maximum allowable input swing to check the overdrive condition of each device. In this work, a unity gain circuit [2] for testing the performance of the three OpAmps is assumed, as shown in Figure 8. To preserve the high output impedance of the amplifiers and limit the DC output current drawn, R was set to be 600 kΩ. C_1 and C_2 were set as 2 and 4 pF, respectively. Small parasitic capacitance could be seen from the two input transistors of the OpAmp, causing little phase shift between the open-loop and closed-loop configurations. However, since it is small (in the order of fF), the overall load is approximately 5 pF by eliminating the parasitic capacitance. The amplifiers are configured such that the input and output common-mode voltages are midway of the supply voltage to maximize the linear output swing.

Figure 9 shows the V_{GS}–V_{GD} relationship at an input swing of 1.2 V_{pp}. Since the circuit is differential, the simulation result just shows half of the circuit. It can be observed that both V_{GS} and V_{GD} vary within the ±1-V boundary and the variation is fairly small. Next, the V_{DS} trajectory is checked. Figure 10(a)–(c) shows the V_{DS} in a period of square-wave input under an input swing of 1.2, 1.6 and 2 V_{pp}, respectively. When the input swing is 1.2 V_{pp}, all V_{DS} are within the ±1-V boundary. When the input swing is increased, some of the V_{DS} exceed 1 V, reached 1.13 V (1.6 V_{pp}) for a 1.25 V (2 V_{pp}) input. Depending to the lifetime targets (e.g. 20 to 40 years), $V_{DS} > 1$ V may still be acceptable for some applications. Thus, an algorithm that can automatically track the overdrive voltages of all devices should be developed for industrial uses.

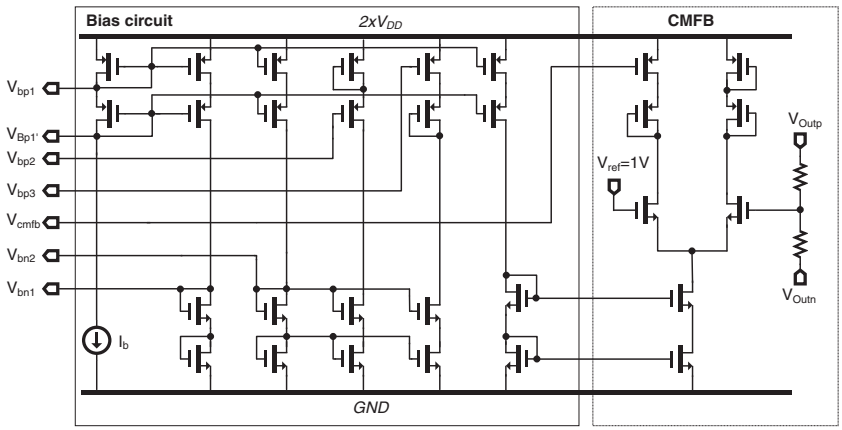

Figure 7. Bias and CMFB circuits of the 2x V_{DD} RFC OpAmp. Devices are not labeled for clarify.

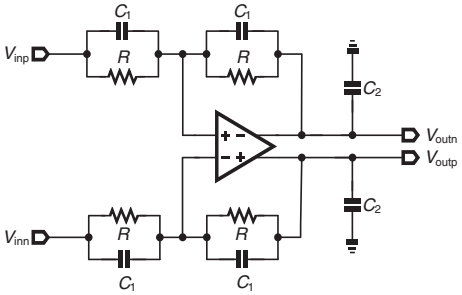

Figure 8. Testbench for reliability assessments.

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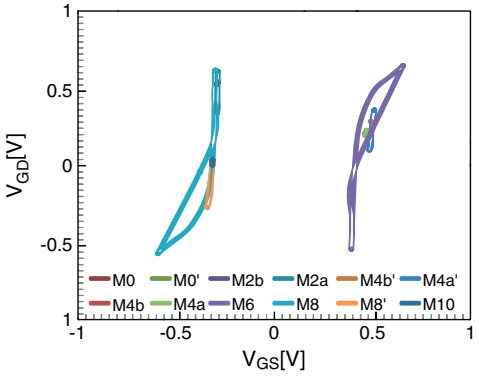

Figure 9. 2-V RFC OpAmp's V_{GS}–V_{GD} trajectories when a square-wave input is applied with a signal swing of 1.2 Vpp. The notations are corresponded to Figure 5.

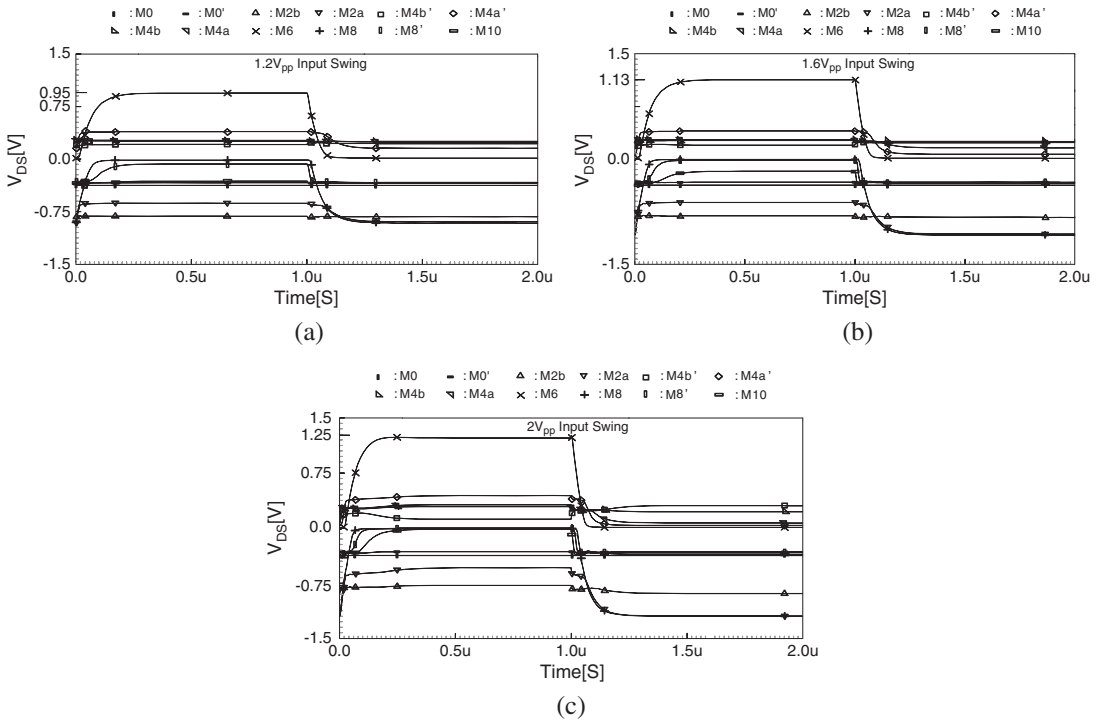

Figure 10. V_{DS} variation versus time at an input swing of (a) 1.2 V (b) 1.6 V and (c) 2 V. The notations are corresponded to Figure 5. The maximum V_{DS} is within 0.95, 1.13 and 1.25 V, respectively.

4. SIMULATION RESULTS

The three OpAmps are designed under the same power budget with their device sizes given in Table I. Their open-loop AC responses are shown in Figure 11(a) and (b). The open-loop DC gains of the 1-V FC, 1-V RFC and 2-V RFC OpAmps are 45.3, 54.0 and 72.8 dB, respectively, which indeed demonstrates the enhanced output impedance of the 2-V RFC and the enhanced gain of the 1-V RFC over the 1-V FC.

The GBWs of the 1-V FC, 1-V RFC and 2-V RFC OpAmps are 68.2, 157.8 and 97.5 MHz, respectively. The GBW of the 2xV_{DD} RFC, as expected, is less than that of the 1xV_{DD} RFC under the same power budget, but is fairly adequate for most analog functions in wireless applications. The phase margins for 1-V FC, 1-V RFC and 2-V RFC OpAmps are 86.6°, 60.9° and 70.7°,

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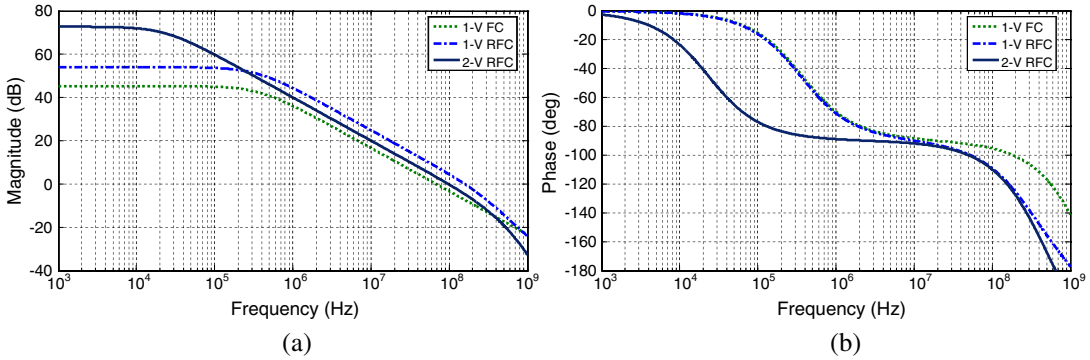
Table I. Device sizes (μm).

	1–V FC	1–V RFC	2–V RFC
M0	136/0.5	136/0.5	68/0.5
M0	–	–	68/0.5
M1/M2	136/0.4	–	–
M1a/M1b/M2a/M2b	–	68/0.4	34/0.4
M3/M4	96/0.5	–	–
M3a/M4a	–	72/0.5	36/0.5
M3a'/M4a	–	–	36/0.5
M3b/M4b	–	–	12/0.5
M3b'/M4b	–	–	36/0.5
M5/M6	16/0.2	16/0.2	8/0.2
M7/M8	72/0.5	72/0.5	36/0.5
M7'/M8	–	–	36/0.5
M9/M10	72/0.5	72/0.5	36/0.5
M11/M12	–	8/0.2	–



(a) (b)

Figure 11. (a) Gain and (b) phase responses of 1-V FC, 1-V RFC and 2-V RFC OpAmps.

respectively, at their respected GBWs. The phase margin of 1-V RFC OpAmp is smallest since it has the largest GBW and has more poles compared to the 1-V FC one. The 2-V RFC OpAmps shows less phase margin when comparing with the 1-V FC one, since the larger GBW and the multiple poles added by the cascode devices and current mirrors.

The linearity of the OpAmps is assessed as follows: two tones centered around 500 kHz (250 mV_{pp} at 450 kHz and 250 mV_{pp} at 550 kHz) were applied to the three OpAmps, and their results are shown in Figure 12(a)–(c). The third intermodulation distortion, *IM3*, is −49.7 dB (1-V FC), –57.2 dB (1-V RFC) and −76.5 dB (2-V RFC), as shown in Figure 13. For an analog-to-digital converter, the achieved gain of the 2-V RFC OpAmp corresponds to >11-bit resolution for an output swing as large as 0.8 V_{pp}. When they are in a unity-gain configuration, Figure 14 confirms the high gain accuracy of the 2-V RFC OpAmp over such a wide output swing.

For the SR, a 0.5-V voltage step was applied to the three OpAmps (in closed loop), and the results are given in Figure 15. The 1-V RFC has a clearly improved SR over the 1-V FC. The 2-V RFC still shows a SR higher than FC even it draws halved amount of current. The average SRs of the 1-V FC, 1-V RFC and 2-V RFC are 53.3 V/μs, 96.6 V/μs and 65.4 V/μs, respectively. No sign of ringing is visible in all step responses, which shows that the additions of the current mirrors and cascode trasistors M_{3a}:M_{3b}, $M_{3a'}$:$M_{3b'}$, M_{4a}:M_{4b}, $M_{4a'}$:$M_{4b'}$, $M_{0'}$, $M_{7'}$ and $M_{8'}$ in the 2-V RFC have not caused any stability issue. The 2-V RFC provides the highest steady-state accuracy.

The input-referred noises of the three OpAmps in closed loop are shown in Figure 16. When integrated over a bandwidth of 1 Hz to 100 MHz, the noises are 74.4 μV_{rms} (1-V FC), 64.3 μV_{rms} (1-V RFC) and 83.2 μV_{rms} (2-V RFC). The simulated input-referred offset voltages of the three OpAmps with process variation and mismatch do not show a big difference, as shown in Figure 17(a)–(c).

DOI: 10.1002/cta

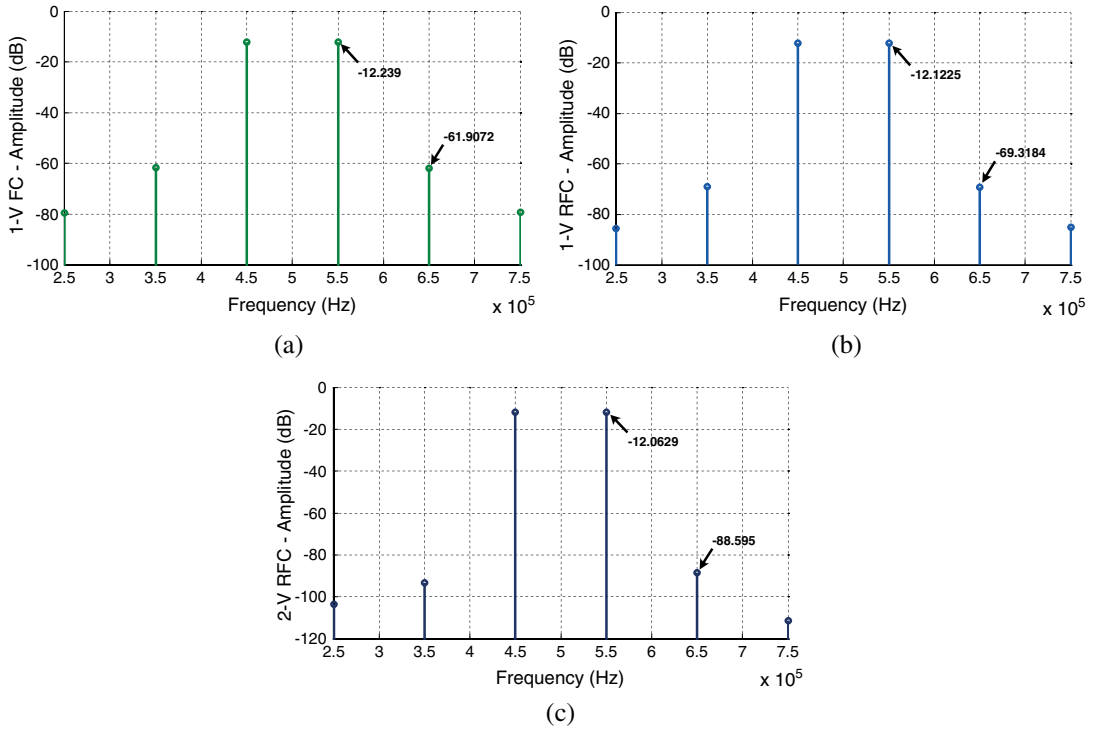


Figure 12. Two-tone tests in (a) 1-V FC, (b) 1-V RFC and (c) 2-V RFC OpAmps for a 0.5 Vpp signal around 500 kHz.

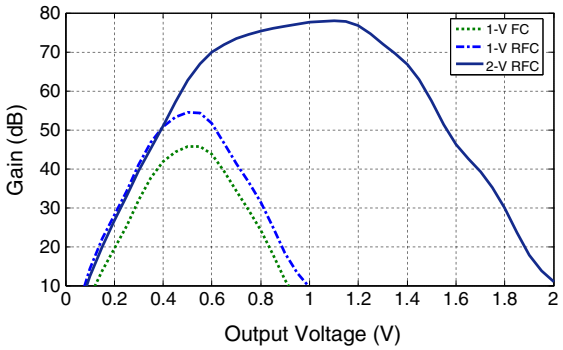


Figure 13. Open-loop gain versus output voltage. The common-mode voltages are Vcm,1-V FC = 0.5 V, Vcm,1-V RFC = 0.5 V and Vcm,2-V RFC = 1 V.

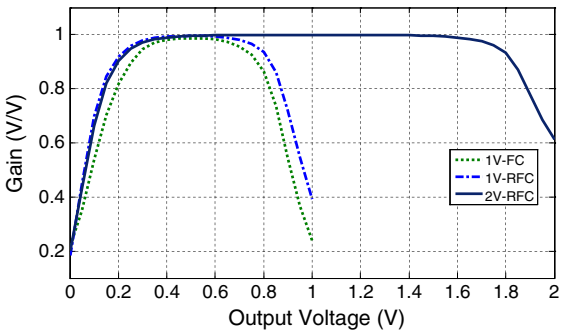


Figure 14. OpAmps in a unity gain configuration. The common-mode voltages are Vcm,1-V FC = 0.5 V, Vcm,1-V RFC = 0.5 V and Vcm,2-V RFC = 1 V.

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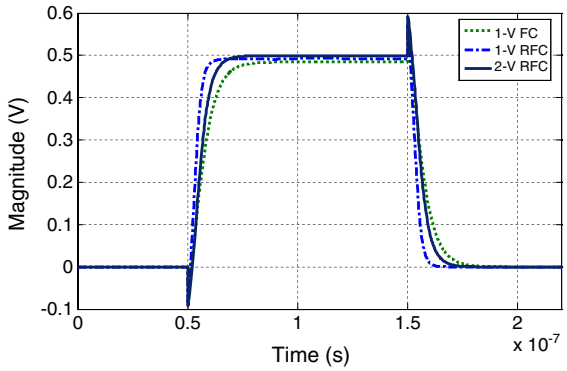

Figure 15. Large-signal step response of the three OpAmps in closed loop.

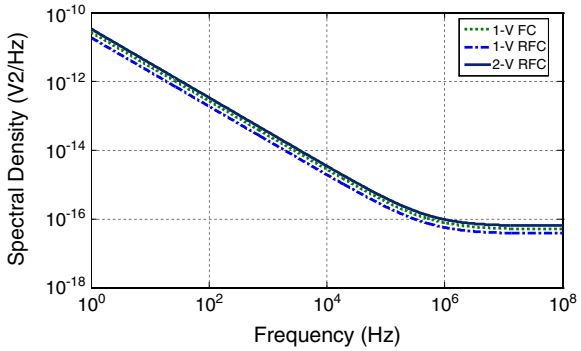

Figure 16. Input-referred noise spectral power density of the three OpAmps in closed loop.

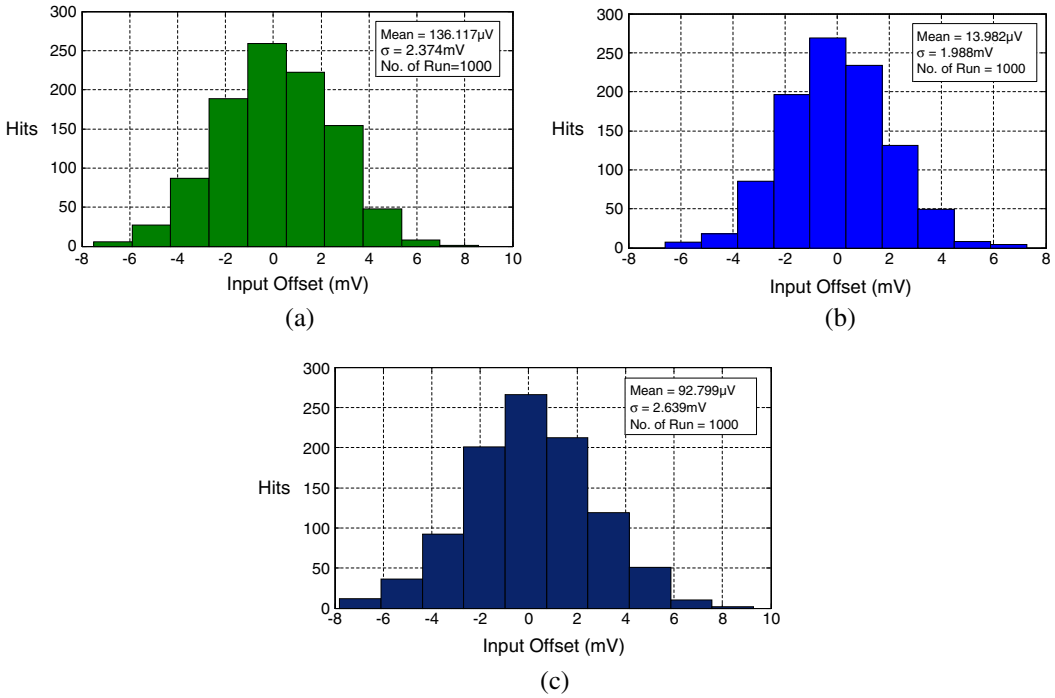

Figure 17. Input-referred offset voltages of the three OpAmps in closed loop: (a) 1-V FC. (b) 1-V RFC. (c) 2-V RFC.

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Table II. Performance summary of 1-V FC, 1-V RFC and 2-V RFC OpAmps.

Paramater	1-V FC	1-V RFC	2-V RFC
Power (Bias current) [μA]	600	600	300
DC gain [dB]	45.3	54.0	72.8
GBW [MHz]	68.2	157.8	97.5
Open-loop PM [deg]	86.6	60.9	70.7
Capacitive load [pF]	5.0	5.0	5.0
Slew rate (average) [V/μs]	53.3	96.6	65.4
1% Settling time [ns]	24.8	9.8	18.0
Gain precision (Closed loop, ideal case is 1)	98.6%	99.4%	99.8%
IM3, 0.5 Vpp at 0.5 MHz [dB]	−49.7	−57.2	−76.5
Input referred noise (1 Hz–100 MHz) [μVrms]	74.4	64.3	83.2
Input offset voltage [mV] (Closed loop, gain = 1)	2.37	1.99	2.64

With 1000 runs, the standard deviations (σ) of the input-referred offset voltage are 2.37 mV (1-V FC), 1.99 mV (1-V RFC) and 2.64 mV (2-V RFC).

Table II summarizes their simulation results. It can be observed that the 2-V RFC OpAmp is more effective in improving the DC gain, gain precision and linearity of analog circuits. However, when speed is the priority, the 1-V RFC OpAmp becomes more superior. In any case, both 1-V and 2-V RFC OpAmps are much improved when comparing with the conventional 1-V FC OpAmp.

It is also feasible that a 2-V analog circuit has to interface with a 1-V one. To solve the concern of unequal common-mode voltages, an additional current source can be served as the level shifter [13].

5. CONCLUSIONS

This paper has shown that a voltage-elevated OpAmp is more effective in realizing high-precision or high-linearity analog circuits in nm-length CMOS technologies. No specialized high-voltage device is entailed. Device reliability is ensured via voltage-conscious biasing and node-voltage trajectory checks. The design example is a 2-V RFC OpAmp optimized in 1-V GP 65-nm CMOS. It employs *current recycling* to boost G_m by 4x, *transistor stacking* to boost R_o by one to two orders of magnitude, and V_{DD} *elevating* to enlarge the output swing by 4x. The achieved DC gain and IM3 (in closed loop) are 20 dB better than its 1-V FC and RFC counterparts under the same power budget of 0.6 mW. On the other hand, when GBW and SR are the priorities, the 1-V RFC OpAmp is still more superior. The analytical and simulation results are in good agreements with each other. The authors believe that a cooperative research between circuit and reliability engineers is essential to rigidly investigate the true impact of the proposed techniques on the circuit reliability.

ACKNOWLEDGEMENTS

This research is funded by Macau Science and Technology Development Fund (FDCT) and the University of Macau Research Committee.

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