A 50-fJ 10-b 160-MS/s Pipelined-SAR ADC Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation

Yan Zhu, *Member, IEEE*, Chi-Hang Chan, *Student Member, IEEE*, Sai-Weng Sin, *Member, IEEE*, Seng-Pan U, *Senior Member, IEEE*, Rui Paulo Martins, *Fellow, IEEE*, and Franco Maloberti, *Fellow, IEEE*

***Abstract*—This paper presents a time-interleaved pipelined-SAR ADC with on-chip offset cancellation technique. The design reuses the SAR ADC to perform offset cancellation, thus saving calibration costs. The inter-stage gain of 8 is implemented in a 6-bit capacitive DAC with a flip-around operation. A capacitive attenuation used in both the first and second DACs significantly reduces the power dissipation and optimizes conversion speed. The detailed circuit implementation of the subthreshold op-amp is discussed, and the possible limits caused by nonidealities are analyzed for a proper correction in the design. These include the inter-stage-gain error and various channel mismatches of offset, gain, and timing. Measurements of a 65-nm CMOS prototype operating at 160 MS/s and 1.1-V supply show an SNDR of 55.4 dB and 2.72 mW total power consumption.**

***Index Terms*—Decoupled flip-around MDAC, offset-cancellation, pipelined-SAR ADC, V_{DD}-attenuator.**

I. Introduction

THE POWER effectiveness of a traditional pipelined analog-to-digital converter (ADC) [1]–[4] is not as good as the successive approximate register (SAR) ADC [5]–[8] with 10–12-bit and 50–100-MS/s specifications. This is attributed to the power consumed by the opamp(s). The problem becomes even more evident in nanometer CMOS technologies since high-gain opamp(s) designed with shrinking values of V_{DD} and intrinsic transistor gain consume significant power. SAR ADCs [9], [10] rely on the passive element (switched-capacitor circuit) and one comparator to perform the binary-searched feedback and comparison. The dynamic operation achieves ultralow-power efficiency but the capacitor mismatches and the high accuracy comparator, where the inputs difference of less than half of the least significant bit (LSB) is determined, limit its resolution. On the other hand, pipelined-SAR ADCs [11], [12] are architectures potentially capable of achieving both high conversion efficiency and resolution, because they use a lower number of opamp(s). The architecture uses two-step pipelined SAR ADCs to prevent high power consumption by the flash ADC in the conventional pipelined ADC. A proper choice of the inter-stage gain trades off the requirements of opamps and increased resolution of the second stage, thus optimizing power consumption. However, its speed benefit is not as significant as the SAR ADC as it needs an additional residue amplification phase. To further improve the conversion speed, a time-interleaved (TI) scheme was utilized in pipelined SAR architecture [13], [14] to release its speed bottleneck with competitive lower power dissipation. But, there are three key design limitations in the TI-pipelined-SAR ADC caused by comparator's offset, the unavailability of low-power flip-around MDACs and the static power requirements of the reference voltage generator.

The use of calibration improves the ADC design. This is particularly beneficial with nanometer CMOS technologies as they enable fast and effective digital logic processing. The analog-domain calibration corrects the nonlinearities of the ADC by properly adjusting circuit inaccuracies. Some SAR ADCs [15], [16] propose on-chip calibration of the conversion error caused by comparator offset and digital-to-analog converter (DAC) mismatches. However, power efficiency, area, complexity of the calibration circuit, as well as its adaptability for the on-chip implementation are of particular concern. For offset corrections less than 6 b, an analog method, such as a ring-counter-based offset calibration [15], [17] or a digital method like background averaging [13] are relatively simple and accurate. However, for medium resolutions of 8–10 b, the calibration usually requires on-chip complex logic algorithms that consume large area and power. Thus, for achieving low power consumption, it would be necessary to use methods that simultaneously explore analog and digital solutions to simplify hardware and attain design flexibility.

A pipelined-SAR architecture uses the first-stage capacitive DAC (CDAC) to perform residue amplification. However, the capacitive ratio of residue amplification increases with the resolution of the first-stage DAC array. Moreover, with the high-resolution front-end CDAC, using the flip-around MDAC becomes

Manuscript received February 03, 2012; revised May 04, 2012 and June 30, 2012; accepted July 10, 2012. Date of publication September 10, 2012; date of current version October 26, 2012. This paper was approved by Guest Editors Shen-Iuan Liu and Tsung-Hsein Lin. This work was supported in part by the Research Committee of the University of Macau and the Macao Science and Technology Development Fund (FDCT).

Y. Zhu, C.-H. Chan, and S.-W. Sin are with the State-Key Laboratory of Analog and Mixed Signal VLSI, and the Faculty of Science and Technology, University of Macau, Macao, China (e-mail: yanjulia@ieee.org).

S.-P. U is with the State-Key Laboratory of Analog and Mixed Signal VLSI and the Faculty of Science and Technology, University of Macau, Macao, China, and also with Synopsys-Chipidea Microelectronics (Macau) Ltd. (e-mail: benspu@ieee.org).

R. P. Martins is with the State-Key Laboratory of Analog and Mixed Signal VLSI and the Faculty of Science and Technology, University of Macau, Macao, China, on leave from the Instituto Superior Técnico, Lisbon, Portugal.

F. Maloberti is with the University of Pavia, Pavia, Italy, and also with the State-Key Laboratory of Analog and Mixed Signal VLSI, Faculty of Science and Technology, University of Macau, Macao, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2012.2211695

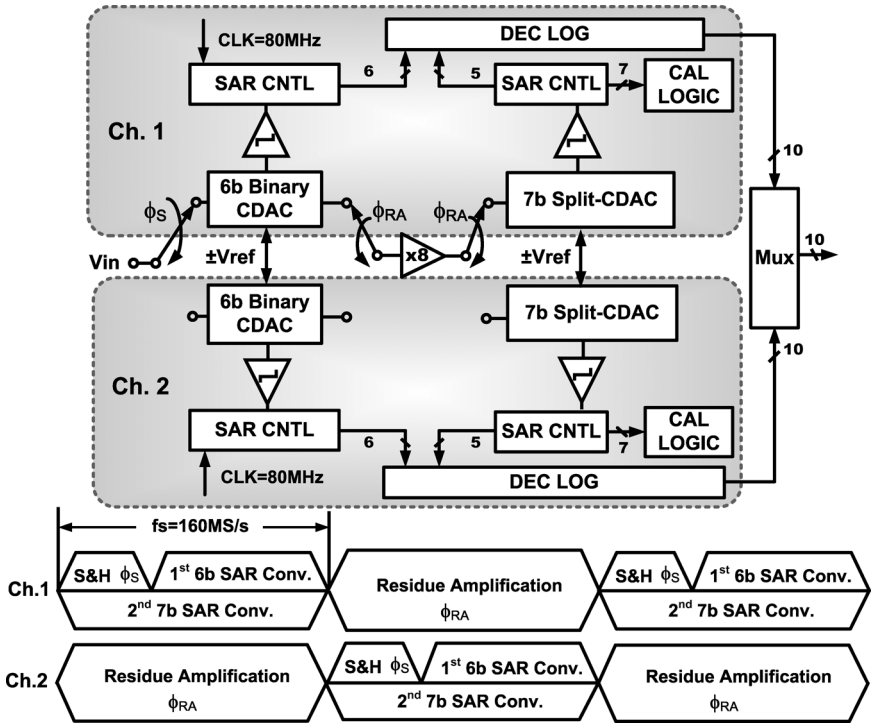


Fig. 1. Overall ADC architecture.

problematic. Previous works either employ a power-hungry resistive ladder that helps the limited resolution in the CDAC to enable the flip-around multiplying DAC (MDAC) [13] or an additional resetting capacitor required for a non-flip-around amplification with reduced feedback factor [11], [12], [14].

Typically, the reference buffers or resistive ladder of pipelined-SAR ADCs generate the reference voltages in the first- and second-stage SAR conversions [12]–[14]. This consumes large static power and increases *RC* settling time. In [13], the reference generation consumes 60% static power dissipation and significantly limits the conversion speed.

This paper presents a TI-pipelined-SAR ADC [18] which obtains remarkable power effectiveness for high conversion speed. This is achieved by using three strategies. First, the ADC corrects the offset with a self-embedded offset-cancellation scheme by reusing the second-stage SAR ADC. The calibration range of the offset can go up to the full-scale of the second stage, demanding very little area and digital power. Second, the capacitive array of the first-stage SAR serves a flip-around MDAC, which integrates the residual charge on a fraction of the array fed back according to the desired residue gain ratio. This solution improves the feedback factor. Finally, the design of CDACs in the first-and second-stage SAR ADCs is adjusted to perform reference-buffer-free SA conversion. By using the capacitive V_{DD}-attenuator, the reference supply voltage is scaled down to match the required reference ranges for both first- and second-stage SAR ADCs. Time-interleaving can multiply the speed of the ADC above the technology limits but it is susceptible to various types of channel mismatches of offset, gain, and timing. The experimental measures of a 65-nm CMOS prototype verify the effectiveness of the methods with state-of-the art results for medium resolution and conversion speed in the 100–200-MS/s range.

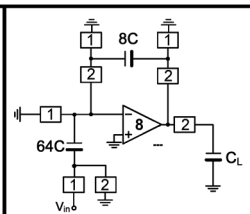
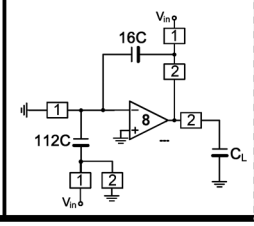
II. ADC Architecture

Fig. 1 shows the ADC architecture and timing diagram. The scheme is made up of two interleaved pipelined-SAR ADCs with a residue amplifier shared by the two channels (similar to [13]). The channels use 6-b and 7-b SAR ADCs, respectively (2 b of the second stage are for offset cancellation) with 1 b overlapping for digital error correction. The first-stage SAR converts the coarse 6-b code and generates the residue $V_{\rm resi}$ at the top-plate of the DAC, which is amplified by 8 to generate the input of the second-stage DAC. The second SAR operates in a pipeline fashion while the first stage starts a new cycle. The 6-b coarse code and the 5-b fine codes enter the digital correction logic to build the final 10-b output. The two extra bits of the second stage used for offset calibration do not increase the extra time requirement as the sample and hold (S&H) phase is not necessary for second-SAR conversion. Each channel operates at 80 MS/s with an equivalent duration of 6.2 ns each to perform the residue amplification and SA conversion.

III. Design Considerations

Time-interleaved pipelined-SAR architecture augments the conversion rate but the channel mismatches could impair performance. This issue can be addressed with various methods. Sharing the inter-stage amplifier avoids the offset mismatch in residual generation. The use of digital error correction relaxes the conversion accuracy of the first-stage SA decisions. However, the mismatches of gain, offset, and timing degrade the conversion linearity and should be considered in the circuit design. Moreover, an inter-stage gain of 8 is used for high-speed consideration. Since the power budget is correlated with the topology of the opamp, the open-loop gain and GBW are properly optimized.

TABLE I
COMPARISON OF NONFLIP-AROUND AND FLIP-AROUND OPERATIONS

		Unit Cap.(C)	Total Samp. Cap.	Total MDAC Capacitance	Output Loading	Feedback Factor	GBW
		Determined only by KT/C noise					
Non flip around operation		10fF	64C, 640fF	72C, 720fF	7.1C+C_L, 71fF+C_L	1/9	9CLBW
Flip around operation		5fF	128C, 640fF	128C, 640fF	14C+C_L, 70fF+C_L	1/8	8CLBW

A. Gain Mismatches

Due to the shared opamp, the gain mismatches in this work are mainly caused by the capacitor mismatches of the first- and second-stage CDACs. Assuming that the channel gain-mismatch components δ_m are independent, identically distributed Gaussian random variables with zero mean and a standard deviation of σ_{gmis}, the SNDR due to the gain mismatch can be derived as [19]

$$\mathrm{SNDR}_{\mathrm{gain,mis}} = 20\log\left(\frac{1}{\sigma_{\mathrm{gmis}}}\right) - 10\log_{10}\left(1-\frac{1}{M}\right) \quad (1)$$

where $M = 2$is the number of TI channels. Considering that the limited quantization noise of a 10-b ADC is 62 dB, the expected SNDR needs to be designed with a value higher than this level. To achieve 66-dB SNDR, the σ_{gmis} should be less than 0.07%. In a TI-pipelined-SAR architecture, the gain mismatch derives from both the first and second stages, and it can be represented as

$$\sigma_{\mathrm{gmis}} = \sqrt{\sigma_{\mathrm{gmis1}}^2 + \sigma_{\mathrm{gmis2}}^2/G^2} \quad (2)$$

where σ_{gmis1} and σ_{gmis2} are the standard deviations of the first-and second-stage gain-mismatch components, where $G = 8$ is the inter-stage gain. Accordingly, the σ_{gmis1} and σ_{gmis2} need to be less than 0.049% and 0.39%, respectively.

B. Offset Mismatches

The first-stage comparators, the opamp and the second-stage comparators, generate offsets in a TI pipelined-SAR ADC. Since the opamp is shared by two channels and the use of digital error correction relaxes the sum of the input-referred offset (including the first-stage comparators' and opamp's offset requirement), it will not cause any conversion nonlinearity, as its value is designed to be within 7 b that is 8.6 $\mathrm{mV_{p-p}}$ (the full-scale version of the ADC is 1.1 $\mathrm{V_{p-p}}$ and 8× offset is required to be less than 1/4 $\mathrm{V_{FS-2nd}}$ of 68.75 $\mathrm{mV_{p-p}}$). When its value exceeds the request, a large conversion distortion will occur due to the offset saturated at the second-stage SAR conversion. On the other hand, the offsets of the second-stage comparators cause offset mismatch tones in the TI-pipelined SAR ADC, if they are not precisely estimated and calibrated. Assuming the channel offset-mismatch components δ_m and a standard deviation of $\sigma_{\mathrm{os-2nd}}$, the SNDR due to input-referred offset σ_{os} ($\sigma_{\mathrm{os}} = \sigma_{\mathrm{os-2nd}}/8$) mismatch of the second-stage SAR ADC can be calculated as [19]

$$\mathrm{SNDR}_{\mathrm{offs,mis}} = 20\log\left(\frac{A_{\mathrm{in}}}{\sqrt{2}\sigma_{\mathrm{os}}}\right) - 10\log_{10}\left(1-\frac{1}{M}\right) \quad (3)$$

where A_{in} equal to 1.1 is the amplitude of the input signal. To achieve 66-dB SNDR, the $\sigma_{\mathrm{os-2nd}}$ should be less than 4.4 mV. This design uses a self-embedded offset cancellation which compensates for the second-stage comparator offset to less than 9 b at a very low cost. The method is described in the next section.

C. Timing Mismatch

Timing mismatch or periodic timing skew in TI systems refers to the mismatch in the sampling instant inside the individual channel. Inaccurate sampling clock edges generated by the mismatch in the clock generation paths give the rise to them. The SNDR thus caused can be calculated as [19]

$$\mathrm{SNDR}_{\mathrm{time,mis}} = 20\log\left(\frac{1}{2\pi f_0\sigma_t}\right) - 10\log_{10}\left(1-\frac{1}{M}\right) \quad (4)$$

where σ_t represents the standard deviation of the timing mismatch in unit of second and f_0 is the input frequency. To achieve 66-dB SNDR with $f_0 = 80$ MHz, the σ_t needs to be suppressed to less than 1.4 ps. Timing mismatch is difficult to be compensated due to its signal-dependent dynamic nature. In this design, the timing mismatch is tolerated by design constraint, and no timing mismatch calibration is utilized.

TABLE II
DESIGN CONSIDERATIONS OF THE OPAMP AND SECOND-STAGE SAR WITH RESPECT TO DIFFERENT INTER-STAGE GAIN

Inter-stage Gain	Opamp					2nd-stage SAR		
	Finite DC Gain (dB)	GBW (GHz)	Output Swing (mV)	W/L of Differential pairs	Power Consumption	Resolution	Offset Mismatch Tolerance σ_{os} (mV)	Gain Mismatch Tolerance σ_{gmis} (%)
32x	60	2.84	550	8α	$8g_m(V_{GS}\text{-}V_{TH})V_{DD}$	6b	17.6	1.56
16x	54	1.42	275	4α	$4g_m(V_{GS}\text{-}V_{TH})V_{DD}$	7b	8.8	0.78
8x	48	0.71	137.5	2α	$2g_m(V_{GS}\text{-}V_{TH})V_{DD}$	8b	4.4	0.39
4x	42	0.36	68.8	α	$g_m(V_{GS}\text{-}V_{TH})V_{DD}$	9b	2.2	0.19

D. Open-Loop Gain and GBW

The pipelined-SAR architecture uses the first-stage CDAC to perform both 6b conversion and the residue amplification. The inter-stage gain G is the ratio of the total array capacitance and the feedback capacitor. As shown in Table I, a nonflip-around amplification [11], [12], [14] by 8 would require using an extra capacitor 8C, which is 1/8 of the total array capacitance 64C. Therefore, the feedback factor of a nonflip-around operation β_{NFA} is 1/9. The increasing of the feedback factor improves the open-loop gain and closed-loop bandwidth (CLBW) of the opamp, which is essential for high-speed operation. In this design, by implementing a flip-around MDAC, the feedback factor β_{FA} is improved from 1/9 to 1/8. The circuit details pertaining to this will be presented next. The design comparison of nonflip- and flip-around operations are illustrated in Table I. The total sampling capacitances in both cases, which are determined only by the kT/C noise, are equivalent. Assuming that to satisfy 10-b kT/C noise the required sampling capacitance is 640 fF. Accordingly, the flip-around operation only needs half of the unit capacitance of the nonflip-around one. The nonflip-around operation gives rise to its total MDAC capacitance, due to the implementation of the extra capacitor of 8C. The benefit of the flip-around operation becomes more significant, as lower G is implemented. For example, with G of 16, the β_{FA} is increased by only 5% as compared to the nonflip-around one, while the improvement of β_{FA} goes up to 20% with a G of 4.

The finite dc gain A of the required opamp is competitively relaxed by implementing an inter-stage gain of 8. Sufficient dc gain of the opamp is required to suppress the gain error $V_{\mathrm{resi}}G/(A\beta_{\mathrm{FA}})$ within $1/2^8V_{\mathrm{FS}}$ (the 8× residue gain relaxes the accuracy requirement of the second-stage SAR from $1/2^{11}V_{\mathrm{FS}}$ to $1/2^8V_{\mathrm{FS}}$). Consequently, with $V_{\mathrm{resi}} < 1/2^6V_{\mathrm{FS}}$ after first-stage 6-b quantizing, G of 8 and β_{FA} of 1/8, A must not be less than 48 dB. However, considering the residue gain errors caused by the opamp's input parasitic that degrades the feedback factor as well as the memory effect, adequate design margin is required.

With an overall conversion speed of 160 MHz, the final settling error of the opamp's output must be less than $1/2^8V_{\mathrm{FS}}$ at the end of the amplification period of 6.2 ns. Correspondingly, the GBW of this design should be >712 MHz.

The 8× inter-stage gain is designed corresponding to the power optimization of the opamp and the second-stage SAR. Table II illustrates the design tradeoffs between the opamp's requirement and second-stage conversion accuracy with respect to different residue gain. The opamp's power is estimated in a telescopic configuration and its output loading maintains the same value due to limited unit capacitance of the second-stage 6-b DAC. The lower inter-stage gain improves the feedback factor relaxing the opamp's GBW as target for the same closed-loop bandwidth. Therefore, power dissipation can be significantly reduced. However, the reduction of inter-stage gain demands the higher conversion accuracy of the second-stage SAR ADC as well as the offset and gain mismatches requirements. Compared with the design of the opamp, a medium resolution (< 9 b) high-speed SAR ADC is comparatively easy to achieve with very low power dissipation. Because it is digital and the switching power remains constant as a result of performing equivalent number of bit cycling, only the analog power from the comparator increases according to the desired conversion accuracy, which is dynamic and much lower than the one required by the opamp. Another benefit of implementing a lower residue gain is the reduction of the output swing of the opamp, which allows for low-power and high-speed topology as in the telescopic configuration to be used. Consequently, this design uses an 8× residue gain to balance the power drawn by the opamp and the second-stage SAR, which allows the pipelined-SAR architecture to achieve both high conversion speed and efficiency.

IV. CIRCUIT DESCRIPTION

A. First-Stage Capacitive DAC With Decoupled Flip-Around MDAC

Fig. 2 shows the first-stage SAR architecture with the residue amplification. There are two binary-weighted arrays of capacitors $\mathrm{DAC_C}$ (conversion) and $\mathrm{DAC_A}$ (amplification). Indeed, $\mathrm{DAC_A}$ also serves during the conversion phase to attenuate the used reference voltage by a factor of 2. Since the desired $\mathrm{V_{ref}} = \mathrm{V_{DD}}/2$, the method enables us to use the supply voltage and avoid power hungry generation of $= \mathrm{V_{DD}}/2$, which is similar to what was done in [11], [15]. The $\mathrm{DAC_C}$ array uses 64 unity elements; $\mathrm{DAC_A}$ also has 64 elements to attain the 2× attenuation. For amplification, 16 elements of $\mathrm{DAC_A}$ are flipped around the opamp to realize the $128/16 = 8$ amplification.

After the 6-b SA conversion, amplification occurs thanks to the flip-around MDAC. Forty-eight elements remain in the nonfeedback, and the other 16C are fed back to the opamp's output. The residue amplification solely depends on the ratio of $\beta =$

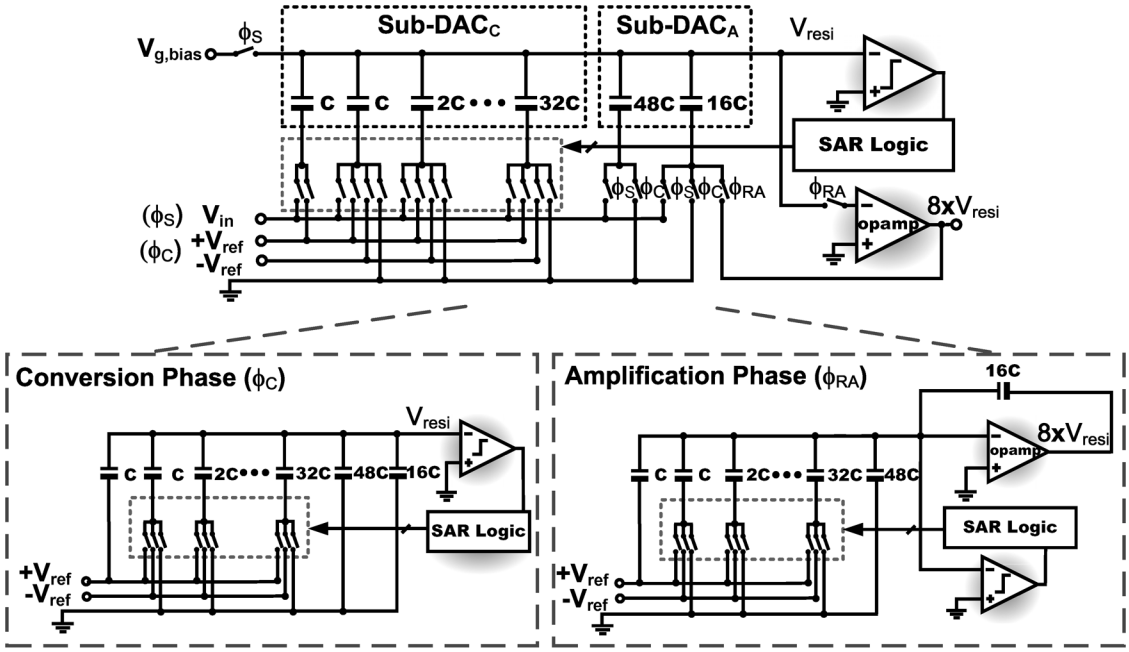


Fig. 2. First-stage SAR ADC architecture with decoupled flip-around MDAC.

$16\mathrm{C}/\mathrm{C}_{\mathrm{sum,first}} = 1/8$ (the total capacitance of the first-stage CDAC $\mathrm{C}_{\mathrm{sum,first}}$ is 128C). The flip around MDAC method is, generally speaking more effective than the nonflip-around one. It reduces the total number of capacitors because a fraction of the array serves as feedback element. Power is reduced because the feedback factor is more favorable and part of the charge is already on the fraction of the array connected in feedback. In traditional flip-around MDAC design [13], the amplification factor of 8 is heavily linked on the use of a maximum 3-b capacitive DAC array in the sub-SAR conversion, as a result, an extra 3-b resistive DAC is required to have a 6-b sub-ADC. In this design, only the partial feedback capacitor (16C) is flipped, so this decoupled the link between the sub-DAC and the amplification factor, allowing a complete 6-b CDAC implementation.

The gain mismatch between two TI channels is determined by the inherit capacitor matching of the first-stage CDAC. The value of the unit capacitor is 13 fF ($5.6\ \mu\mathrm{m} \times 5.6\ \mu\mathrm{m}$) leading to the total sampling capacitance of 1.66 pF single-ended, which only complies with matching requirements as in Section III-A. The DAC array was built based on a sandwich capacitor consisting of three metals layers: M2 and M4 for the bottom-plate and M3 for the top-plate. The bottom-plate enclosing the top-plate minimizes parasitic capacitance, which yields smaller capacitance per unit area with higher matching accuracy than the finger structure [20].

B. Second-Stage Capacitive DAC With V_{DD}*-Attenuator*

The $\times 8$ inter-stage gain makes the residue range equal to 1/8 of the overall input signal. Thus, considering the 1 b used for digital error correction, the reference voltages of the second stage must be 1/4 of the ones of the first stage. To generate the second-stage reference voltage of $\mathrm{V}_{\mathrm{DD}}/8$, the CDAC in the second stage employs a capacitive attenuator as shown in Fig. 3. The first split-stage scales down the reference as required by a lower inter-stage gain of 8, and the 7-b split-DAC determines the fine 5-b output with an extra 2 b for offset cancellation, as will be described later. Normally, the 7-b DAC array connected in series with the attenuation capacitor $\mathrm{C}_{\mathrm{att}}$ of 64/31C results in equivalent output capacitance $\mathrm{C}_{\mathrm{out}}$ of 2C. The total equivalent capacitance C_{eq} of the DAC is 16C. Therefore, the first-split stage operates as a voltage-divider that scales down the reference voltage at the comparator's input by 8. However, the parasitic capacitances of the internal and external nodes of the DAC array cause an inter-stage gain error. This limit is affordable and its contribution is analyzed in the Appendix. The total capacitance needed to fulfill the second-stage kT/C noise limit is 177 fF with a unit capacitance of 10.53 fF ($5\ \mu\mathrm{m} \times 5\ \mu\mathrm{m}$). The value of the capacitance of $\mathrm{C}_{\mathrm{att}}$ ($8.9\ \mu\mathrm{m} \times 8.9\ \mu\mathrm{m}$ equivalent to 31.25 fF) is sized larger to compensate for the gain error caused by the top-plate parasitic of the CDAC.

As shown in Fig. 3, the residue is sampled at the top-plate of the DAC during the residue amplification phase (Φ_{RA}). The switch S_{A} is sized small to reduce signal-dependent charge injection. Assuming that all the channel charge of the switch is injected to the second-stage DAC, the worst error difference between two samples can be calculated as

$$|\Delta V| = \left| \frac{C_{\mathrm{SW}}(V_{\mathrm{DD}} - V_{TH} - V_{\mathrm{in,max}})}{C_{\mathrm{eq}}} - \frac{C_{\mathrm{SW}}(V_{\mathrm{DD}} - V_{\mathrm{TH}} + V_{in,min})}{C_{\mathrm{eq}}} \right| = \frac{C_{\mathrm{SW}} V_{\mathrm{op,p-p}}}{C_{\mathrm{eq}}} \quad (5)$$

where C_{SW} representing WLC_{ox} is the channel capacitance of S_{A}. The output swing of the opamp $V_{\mathrm{op,p-p}}$ is $1/8\mathrm{V}_{\mathrm{FS}}$, and the output equivalent capacitance of the DAC C_{eq} is 177 fF. To guarantee the conversion accuracy, $|\Delta V|$ needs to be restricted to $<$8b. Accordingly, the C_{SW} needs to be $<$5 fF. In this design,

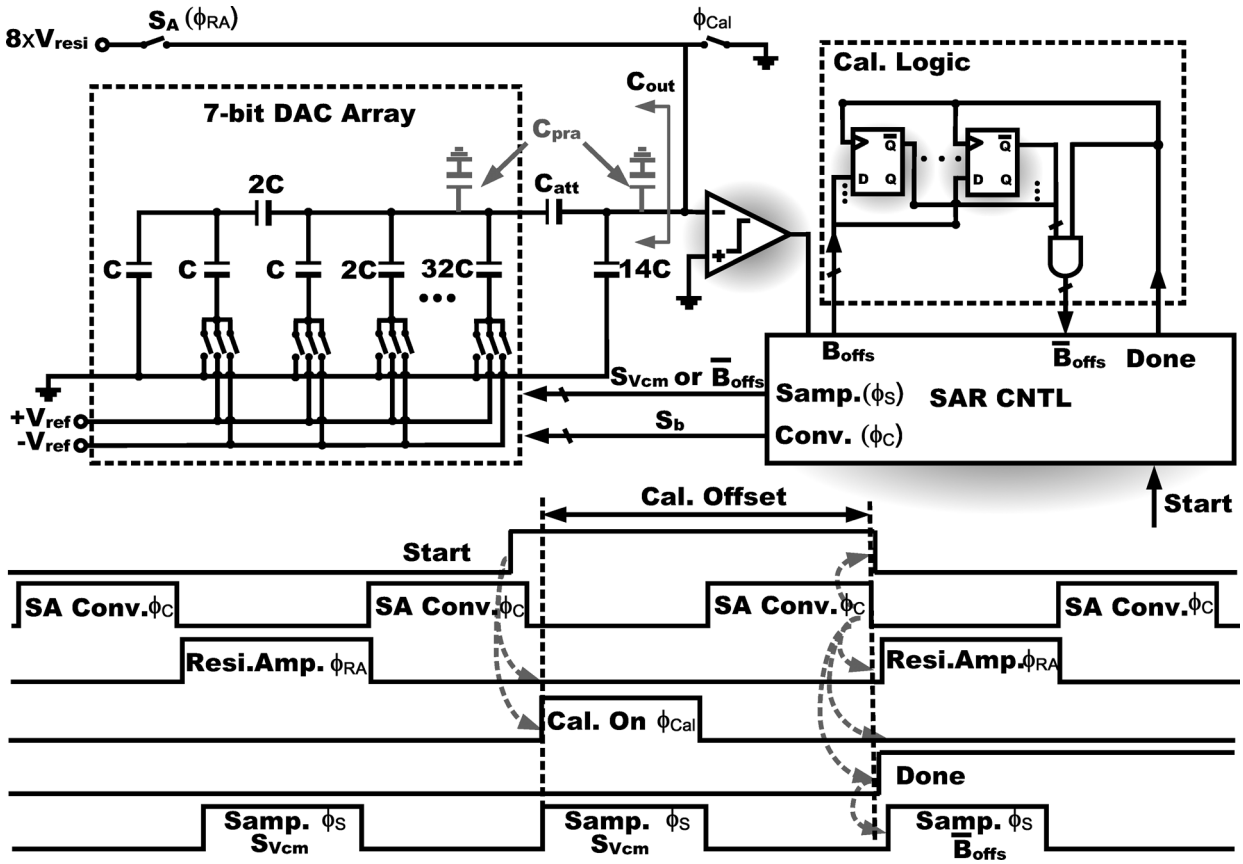


Fig. 3. Second-stage SAR ADC architecture and calibration timing diagram.

an NMOS switch sized with (W/L) of $(0.54\ \mu\text{m}/0.06\ \mu\text{m})$ is used that leads to a C_{SW} around 3.6 fF. The large *RC* time constant of the second-stage sampling network is not problematic as the amplification phase of 6.2 ns is sufficient for the settling as the second-stage residue swing is small.

C. Offset-Cancellation Technique

Fig. 3 shows block and timing diagrams of the second-stage SAR ADC implementing the offset-cancellation technique. It is a 7-b split DAC array used for both conventional SA conversion and offset measurement. In the calibration mode, the input of the stage is set to zero. The conversion accuracy of the second-stage SAR ADC is 9 b, which is within the corresponding offset requirement. The offset value is stored on a memory and subtracted later during normal SA conversion. As Fig. 3 outlines when calibration is not active $(\text{Start} = 0)$, the residue is sampled at the top-plate of the DAC by connecting its bottom-plate to ground during phase (Φ_{S}). When calibration is active $(\text{Start} = 1)$, the residue amplification phase (Φ_{RA}) is disabled. Both top- and bottom-plates of the DAC are reset to ground. Since there is no initial charge in the capacitive array, two inputs of the comparator are set to zero. After 7-b conversion (Φ_{C}) is completed $(\text{Done} = 1)$, the output of the DAC approximates to the comparator offset voltage according to switch control logic S_{b}, which are locked and stored by seven flip-flops as offset code B_{offs}. When the next residue sampling phase Φ_{RA} appears, the offset cancellation is achieved by switching a 7-b complementary offset code at DAC's bottom-plate instead of ground, consequently leading to a value of $8 \times \text{V}_{\text{resi}} - \text{V}_{\text{offs}}$ at the DAC's output for subsequent 5-b SA comparison.

The technique allows an offset cancellation range up to full scale of the second-stage and compensates for the offset with 1/4 LSB accuracy. The calibration logic, consisting of dynamic flip-flops and AND gates, is easily implemented with small area costs.

V. Circuit Implementation

A. Subthreshold Opamp

Fig. 4 shows the circuit schematic of the single-stage opamp along with its biasing circuit that is able to track process variations. Conventional opamp(s) designed in low-voltage nanometer CMOS technologies normally use two-stage architectures. Thanks to the reduced output swing, this design employs a telescopic configuration with a gain-boosting technique. The used currents keep transistors in the subthreshold, thus minimizing overheads and making possible a 1.1-V supply. Because of the subthreshold operation, the V_{GS} of transistor M9C is quite close to the overdrive voltage V_{OD} of M5A. This feature does not increase the headroom as normally required in gain-boosted telescopic opamp(s). Since the opamp gain is in the order of $(\text{g}_{\text{m}}\text{r}_{\text{o}})^3$, transistor lengths can be reduced

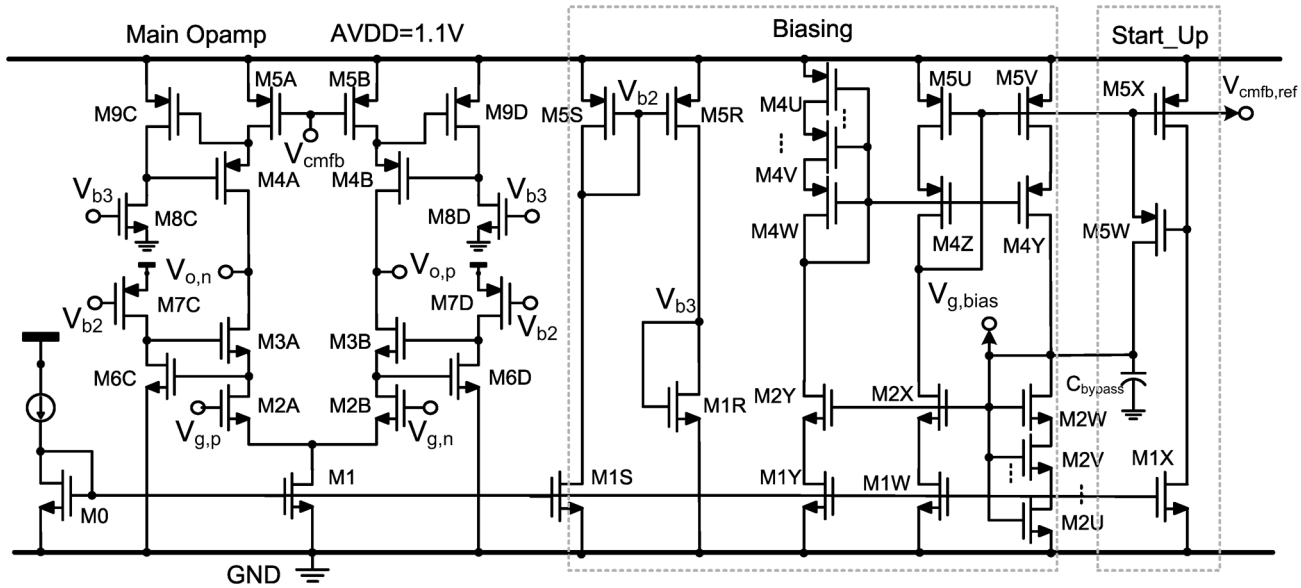


Fig. 4. Circuit schematic of the opamp.

TABLE III
OPAMP'S PERFORMANCE UNDER PROCESS AND TEMPERATURE VARIATIONS WITH AND WITHOUT M2X

Temperature (°C)	Corners	With M2X in biasing network				Without M2X in biasing network			
		GAIN (dB)	GBW (GHz)	PM (°)	$(V_{o,p}+V_{o,n})/2$	GAIN (dB)	GBW (GHz)	PM (°)	$(V_{o,p}+V_{o,n})/2$
27	TT	68	1.44	77	575	62	1.3	75	610
	SS	70	1.36	73	573	65	1.4	67	620
	FF	65	1.56	81	585	56	0.94	82	609
	FS	65	1.38	82	582	54	0.9	85	585
	SF	70	1.58	74	603	67	1.6	69	585
85	TT	59	0.98	77	591	43	0.3	83	675
	SS	64	1.04	82	580	55	0.7	71	673
	FF	52	0.75	74	612	F	F	F	905
	FS	52	0.61	81	623	F	F	F	983
	SF	63	1.3	78	575	56	0.97	72	633
-40	TT	72	1.76	78	565	70	1.77	73	612
	SS	72	1.7	73	565	68.7	1.68	65	631
	FF	72	2	82	567	69	2	81	602
	FS	71	1.9	85	564	67	2.1	85	569
	SF	74	1.8	74	562	74	1.8	71	605

significantly to alleviate the large aspect-ratio requirements of transistors.

The opamp is biased by the process-tracked biasing network that makes the opamp insensitive to the supply, process, and reference current variations under a 1.1-V supply with five stacked transistors. The current in M0 is mirrored to the main opamp in M1, and through the biasing circuit in M1W to the gate of M5U that sets the common-mode feedback (CMFB) reference to M5A, the goal is to make an accurate current matching in the main opamp with $I_{\mathrm{M1}} = 2I_{\mathrm{M5A}}$. To achieve this goal, two techniques are employed. First, it is mandatory to insert an M2X (scaled-down version of diff-pair M2A) on top of M1W. This ensures that the drain voltages of M1 and M1W are identical, and this current sets the reference to $\mathrm{V_{cmfb,ref}}$ thus making the main op-amp's upper and lower current branch equal over process variations. Second, the gate $(\mathrm{V_{g,bias}})$ of M2X is made process-tracked by M2W, M2V that help suppress the absolute current variation in M1W, and this $\mathrm{V_{g,bias}}$ is used to also set the opamp input common-mode through the capacitive DAC in Fig. 2.

Table III exhibits the simulated operating points over process variation for the opamp, compared with and without the usage of M2X. It is clear that the opamp without M2X failed to operate in certain corners (85 °C FF and FS) since the reference current in the upper branch of the opamp is set as too large, such that the CMFB pulls the output common mode up to over 900 mV (this also demonstrates the difficulties in biasing a telescopic opamp under 1.1 V without any special techniques); while with

the usage of the M2X the opamp can be reasonably operated over all corners with the output common-mode properly set (this means that the upper and lower current branches in the opamp are quite well set).

Two main issues drive the design of the process-tracked biasing networks. First, the biasing circuit (the middle part of the opamp in Fig. 4) forms a self-biased loop that may fail to operate under the condition of $I_{\mathrm{D,M1W}} = I_{\mathrm{D,M2W}} = 0$. This occurs when the node $V_{\mathrm{g,bias}}$ is not properly set and pushes the $\mathrm{V_{DS}}$ of M1W all the way down to zero, even if the reference current is presented. The transistor M5X in startup circuit detects this zero-current condition and trigger M5W that shorts the nodes $\mathrm{V_{cmfb,ref}}$ and $\mathrm{V_{g,bias}}$. This action pulls the $\mathrm{V_{cmfb,ref}}$ down and $\mathrm{V_{g,bias}}$ up, thus forcing current to flow in M5U and M5V; b) The two feedback loops in the main opamp and the biasing circuit, the normal negative feedback (the main CMFB) that controls the current sources M5A and M5B, and the positive feedback possibly appearing when the $\mathrm{V_{g,bias}}$ drops, and the drain voltage of M1W drops, thus reducing the current in M1W and eventually M5V (due to the channel-length modulation, CLM), which further exacerbates the decrease in the $\mathrm{V_{g,bias}}$. The positive feedback is very weak in traditional long-channel devices but can be noticeable in nanometer CMOS opamp designs. Therefore, the channel length of M1W must be sufficiently enough to suppress CLM-induced positive feedback opposing the normal negative one. As shown in Table III, the open-loop gain and GBW of the designed opamp are sufficiently large to cover all of the process and temperature variations, as well as residue gain errors due to its input parasitic and memory effect. The gain boosting circuit consumes only 48 μA current, which is 7% of the opamp's total current 700 μA.

The offset of the shared opamp is not cancelled. However, its value gives rise to conversion distortion. This design obtains a 3σ input-referred opamp's offset $\mathrm{V_{offs,opm}}$ well within 7 b, which is achieved by using a large input differential pair operating in the subthreshold region.

B. Comparator and Clock Generator

The comparators [21] used in this work are differential pair dynamic comparators without pre-amplifier. Fig. 5 shows the circuit schematic for first-stage SA comparison. During the reset phase $(\mathrm{STROBE} = 0)$, the transistor M11 is switched off and the relevant nodes are reset to cancel the memory of the previous status. When the regeneration phase $(\mathrm{STROBE} = 1)$ starts, M11 is switched on and input transistors M1–M2 force currents through the back-to-back inverters M3–M5 and M4–M6, which are connected in series with M1–M2 amplifying the input difference to a full swing.

The use of very small transistors minimizes the parasitic, thus obtaining a very high speed even with one LSB imbalance at the input. However, a small area of the transistors' gate give rise to large mismatches and, consequently, a large input referred offset. Fortunately, the used on-chip offset calibration [22] compensates for that limit and allows a very low power implementation of the comparators. The unbalanced capacitive loading method is an effective approach for calibrating the comparator

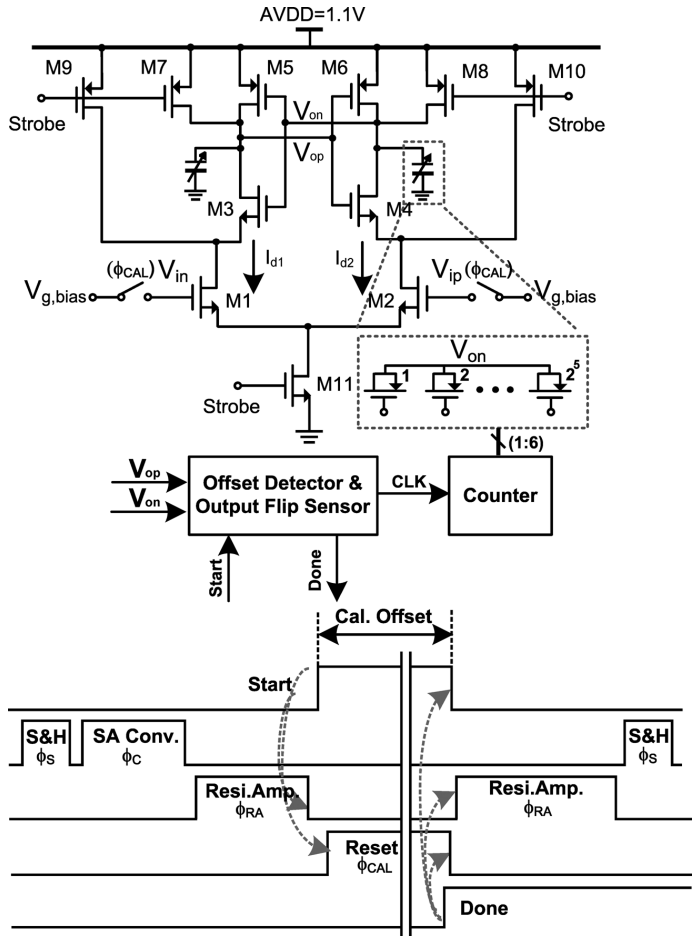


Fig. 5. Circuit schematic of the first-stage dynamic comparator with its offset calibration.

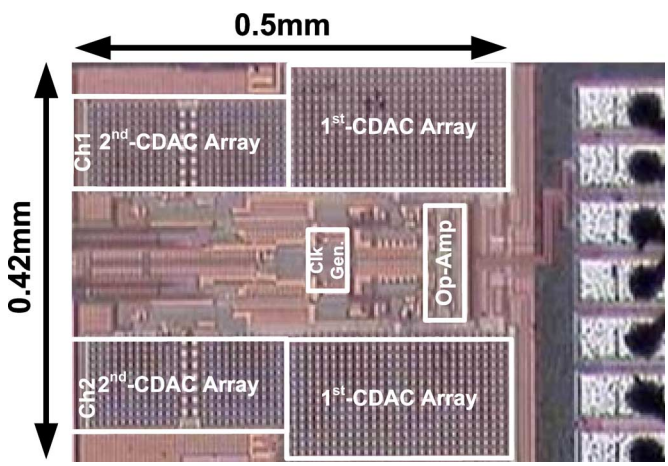


Fig. 6. Die microphotograph of the SAR ADC.

offset. Possible mismatches are corrected by changing the capacitive load of the two branches of the latch. The dynamic behavior is therefore unbalanced as required to compensate for static and dynamic mismatches. During the calibration phase that is performed synchronously on the first and second stages, the inputs are shorted to the reference voltage. Under matched conditions the output would be meta-stable. On the contrary,

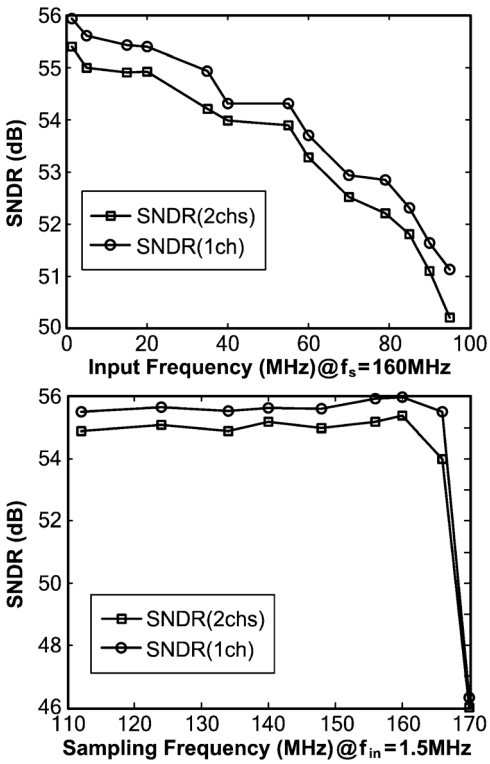


Fig. 7. Measured dynamic performance of the TI pipelined-SAR ADC.

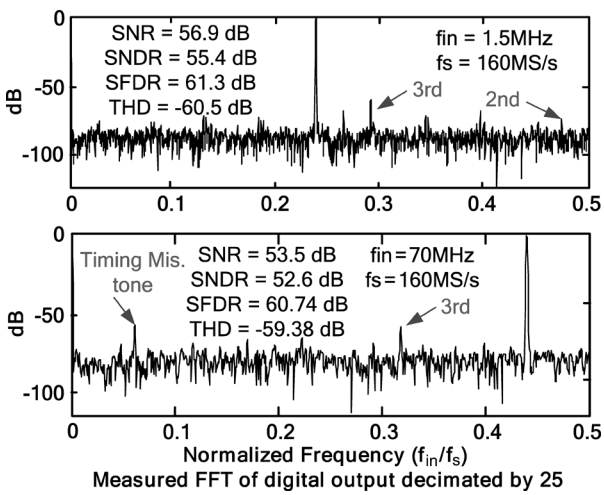


Fig. 8. FFT of the digital output. The input is either a 1.5-MHz or a 70-MHz sine wave sampled at 160 MS/s.

mismatch gives rise to a logic signal. A simple counter that adjusts the binary-weighted capacitor loads uses this signal. The calibration cycle continues until the comparator output changes sign.

A master clock of 160 MHz generates the matched interleaved clock phases through a divider-by-2 low-skew clock generator [23]. The timing skew achieved by this design is 2 ps. The self-timed loop [7] avoids the need of an external fast master clock. The conversion period for one bit cycling is around 800 ps that is sufficient for DAC settling and comparison.

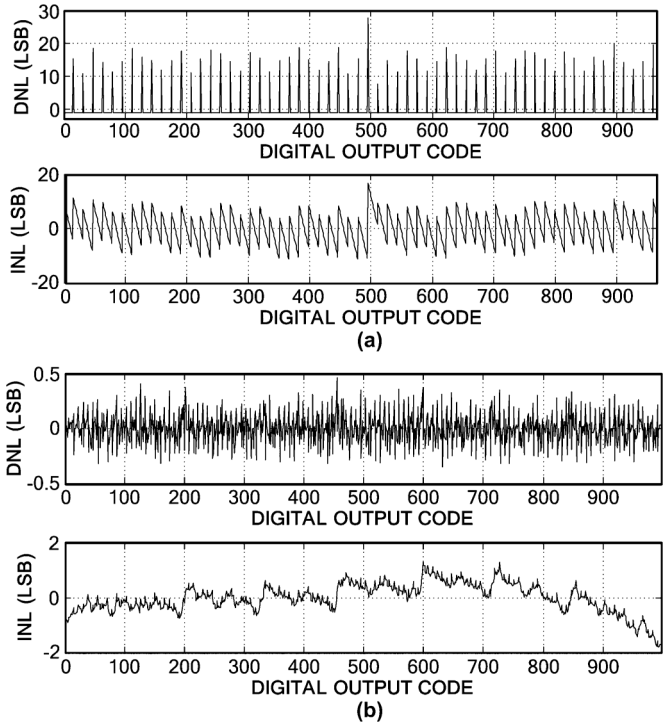


Fig. 9. Measured INL and DNL (a) without offset calibration and (b) with offset calibration.

TABLE IV
SUMMARY OF PERFORMANCE

Technology	65-nm CMOS
Resolution	10-bit
Sampling Rate	160-MS/s
Supply Voltage	1.1-V
Full Scale Analog Input	1.1-V_{PP}
SNDR	55.4dB
SFDR	61.3dB
ENOB	8.9-bit
DNL	+0.46/-0.3LSB
INL	+1.3/-1.7LSB
Analog Power	1.35mW
Digital Power	1.37mW
Total	2.72mW

VI. MEASUREMENT RESULTS

The 10-b TI pipelined-SAR was implemented in 1P7M 65-nm CMOS with a metal–oxide–metal (MOM) capacitor. Fig. 6 shows the die photograph; the active area is 0.21 mm^2. Fig. 7 exhibits the measured dynamic performance of the ADC. The ADC achieves a peak SNDR of 55.4 dB at 1.5-MHz input frequency and 52.6 dB near the Nyquist frequency (70 MHz) with a conversion rate of 160 MS/s and 1.1-V supply. Accounting for the foreseeable inter-stage gain error due to process variation, the expected SNDR degradation is just 0.5 dB without gain calibration. Fig. 8 shows the measured FFT plotted with 1.5- and 70-MHz inputs at 160-MS/s sampling rate. The phase slew error between two channels, including the

TABLE V
COMPARISON WITH STATE-OF-THE-ART WORKS

	[11] VLSI' 10	[12] ISSCC' 10	[14] CICC' 10	[24] ISSCC'07	[25] ISSCC'08	[26] CICC'07	This work
Architecture	Pipelined-SAR	Pipelined-SAR	Pipelined-SAR	Subranging	Pipelined	Pipelined	Pipelined-SAR
Technology (nm)	65	65	65	90	65	65	65
Resolution (bit)	12	10	10	10	11	10	10
Sampling Rate (MS/s)	50	40	204	160	200	125	160
Supply Voltage (V)	1.3	1.1	1	1	1	1.2	1.1
SNDR (dB)@DC	65.5	55.1	55.2	57.1	62.2	57.8	55.4
ENOB (bit)@DC	10.6	8.86	8.87	9.2	10	9.26	8.91
Power (mW)	3.5	1.21	9.15	84	180	20	2.72
FoM =Power/$2^{ENOB@DC}$*f_s (fJ/conv.-step)	46	65	95.4	890	870	270	35
FoM =Power/$2^{ENOB@Nyq.}$*f_s (fJ/conv.-step)	52	89	120	956	1081	N/A	50

timing skew and bandwidth mismatch errors cause the timing mismatch tone higher at high frequency input.

Fig. 9(a) shows static performance when calibration is not active. The differential nonlinearity (DNL) and integral nonlinearity (INL) are quite large at the carry from the second-stage 5-b outputs to the first-stage 6-b outputs as expected. The large quantize tones happen periodically at the positions where the second-stage outputs equal to 11111, which is due to the comparator offsets that cause the second-stage SA comparison saturated. When calibration is active, as shown in Fig. 9(b), the DNL and INL improve from $+27.6/-1$ LSB to $+0.46/-0.31$ LSB and $+16.7$/LSB/-9 to $+1.6/-1.7$ LSB, respectively.

Table IV summarizes the overall measured performance of the ADC. The analog power consumption drawn by the S/H, DAC, comparators, and opamp is 1.35 mW. The digital power consumed by the SAR logic, offset calibration, and clock generator is 1.37 mW. The total power consumption is 2.72 mW at 160 MS/s from a 1.1-V supply. The figure of merit (FoM) calculated as $\mathrm{power}/(2^{\mathrm{ENOB@Nyq}} \times \mathrm{f_s})$ is 50 fJ/conv.-step. Table V illustrates a benchmark with state-of-the-art high-speed ADCs. This work achieves the lowest FoM among pipelined-SAR ADCs, as well as the high-speed ($\mathrm{f_s} > 100$ MS/s) and high-resolution (>10 b) ADCs.

VII. CONCLUSION

A 10-b 160-MS/s TI-pipelined SAR ADC has been presented in this paper. The self-embedded offset cancellation and the design of CDAC arrays for two-stage SAR ADCs have also been addressed. The offset cancellation enables a more relaxed calibration range with less additional calibration effort, thus allowing for the implementation of high-speed and low-power comparators. The CDAC of the first-stage implements both decoupled flip-around MDAC amplification and prevents the use of a power hungry reference generator. The $\mathrm{V_{DD}}$-attenuator used in the second-stage DAC array enables reference-buffer-free operation and establishes a sufficiently low output equivalent capacitance, to improve the bandwidth of the opamp. The ADC achieves 8.9-b ENOB without gain calibration. The prototype ADC draws only 2.72-mW power from the 1.1-V supply and exhibits an FoM of 50 fJ/conv.-step.

APPENDIX

The top-plate parasitic of the second-stage CDAC with $\mathrm{V_{DD}}$-attenuator causes an inter-stage gain error that is analyzed as follows. Fig. 10 shows the 5-b CDAC used in the second-stage SAR ADC, where an extra 2 b for offset cancellation is not considered. The output of the DAC including its top-plate parasitic can be expressed as shown in (A1) at the bottom of the page, where C_{Sum} equal to $64C$ is the sum of internal array capacitance, and S_n equal to "1" or "0" is the bit decision of each comparison. Assuming that the top-plate parasitic of each unit is αC, C_{P1} and C_{P2} representing the sum of the array's top-plate parasitic are $64\alpha C$ and $14\alpha C$, respectively (the parasitic of C_{att} is neglected here). The parasitic C_{P1} and C_{P2} appearing in the denominator are S_n independent, thus only contributing to the gain error. As a consequence, the normalized gain error can be expressed as

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{out,id}}} = \frac{78C_{\mathrm{att}}C + 896C^2}{78C_{\mathrm{att}}C(1+\alpha) + 896C^2(1+2\alpha+\alpha^2)}$$

$$V_{\mathrm{out,id}} = \frac{C_{att} \times \sum_{n=1}^{i} S_n C_n}{78C_{\mathrm{att}}C + 896C^2}. \tag{A2}$$

$$V_{\mathrm{out}} = \frac{C_{\mathrm{att}} \times \sum_{n=1}^{i} S_n C_n}{C_{\mathrm{att}} \times (C_{\mathrm{Sum}} + C_{P1} + 14C + C_{P2}) + (C_{\mathrm{Sum}} + C_{P2})(14C + C_{P1})} V_{\mathrm{ref}} \tag{A1}$$

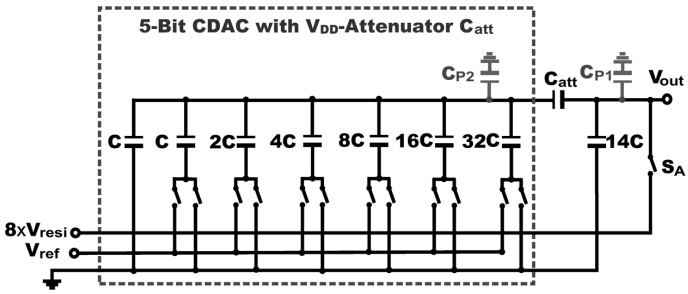


Fig. 10. A 5-b capacitive DAC array with $\mathrm{V_{DD}}$-attenuator $\mathrm{C_{att}}$ to divide the reference voltage by 8.

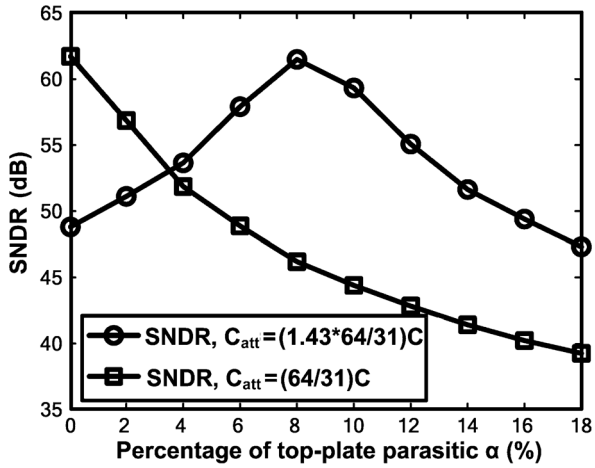


Fig. 11. SNDR versus the top-plate parasitic α in a 10-b TI-pipelined-SAR (w/& w/o compensated $\mathrm{C_{att}}$).

Since the term α^2 in the denominator is quite small, (A2) can be simplified as

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{out,id}}} \approx \frac{78C_{\mathrm{att}} + 896C}{78C_{\mathrm{att}}(1+\alpha) + 896C(1+2\alpha)} \approx 1 - \frac{78\alpha C_{\mathrm{att}} + 1692\alpha C}{78C_{\mathrm{att}}(1+\alpha) + 896C(1+2\alpha)}. \quad \text{(A3)}$$

The value of α needs to be determined so that the V_{out} deviation from $V_{\mathrm{out,id}}$ can be less than $1/2^8$. Accordingly, the error term V_{error} can be written as

$$V_{\mathrm{error}} = \frac{78\alpha C_{\mathrm{att}} + 1792\alpha C}{78C_{\mathrm{att}}(1+\alpha) + 896C(1+2\alpha)} V_{\mathrm{out,id}} < \frac{1}{2^8}. \quad \text{(A4)}$$

As the full-scale of $V_{\mathrm{out,id}}$ is $1/2^3$, with the attenuator C_{att} of 64/31C, it can be obtained that α should be suppressed to less than 1.7%. Fig. 11 plots the result of SNDR versus α in a 10-b TI-pipelined-SAR ADC. Since the drop of the performance is large even with relatively small parasitic it is necessary to compensate for the limit. After layout routing, the layout extraction tools show that the top-plate parasitics of C_{P1} and C_{P2} is around 15 and 56 fF, respectively, which approximates to α of 8%. Therefore, to compensate for the inter-stage gain error, it is necessary to increase the capacitance of $C_{\mathrm{att}}\eta$ times according to

$$\frac{\eta C_{\mathrm{att}} \times \sum_{n=1}^{i} S_n C_n}{\eta C_{\mathrm{att}} \times (78C+78\alpha C)+(64C+14\alpha C)(14C+64\alpha C)} = V_{\mathrm{out,id}} \quad \text{(A5)}$$

giving η equal to 1.43. Therefore, the capacitance of C_{att} equal to 31.25 fF becomes 1.43 times larger than its nominal value. Considering the mismatch and process variation, the split structure can be implemented in medium resolution. For higher accuracy, gain calibration would be required.

ACKNOWLEDGMENT

The authors would like to express their sincere appreciation to H.-L. Choi for valuable support in the measurement and H. Venkatesan for the English revision.

REFERENCES

[1] I. Ahmed, J. Mulder, and D. A. Johns, "A 50 MS/s 9.9 mW pipeline ADC with 58 dB SNDR in 0.18 μm CMOS using capacitive charge-pumps," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 164–2165.

[2] K. Honda, M. Furuta, and S. Kawahito, "A low-power low-voltage 10-bit 100-MSample/s pipeline A/D converter using capacitance coupling techniques," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 757–765, Apr. 2007.

[3] S. T. Ryu, B. S. Song, and K. Bacrania, "A 10-bit 50-MS/s pipelined ADC with op-amp current reuse," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 475–485, Mar. 2007.

[4] B. Murmann and B. Boser, "A 12b 75 MS/s pipelined ADC using open-loop residue amplification," in *ISSCC Dig. Tech. Papers*, Feb. 2003, pp. 328–329.

[5] W. Liu *et al.*, "A 12b 22.5/45 MS/s 3.0 mW 0.059 mm^2 CMOS SAR ADC achieving over 90 dB SFDR," in *ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 380–381.

[6] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 μm CMOS process," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2009, pp. 236–237.

[7] Y. Zhu *et al.*, "A 10-bit 100 MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[8] C. C. Liu *et al.*, "A 10b 100 MS/s 1.13 mW SAR ADC with binary-scaled error compensation," in *ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 368–369.

[9] M. van Elzakker *et al.*, "A 1.9 μW 4.4 fJ/conversion-step 10b 1 MS/s charge-redistribution ADC," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 244–610.

[10] V. Giannini *et al.*, "An 820 μW 9b 40 MS/s noise-tolerant dynamic-SAR ADC in 90 nm digital CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 238–610.

[11] C. C. Lee and M. P. Flynn, "A 12b 50 MS/s 3.5 mW SAR assisted 2-stage pipeline ADC," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2010, pp. 239–240.

[12] M. Furuta, M. Nozawa, and T. Itakura, "A 0.06 mm^2 8.9b ENOB 40 MS/s pipelined SAR ADC in 65 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 382–383.

[13] S.-W. Sin *et al.*, "An 11b 60 MS/s 2.1 mW two-step time-interleaved SAR-ADC with reused S&H," in *ESSCIRC Dig. Tech.Papers*, Sep. 2010, pp. 218–221.

[14] Y.-D. Jeon *et al.*, "A 9.15 mW 0.22 mm^2 10b 204 MS/s pipelined SAR ADC in 65 nm CMOS," in *CICC Dig. Tech. Papers*, Oct. 2010, pp. 1–4.

[15] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto, "A 10b 50 MS/s 820 μW SAR ADC with on-chip digital calibration," in *ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 384–385.

[16] Y. F. Chen *et al.*, "Split capacitor DAC mismatch calibration in successive approximation ADC," in *Proc. IEEE CICC*, Sep. 2009, pp. 279–482.

[17] C. H. Chan *et al.*, "A threshold-embedded offset calibration technique for inverter-based flash ADCs," in *Proc. IEEE MWSCAS*, Aug. 2010, pp. 489–492.

[18] Y. Zhu *et al.*, "A 35 fJ 10b 160 MS/s Pipelined-SAR ADC with decoupled flip-around MDAC and self-embedded offset cancellation," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2011, pp. 61–64.

[19] M. Gustavsson, *CMOS Data Converters for Communications*. Dordrecht, The Netherlands: Kluwer, 2000.

[20] S.-W. Sin *et al.*, "On-chip small capacitor mismatches measurement technique using beta-multiplier-biased ring," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Taipei, Taiwan, Nov. 2009, pp. 49–52.

[21] G. Van der Plas and B. Verbruggen, "A 150 MS/s 133 μW 7b ADC in 90 nm digital CMOS using a comparator-based asynchronous binary-search sub-ADC," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 242–243.
[22] B. Verbruggen *et al.*, "A 2.2 mW 1.75 GS/s 5 Bit Folding Flash ADC in 90 nm Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 874–882, Mar. 2009.
[23] S.-W. Sin, S.-P. U, and R. P. Martins, "A generalized timing-skew-free, multi-phase clock generation platform for parallel sampled-data systems," in *Proc. ISCAS*, May 2004, vol. 1, pp. I-369–I-372.
[24] D. J. Huber and R. J. Chandler, "A 10b 160 MS/s 84 mW 1 V Sub-ranging ADC in 90 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 454–456.
[25] K. W. Hsueh *et al.*, "A 1 V 11b 200 MS/s Pipelined ADC with Digital Background Calibration in 65 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 546–547.
[26] P. N. Singh, A. Kumar, C. Debnath, and R. Malik, "20 mW, 125 Msps, 10 bit pipelined ADC in 65 nm standard digital CMOS process," in *Proc. IEEE CICC*, Sep. 2007, pp. 189–192.

Yan Zhu (S'10–M'12) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau Macao, China, in 2009 and 2011, respectively.

She is now a Postdoctoral Researcher with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China. Her research interests include low-power and wideband high-speed Nyquist A/D converters as well as digitally assisted data converter designs.

Chi-Hang Chan (S'12) received the B.S. degree from the University of Washington, Seattle, and the M.S. degree from the University of Macau, Macao, China, in 2012, where he is currently working toward the Ph.D. degree.

He was an intern with Synopsys-Chipidea Microelectronics, Macau, during his undergraduate studies. His research is mainly focused on gigahertz-range ADCs with low and moderate resolution, comparator, dynamic circuit design, and mixed-signal layout consideration.

Sai-Weng Sin (S'98–M'06) received the B.Sc., M.Sc., and Ph.D. degrees (with highest honor) in electrical and electronics engineering from the University of Macau, Macao, China, in 2001, 2003, and 2008, respectively.

He is currently an Assistant Professor with the Faculty of Science and Technology, University of Macau, Macao, China, and is the Coordinator of the Data Conversion and Signal Processing (DCSP) Research Line in State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. He has published one book, entitled *Generalized Low-Voltage Circuit Techniques for Very High-Speed Time-Interleaved Analog-to-Digital Converters* (Springer) and over 70 technical journals and conference papers in the field of high-performance data converters and analog mixed-signal integrated circuits.

Dr. Sin is/has been a member of the Technical Program Committee of IEEE Sensors 2011 and IEEE RFIT 2011-2012 Conference, Review Committee Member of PrimeAsia 2009 Conference, Technical Program, and Organization Committee of the 2004 IEEJ AVLSI Workshop, as well as the Special Session Co-Chair and Technical Program Committee Member of 2008 IEEE APCCAS Conference. He is currently the Secretary of the IEEE Solid-State Circuit Society (SSCS) Macau Chapter and IEEE Macau CAS/COM Joint Chapter. He was the corecipient of the 2011 ISSCC Silk Road Award, Student Design Contest winner in A-SSCC 2011 and the 2011 State Science and Technology Progress Award (second-class), China.

Seng-Pan U (S'94–M'00–SM'05) received the B.Sc. and M.Sc degree in 1991 and 1997, respectively, and the joint Ph.D. degree (with highest honor) from the University of Macau, Macao, China, the Instituto Superior Técnico, Universidade Técnica de Lisboa (IST/UTL) in 2002 in the field of high-speed analog IC design.

Dr. U has been with the Department of Electrical and Electronic Engineering, Faculty of Science and Technology (FST), University of Macau, Macao, China, since 1994, where he is currently a Professor and Deputy Director of State-Key Laboratory of Analog & Mixed-Signal VLSI of UM. During 1999-2001, he was also on leave to the Integrated CAS Group, Center of Microsystems, IST/UTL, as a Visiting Research Fellow. In 2001, he cofounded the Chipidea Microelectronics (Macau), Ltd., and was Engineering Director and since 2003 the corporate Vice-President of IP Operations Asia Pacific and site General Manager of the company for devoting in advanced analog and mixed-signal Semiconductor IP (SIP) product development. Chipidea group was acquired in May 2009 by Synopsys Inc. (NASDAQ: SNPS), the world leading EDA and IP provider, he is currently the corporate Senior Analog Design Manager and Site General Manager. He holds five U.S. patents and has coauthored *Design of Very High-Frequency Multirate SC Circuits—Extending the Boundaries of CMOS AFE Filtering*, *Analog-Baseband Architectures and Circuits for Multistandard and Low-Voltage Wireless Transceivers*, and *Generalized Low-Voltage Circuit Techniques for Very High-Speed TI ADCs* (Springer), and the foremost one was selected in 2007 by China Science Press for republication in The Overseas Electronics & Information Book Excellence Series."

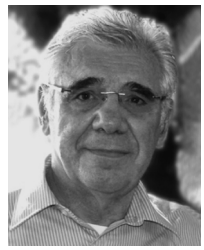
Dr. U has received various scholarship and R&D grants and published more than 120 scientific papers in IEEE/IET journal and conferences. He has received 20+ research & academic/teaching awards and is also the advisor for 20+ various international student paper award recipients, e.g., ISSCC Silk-Road Award, IEEE DAC/ISSCC Student Design Contest, A-SSCC Student Design Contest, ISCAS, MWSCAS, and IEEE PRIME. He also received, at the first time from Macau, the Scientific and Technological Innovation Award of Ho Leung Ho Lee Foundation in 2010, and also The State Scientific and Technological Progress Award in 2011. In recognition of his contribution in high-technology research & industrial development in Macau, he was awarded by Macau SAR government the Honorary Title of Value in 2010. He is currently the Industrial Relationship Officer of IEEE Macau Section, the Chairman of the IEEE Macau CAS/COMM chapter, and also the founding Chairman of the IEEE Macau SSC Chapter. He has been with technical review committee of various international scientific journals and conferences for many years, e.g., JSSC, TCAS, IEICE, ISCAS and etc. He was the chairman of the local organization committee of IEEJ AVLSIWS'04, the Technical Program co-Chair of IEEE APCCAS'08, ICICS'09 and PRIMEAsia'11. He is currently a member of the Technical Program Committee of RFIT, VLSI-DAT, and A-SSCC.

Rui Paulo Martins (M'88–SM'99–F'08) was born on April 30, 1957. He received the B.Sc., M.Sc., and Ph.D. degrees, as well as the Habilitation for Full-Professor, in electrical engineering and computers from Instituto Superior Técnico (IST), TU of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering (DECE)/IST, TU of Lisbon, since October 1980. Since 1992, he has been on leave from IST, TU of Lisbon, and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Full Professor since 1998. At FST, he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment as Vice-Rector (Research) until August 31, 2013. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and has supervised (or cosupervised) 25 theses, Ph.D. (11) and Masters (14). He has published 12 books, coauthoring five and coediting seven, plus five book chapters, 230 refereed papers, in scientific journals and conference proceedings, as well as other 70 academic works, in a total of 317 publications. He has coauthored four U.S. Patents (two issued in 2009 and two in 2011) and with another six pending. He has created the Analog and Mixed-Signal VLSI Research Laboratory of UM, elevated in January 2011 to the State Key Lab of China (the first in Engineering in Macao), being its

Founding Director. He is the financial manager, recognized by the European Union, of a *Jean Monnet Chair* in "*EU Law–Facing the Constitution and Governance Challenges in the Era of Globalization*", unique in the universities from HK & Macao, for the period 2007 to 2012.

Prof. Rui Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and of the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 (2009 World Chapter of the Year of the IEEE Circuits and Systems (CAS) Society). He was the General Chair of the 2008 IEEE Asia-Pacific Conference on Circuits And Systems—APCCAS'2008, and was the Vice-President for the Region 10 (Asia, Australia, the Pacific) of the IEEE CAS Society for the period 2009 to 2011. He was elected recently to the position of Vice-President (World) Regional Activities and Membership also of the IEEE CAS Society for the period 2012 to 2013. He has been an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS since 2010. He was the recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010 he was unanimously elected, as a Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese academician living in Asia.



Franco Maloberti (A'84–SM'87–F'96) received the Laurea degree in physics (*summa cum laude*) from the University of Parma, Parma, Italy, in 1968, and the Dr. Honoris Causa degree in electronics from Inaoe, Puebla, Mexico, in 1996.

He was a Visiting Professor with ETH-PEL, Zurich, in 1993 and with EPFL-LEG, Lausanne, in 2004. He was a Professor of Microelectronics and Head of the Micro Integrated Systems Group University of Pavia, Pavia, Italy, TI/J.Kilby Analog Engineering Chair Professor with the Texas A&M University and the Distinguished Microelectronic Chair Professor with University of Texas at Dallas. Currently, he is a Professor with the University of Pavia, Pavia, Italy, and Honorary Professor with the University of Macau, Macao, China. He has written more than 450 published papers, five books, and holds 30 patents. He has been responsible for many research programs including ten ESPRIT projects and served the European Commission in many European Initiatives. He served the Academy of Finland on the assessment of electronic research. He served the National Research Council of Portugal for the research activity assessment of Portuguese Universities. He was a Member of the Advisory Board of INESC-Lisbon, Portugal. He is the Chairman of the Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China.

Prof. Maloberti was VP Region 8 of the IEEE Circuits and Systems (CAS) Society (1995–1997), Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, President of the IEEE Sensor Council (2002–2003), an IEEE CAS BoG member (2003–2005), and VP Publications for IEEE CAS (2007–2008). He was a Distinguished Lecturer for the IEEE Solid-State Circuits Society (2009–2010) and presently is a Distinguished Lecturer for the IEEE CAS Society. He received the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, and the IEEE Millennium Medal. He received the 1996 IEE Fleming Premium, the ESSCIRC 2007 Best Paper Award and the IEEJ Workshop 2007, and 2010 Best Paper Award. He is IEEE Fellow. In 1992, he was a recipient of the XII Pedriali Prize for his technical and scientific contributions to national industrial production.