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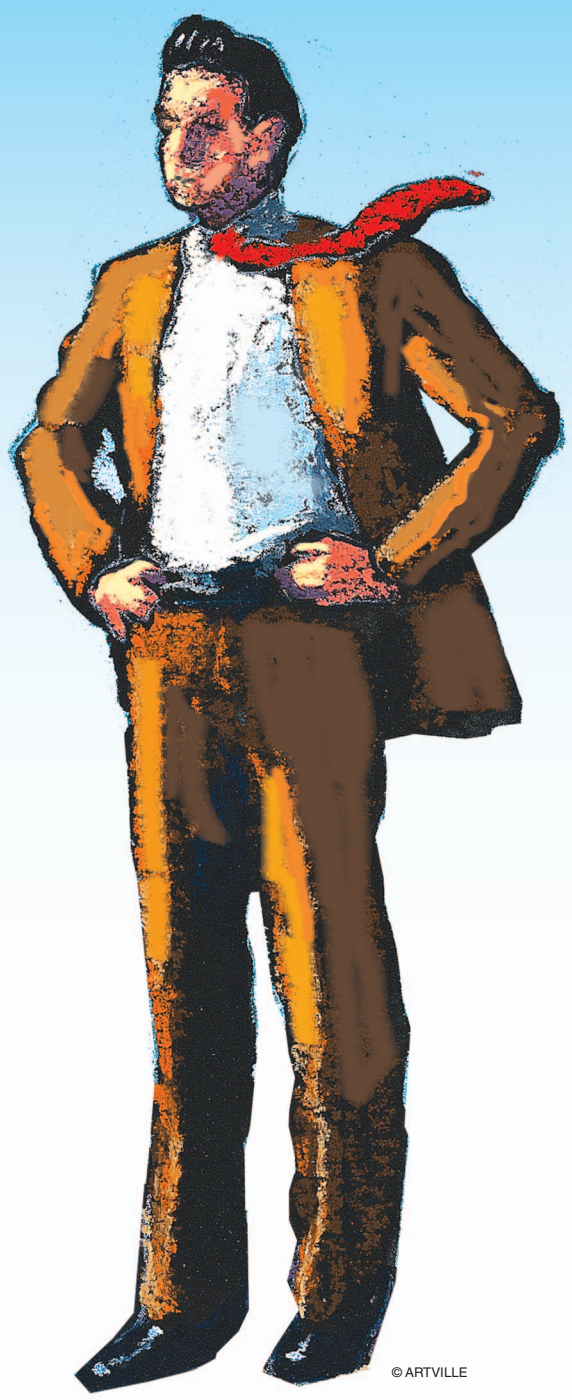
Enhanced RFICs in Nanoscale CMOS



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Wireless and semiconductor industries have recently discussed their vision of fully autonomous and seamless wireless connectivity by combining advanced nanoscale CMOS technologies with innovative hybrid-domain circuits and systems solutions [1]. One goal inside this broad vision is to develop a smart mobile companion device with high performance, adaptive connectivity, and high power efficiency. High performance is the essential ingredient to coping with the ever-increasing add-on functionalities in small handheld devices, integrating cellular, WiFi, Bluetooth, Global Positioning System and mobile TV. All of these generate many opportunities for furthering the

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horizons of radio frequency integrated circuits (RFICs) [2] in the years to come.

RFIC development has trended toward wideband, software-defined radios [3], [4] and cognitive radios [5] that are capable of handling all essential bands in a small die area, thus minimizing parasitic effects and manufacturing costs. Yet, when extracting a weak signal in the range of –80 dBm in the presence of high-power blocking signals of 0 dBm or even higher, dynamic range (DR) requirements of the RFICs are considerable, as shown in Figure 1.

In the nanoscale CMOS regime, enhancing speed is easier than enhancing DR because of a low supply voltage (V_{DD}) with respect to the device threshold voltage (V_T), as shown in Figure 2. As analyzed in [6] and [7], for most analog and RF circuits, preserving performance metrics such as signal to noise and distortion ratio in a newer technology consistently requires extra power to compensate for the loss of voltage headroom. As a result, developing more sustainable circuit techniques capable of surpassing the low-voltage constraints of nanoscale CMOS would be beneficial.

Recent research has already shown benefits from mixed-$V_{DD,}$ mixed-device analog and RF circuits in advancing state-of-the-art performance [8]–[10]. By consciously selecting the available features of advanced fabrication processes, such as thick- and thin-oxide MOSFETs, core V_{DD} and input/output (I/O) V_{DD}, the design flexibility is expanded while also ensuring reliability. This article outlines the system implications of mixed-V_{DD} mixed-device design and discusses the pros and cons of state-of-the-art works. Novel mixed-$V_{DD,}$ mixed-device RFIC design ideas, as well as transceiver architecture, are also introduced.

System Implication of Mixed-V_{DD} Mixed-Device RFICs

The platform of a typical wireless system-on-a-chip (SoC) is depicted in Figure 3. Thin-oxide MOSFET and core V_{DD} ($V_{DD,c}$) directly befit the all digital portions of the SoC. Regrettably, analog and RF circuits, such as the power amplifier (PA) and baseband (BB) operational amplifier (OpAmp), do not work efficiently under such a low $V_{DD,c}$ which, in advanced processes such as 65 and 40 nm, is roughly 0.9–1 V. The tight voltage headroom implies higher design rigidity and less variability margin. For instance, it would be more speed- and power-efficient to utilize cascode amplifiers rather than its cascade counterpart to minimize high-impedance internal nodes [11]. Yet, concerning the voltage swing, the latter becomes mandatory.

In a wireless SoC, there are still many peripherals that do not scale synchronously with CMOS. Thick-oxide MOSFET and high-voltage I/O supply ($V_{DD,I/O}$) are made available by the foundry [12], [13] in nanoscale CMOS technologies to facilitate those high-voltage I/O communications. Therefore,

High performance is the essential ingredient to coping with the ever-increasing add-on functionalities in small handheld devices.

bringing thick-oxide transistors and $V_{DD,IO}$ into the RF and analog design portfolio will not induce, by itself, extra cost because they are generally open for designers. Although thick-oxide transistors exhibit a lower intrinsic cutoff frequency f_t, they are still well suitable for most RFIC in the GHz range.

Thick-oxide MOSFET exhibits similar characteristics to those observed in mature process nodes such as 0.25- and 0.18-μm CMOS with operating voltages of 2.5 and 1.8 V, respectively. Both are much more suitable for large-signal-handling circuits such as the PA. One example is [14], it benefits from the availability of 0.25-μm thick-oxide device and 2.5-V supply, achieving +31-dBm output power with 58% power-added efficiency. Such an internal supply of 2.5 V or 1.8 V can be generated by a 3.6/3.7-V Li-ion battery.

Obviously, circuits built exclusively with pure thick-oxide transistors cannot benefit from the speed

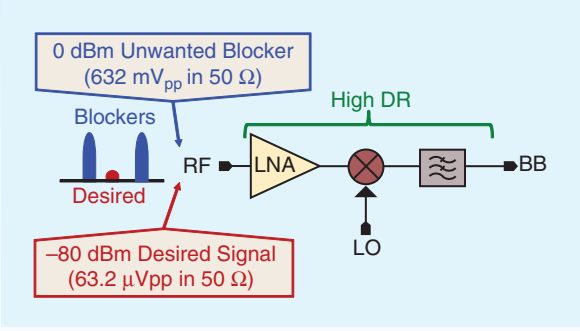


Figure 1. *Wideband receiver with no preselect filtering demands a high DR.*

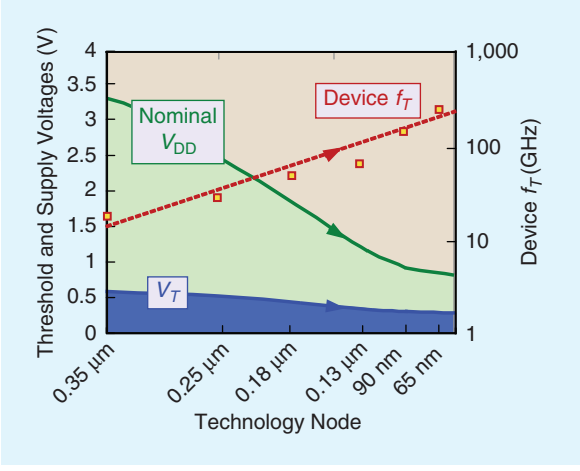


Figure 2. *Technology scaling significantly boosts speed but reduces the voltage headroom.*

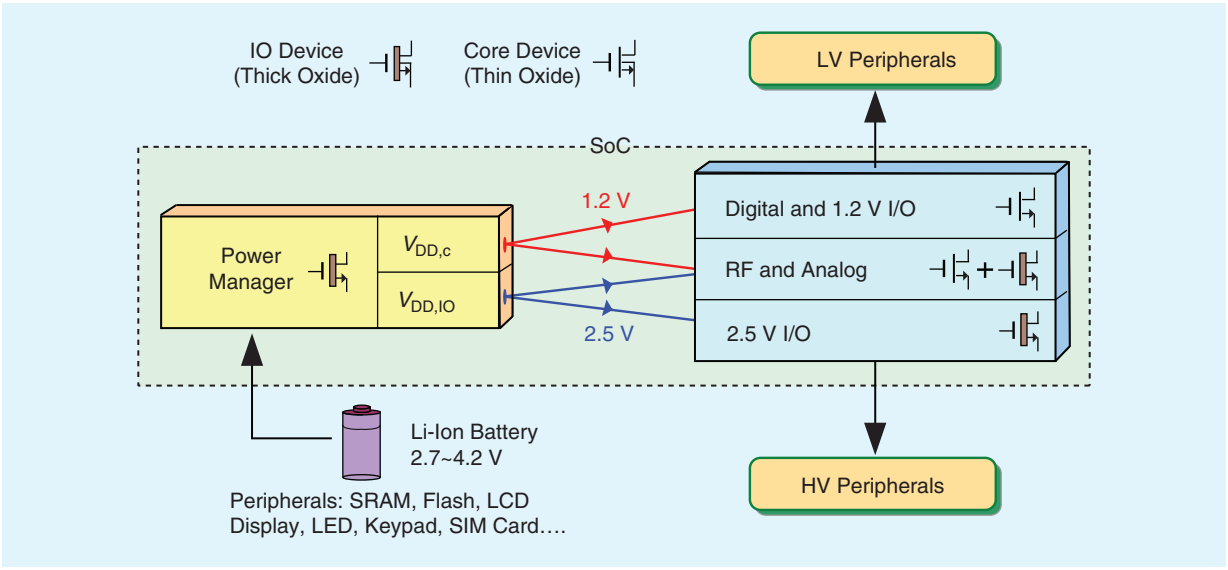


Figure 3. *An SoC in nanoscale CMOS typically offers multiple V_{DD} and device types. The mixed-V_{DD} mixed-device design approach therefore enriches the design flexibility of the RF and analog parts with no extra cost.*

and area advantages of advanced processes. Hybrid use of thin- and thick-oxide MOSFETs, $V_{DD,c}$ and $V_{DD,IO}$, is becoming a new design art of RFICs. In the following section, the fundamental relationship between V_{DD} and the circuit's DR is revisited first.

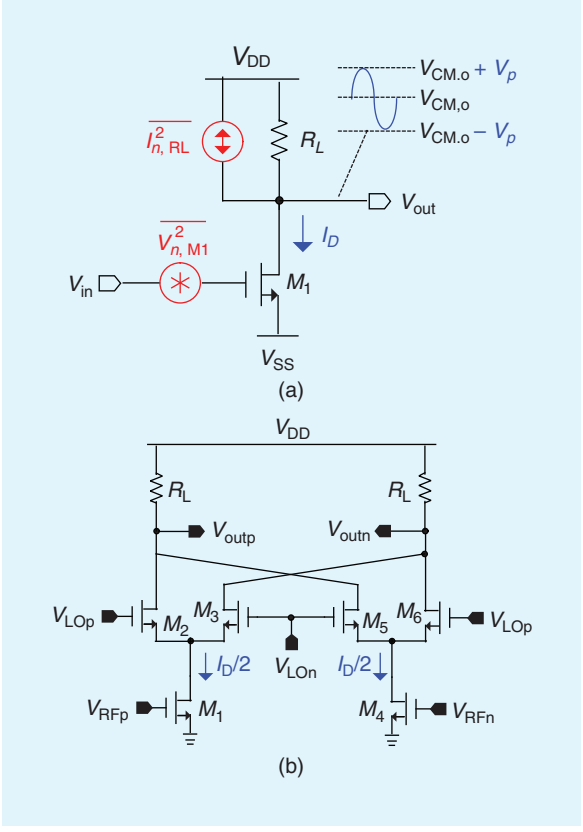


Figure 4. *(a) Typical common-source amplifier and (b) typical active mixer with resistive load.*

V_{DD} and Dynamic Range

The rationale of adopting high-V_{DD} or mixed-V_{DD} on circuit design can be illustrated by analyzing the relationship between the V_{DD} and DR of a common-source amplifier, as shown in Figure 4(a). For simplicity, channel-length modulation is neglected in the calculation. The input-referred noise attributed to M_1 and R_L are given by [11], respectively,

$$\overline{V^2_{n,M1}} = 4kT\frac{1}{g_m}\gamma \text{ and } \overline{V^2_{n,RL}} = \overline{I^2_{n,RL}}\frac{1}{g_m^2} = \frac{4kT}{R_L}\frac{1}{g_m^2}, \quad (1)$$

where γ is the noise factor and g_m is the transconductance of M_1, k is the Boltzmann's constant, and T is the temperature (in Kelvin). The generic current-voltage equation of a MOSFET, considering the mobility degradation parameter θ, is given by,

$$I_D = \frac{1}{2}\frac{W}{L}\mu_o C_{ox}(V_{GS} - V_T)^2\frac{1}{1+\theta(V_{GS}-V_T)}, \quad (2)$$

where W/L is the aspect ratio of the transistor and $\mu_o C_{ox}$ is the transconductance parameter. From (2), the input-referred third-order intercept point (IIP3) of a MOSFET can be approximated by [15],

$$V^2_{IIP3} \approx \frac{8}{3}\frac{V_{GS}-V_T}{\theta} = \frac{16}{3}\frac{I_D}{g_m\theta}. \quad (3)$$

With (1) and (3), the DR of the common source (CS) amplifier can be deduced,

$$DR_{CS} \approx \frac{V^2_{IIP3}}{\overline{V^2_{n,M1}} + \overline{V^2_{n,RL}}} \approx \frac{4}{3}\frac{I_D}{kT\theta\gamma}. \quad (4)$$

In practice, I_D cannot be arbitrarily increased to maximize the DR when there is no voltage headroom since the output common-mode voltage $V_{CM,o}$ must be within V_{DD},

$$V_{CM,o} = xV_{DD} = V_{DD} - I_D R_L, \quad (5)$$

where x denotes a ratio value < 1 and can be set as 0.5 for $V_{CM,o} = V_{DD}/2$, which roughly yields the highest 1-dB compression point (P_{1dB}) [11]. Substituting (5) into (4) yields

$$DR_{CS} \approx \frac{2}{3}\frac{V_{DD}}{R_L}\frac{1}{kT\theta\gamma}. \quad (6)$$

When a high gain is desired, R_L and V_{DD} can be increased together by a factor A so that the DR is maintained, while I_D remains unchanged; the power will only be raised by a factor of A. A similar situation holds for the active mixer shown in Figure 4(b). Its DR can be obtained following the same approach as the CS amplifier

$$DR_{MIXER} \approx \frac{2}{3}\frac{V_{DD}}{R_L}\frac{1}{kT\theta\gamma}\frac{4}{\pi^2}, \quad (7)$$

where the factor $4/\pi^2$ is due to the mixer conversion gain. Obviously, VDD cannot be arbitrarily increased to maximize the circuit's DR due to major device reliability limitations of ultrascaled CMOS processes such as the absolute maximum (voltage) rating, hot carrier injection, negative bias temperature instability, time-dependent dielectric breakdown, and punch-through effect [16]. Boosting the device reliability by transistor stacking can push up drain-source voltage limits. On the other hand, the gate-drain/-source voltages should be controlled via proper bias in all operating modes, active and standby. Though device stacking can simply be based on thin-oxide devices, a hybrid structure of thin- and thick-oxide devices can balance the speed and voltage withstand capability. Their implications should be analyzed according to the actual operation of the circuits. One typical example is a mixed-device PA under an elevated VDD depicted in Figure 5, where a triple well process must be used for the thick-oxide MOS (M2); this is done to ensure that the body-to-well junction is not overdriven. An overdriven junction can suffer from destructive breakdown due to large reverse current flows through the junction.

When the data modulation type and maximum input and output swings are given, a node-voltage trajectory check, using transient simulations, can ensure all devices are operating under their safe operating area [16] at all times, which are bounded by the V_{GS}, V_{GD}, and V_{DS} limits specified in the technology rule manual.

Mixed-V_{DD} Mixed-Device Wireless Circuits

RF Circuits

Cascode building blocks [17], [18] are an effective solution for current reuse and maximizing the bandwidth at RF, as the node between the low-noise amplifier (LNA) and mixer can be of low impedance (Z), as shown in Figure 6. The main shortcomings are the limited reverse isolation between blocks and DR due to insufficient voltage headroom in nanoscale CMOS. Recently, a mixed-V_{DD} design approach [19] has been proposed to alleviate these drawbacks. Both V_{DD25} (I/O V_{DD}) and V_{DD12} ($V_{DD,c}$), thick- and thin-oxide devices are jointly employed, as depicted in Figure 7. The V_{DD25} enlarges the voltage headroom while allowing the bandwidth- or linearity-demanding nodes to be operated in the current domain. Specifically in [19], the balun LNA employs a differential current balancer (DCB) to improve the output gain-phase balancing of the single-to-differential (S2D) stage, yielding better IIP2 and reverse isolation. The key expense will be a high impedance node at RF (V_{RF}) that may limit the RF bandwidth as a tradeoff with the desired gain. With V_{DD25}, the BB lowpass filter (LPF) can be designed in current mode, stacked on top of the mixer. This cascode topology is more efficient than the traditional cascade design in improving out-of-channel linearity, as adequate filtering occurs prior to BB current-to-voltage conversion (at the load). As the multiphase local oscillator generator (LOG) operates as a digital circuit, fabricating it with thin-oxide devices and V_{DD12} ($V_{DD,c}$) will directly benefit the speed, power, and area

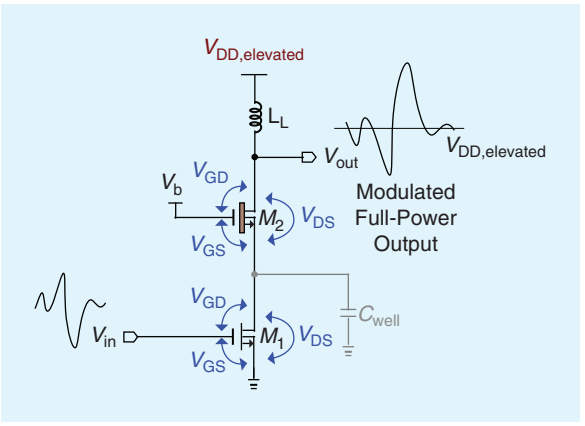


Figure 5. *Reliability tests must follow the application case: a V_{DD}-elevated PA must be tested using the modulated data at full power level to ensure all node voltage trajectories are within their reliability limits.*

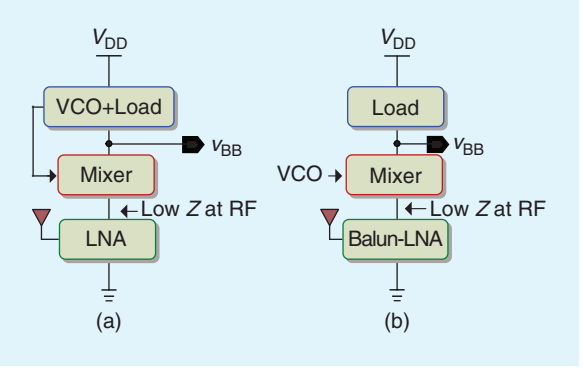


Figure 6. *Single-VDD design with cascoded blocks: (a) LNA-mixer-VCO (LMV) [17] and (b) Blixer [18].*

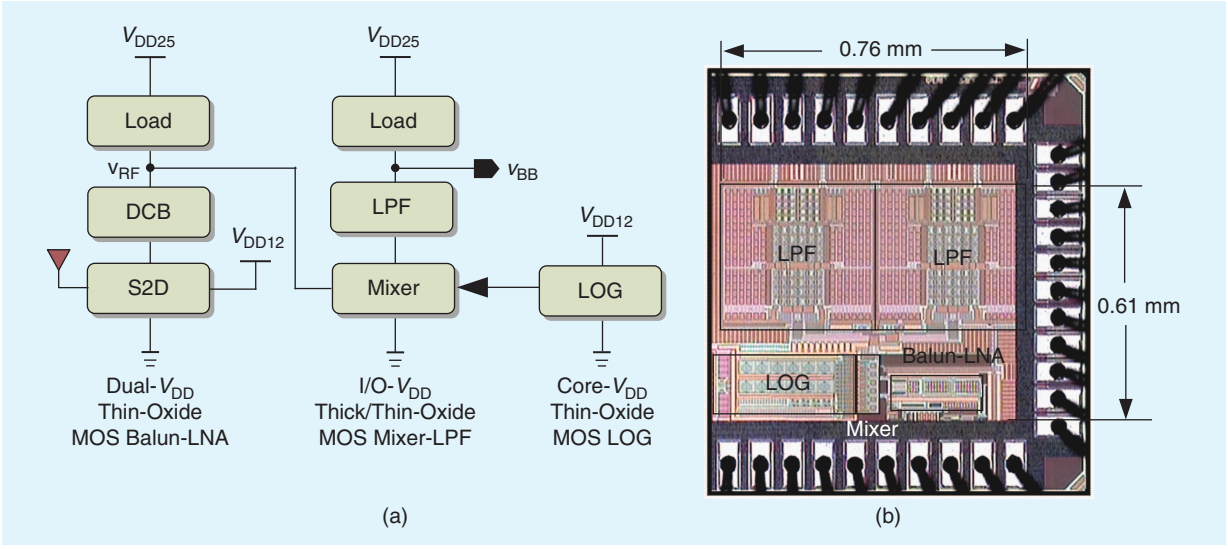


Figure 7. *Mixed-V_{DD} mixed-device design with cascoded blocks for current-mode operation improves linearity, power, and area efficiencies [19].*

advantages of advanced CMOS. The 65-nm chip measured improved performances and area efficiency with respect to the prior arts [20], [21] as shown in Table 1.

Analog-Baseband Circuits

Other research [22] has shown that a $2xV_{DD}$ recycling folded-cascode OpAmp can achieve higher dc gain and close-loop linearity than its $1xV_{DD}$ folded-cascode and $1xV_{DD}$ recycling folded-cascode counterparts under a similar power budget, as summarized in Table 2. The key concept is that when a high V_{DD} is available as shown in Figure 8, more cascode transistors can be added without penalizing the output swing. The cascode transistors not only boost the output resistance (i.e., the voltage gain), but also share the voltage stress from the high V_{DD}, ensuring safe operation of all devices.

TABLE 1. Performance comparison of state-of-the-art wideband RFEs.

Parameters	[19]	[20]	[21]
Operation frequency f_{RF} (GHz)	**0.17–1.7**	0.4–0.9	0.3–0.8
Required master LO frequency f_{LO} (GHz)	**$f_{LO} = f_{RF}$ (four and eight phases)**	$f_{LO} = 8\ f_{RF}$ (eight phases)	$f_{LO} = 4\ f_{RF}$ (eight phases)
Maximum gain (dB)	**35**	34	22–28#
RF gain control (dB)	**17–35**	No	No
External components	**One inductor**	Two inductors and one balun	Two inductors
Area (mm^2)	**0.46**	1	0.5
BB filter order	**Third-order LPF (1 biquad + 1 real)**	LPF (2 real poles)	First-order IIR LPF (minor channel selectivity)
Power (mW) at f_{RF} (GHz)	**55 at 1.7**	60 at 0.9	18 at 0.8
Input impendance matching	**Matched**	Matched	Unmatched
DSB NF (dB)	4 [specification: 4]	4	0.8 to 4.3#
IIP3 (dBm)	–3.4 [specification: –5]	3.5	–1.4 to –9#
IIP2 (dBm)	32 [specification: 27] (Balun LNA)	46 (differential LNA)	38–49# (Balun LNA)
HRR_3 (dB)	35	60	60
HRR_5 (dB)	39	64	60
Supply voltage (V)	1.2 and 2.5	1.2	1.2
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS

(#) – In-band variation

In some cases, standard- and high-V_{DD} building blocks will need to be interfaced. An extra current source, I_b, serving as a level shifter can be employed. The value of I_b, depending on the size of R_i, should be considered when optimizing the noise performance. In a transmitter, the use of 1xV_{DD} and 2xV_{DD} OpAmps allows a progressive increase of linear output swing from the digital-to-analog converter (DAC), as shown in Figure 9(a). For a receiver headed by a low-noise transconductance amplifier (LNTA) and a passive mixer [Figure 9(b)], a 2xV_{DD} OpAmp at the front end offers a wider linear output swing to handle an out-of-channel interferer. A 1xV_{DD} OpAmp at the back end easily interfaces with a 1xV_{DD} analog-to-digital converter (ADC).

After lowpass filtering, the BB signal can be driven off-chip or to the on-chip ADC. In either case, a source follower can be used as the buffer. In a simple 1xV_{DD} design with thin-oxide MOS [Figure 10(a)], a highpass network ($R_{DC}C_{DC}$) is entailed to interface with the source follower to maximize the output swing. As the cutoff of such a highpass network has to be very low to prevent damaging the signal, the chip area is affected by the realization of R_{DC} and C_{DC}. On the other hand, a 2xV_{DD} design with thick-oxide MOS [Figure 10(b)] not only can avoid such a highpass network but also enlarge the linear output swing due to more voltage headroom.

When a high V_{DD} is available, more cascode transistors can be added without penalizing the output swing.

Power Management

Low-dropout regulators (LDOs) are widely employed in SoCs to improve the power-supply rejection ratio (PSRR) of internal circuits. Because of its lower dropout voltage property, the PMOS-based LDO [Figure 11(a)] is more commonly used than its NMOS counterpart

TABLE 2. Design considerations of RF and analog circuits in nanoscale CMOS.

	RF	Analog
Increase Area	• Gain-bandwith (e.g., via inductors)	• Matching (dc-offset) • kT/C noise
Increase Current	• Unity-gain frequency (e.g., higher device f_T)	• Slew rate • Bandwidth
Increase Supply	• Gain (e.g., allows a larger R_L load) • Bandwidth (e.g., cascode of blocks to avoid high impedance nodes) • Dynamic range • Power efficiency (e.g., in PA)	• Gain precision • PSRR (e.g., via LDO) • Dynamic range • Buffering and level shifting in I/Os

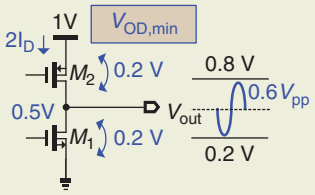
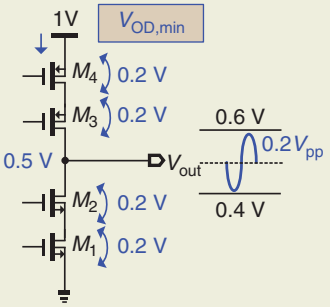
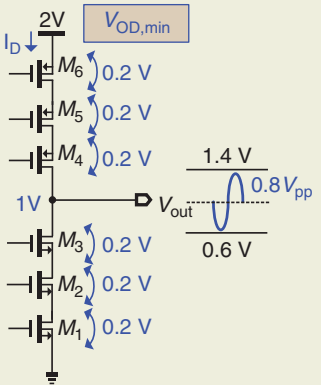
	1V – Non Cascode	1V – Double Cascode	2V – Triple Cascode
			
dc Gain	Low	Medium	High
GBW	High	Medium	Low
Output Swing	Medium	Low	High

Figure 8. *Three possible output stages of an OpAmp with respect to 1-V and 2-V V_{DD}. Comparing with 1-V designs with or without cascode, the 2-V design allows simultaneously higher dc gain and wider output swing given a typical V_{DS} overdrive voltage of 0.2 V.*

With the advance in ADCs, $V_{DD,C}$ can already lead to excellent power efficiency for the requirements of most wireless applications.

[Figure 11(b)]. The main pitfall of the PMOS-based LDO is the necessity of a large external capacitor to ensure stability. Such a large capacitor significantly increases the manufacturing cost and pin counts when many LDOs are entailed. The NMOS-based LDO, however, is free from such a requirement [i.e., capacitorless (cap-less)] and

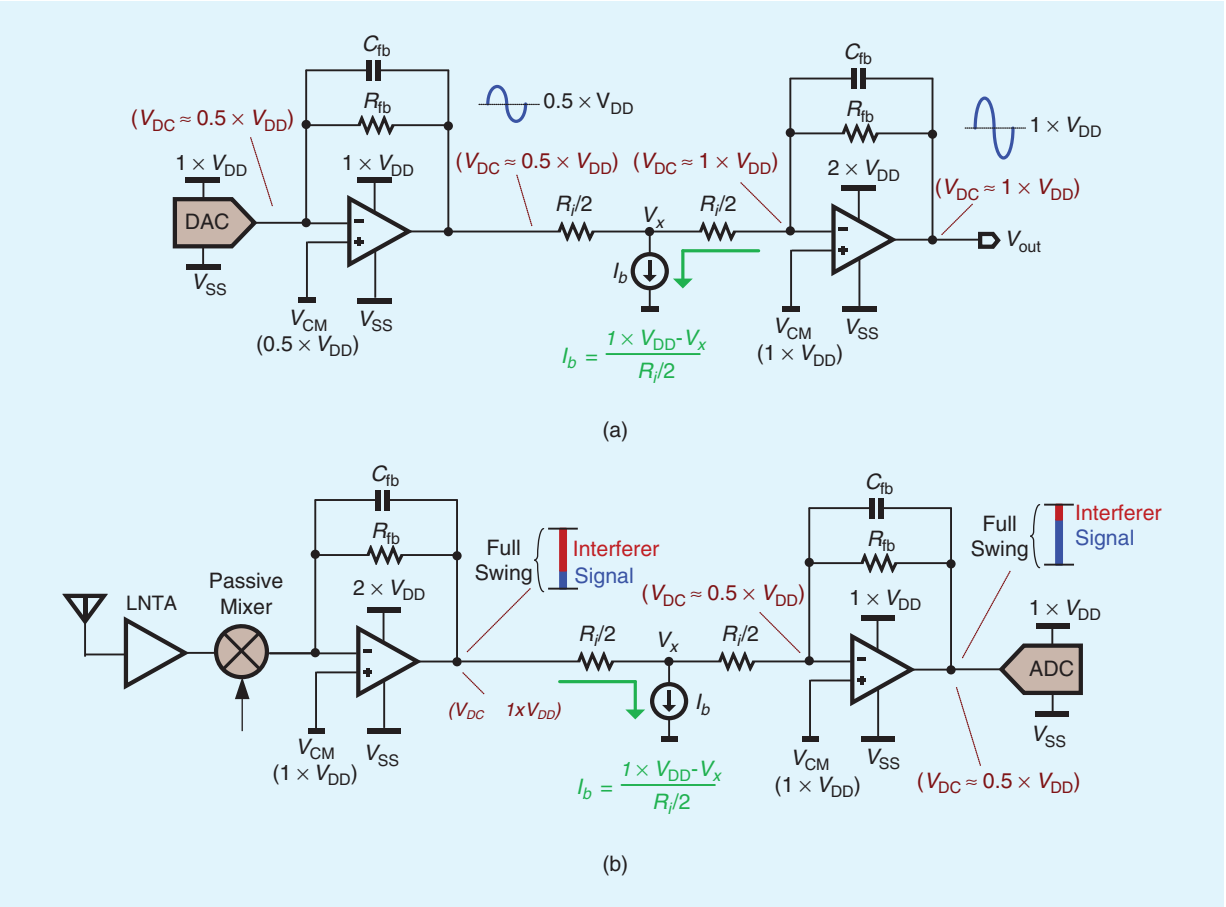


Figure 9. *(a) $1xV_{DD}$ to $2xV_{DD}$ level shifting in a transmitter. (b) $2xV_{DD}$ to $1xV_{DD}$ level shifting in a receiver.*

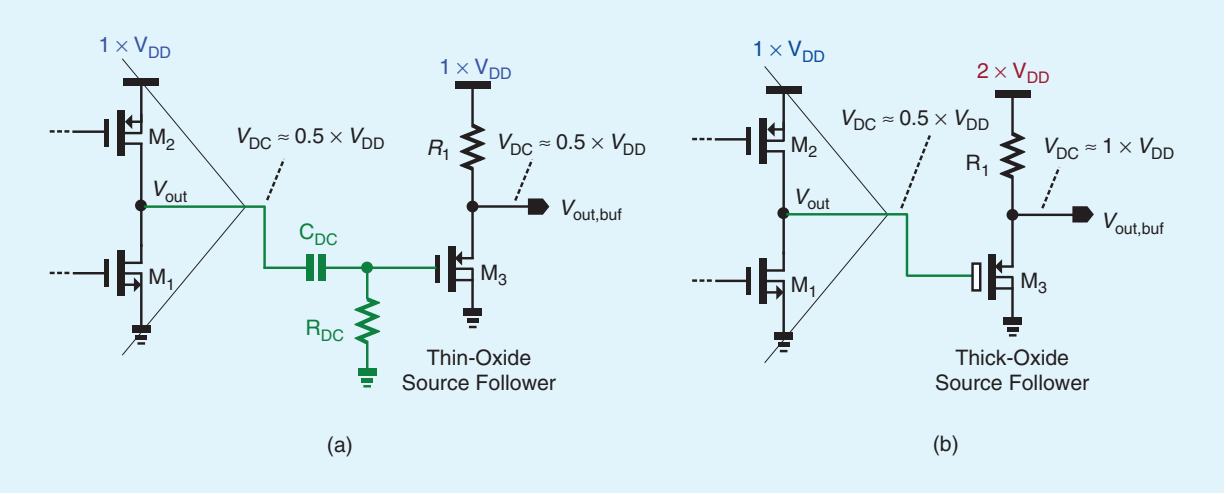


Figure 10. *Source follower as buffer: (a) $1xV_{DD}$ design with thin-oxide MOS needs ac-coupling RC circuit for correct biasing. (b) $2xV_{DD}$ design with thick-oxide MOS avoids the RC circuit while enlarging the output swing.*

features better stability and PSRR. The key appeal is that $V_G > V_{DD12}$ occurs, which was not possible in a single-V_{DD} design. In a mixed-V_{DD} design with 1.2 V (V_{DD12}) and 2.5 V (V_{DD25}), $V_G > V_{DD12}$ becomes possible [Figure 11(c)]. The benefits of NMOS-based LDO are retained, while an added benefit is that the maximum $V_{out,max}$ can now be V_{DD12} (i.e., no dropout voltage). The key drawback is that every 1-mA current to the core circuit induces a 1.3-mW power loss in the pass transistor, as the core just uses its internal 1.2 V, while the total current is drawn from the global 2.5 V. Thus, the technique is more appropriate for low-power, high-sensitivity circuits.

In addition to V_{DD}-LDO, ground-LDO is becoming more important to desensitize low-noise circuits such as voltage-controlled oscillators (VCOs) from substrate noise coupling. Due to the presence of V_{DD25}, V_{DD}- and ground-LDOs can be used jointly, as shown in Figure 12, featuring the same advantages as the one shown in Figure 11(c). The VCO may employ a thick-oxide varactor or MOSFET capacitor as the frequency tuning element, potentially covering a wider tuning range. Proper biases can ensure that the internal rail is sufficiently large for the core circuit, offsetting the voltage headroom consumed by the LDO. Again, the drawback is that every 1-mA current to core circuit yields 1.3-mW power loss in the pass transistors. This is the price for avoiding external components.

Proper biases can ensure that the internal rail is sufficiently large for the core circuit, offsetting the voltage headroom consumed by the LDO.

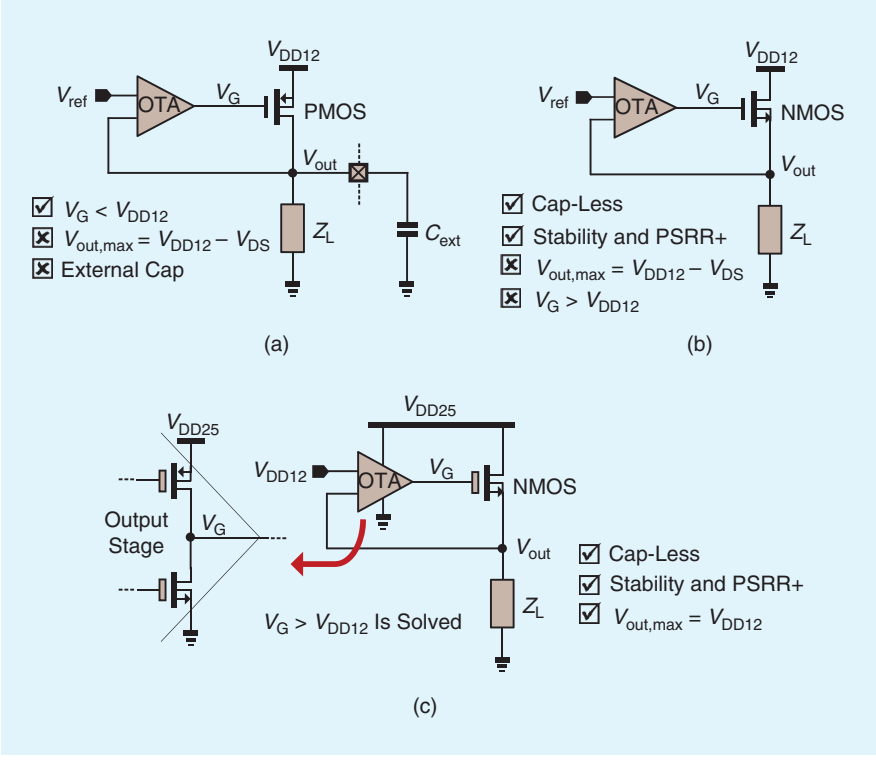


Figure 11. *LDO using an operational transconductance amplifier (OTA) with (a) a PMOS pass transistor, (b) an NMOS pass transistor, and (c) a mixed-voltage design on a NMOS pass transistor. (PSRR+: positive-rail power supply rejection ratio).*

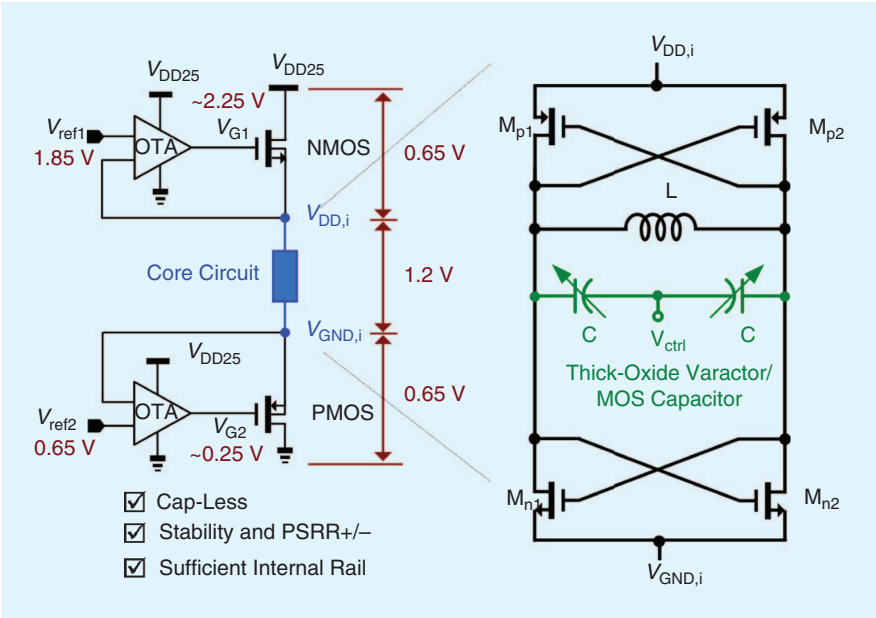


Figure 12. *Mixed-V_{DD} mixed-device LDO pair for both V_{DD} and ground regulation. Triple well can be used for $M_{n1\text{-}2}$ and $M_{p1\text{-}2}$.*

A Mixed-V_{DD} Mixed-Device Transceiver

There is no unique solution on how to select the optimum V_{DD}s and devices in a system plan, but the design considerations can be generalized to delineate a mixed-$V_{DD,}$ mixed-device wideband

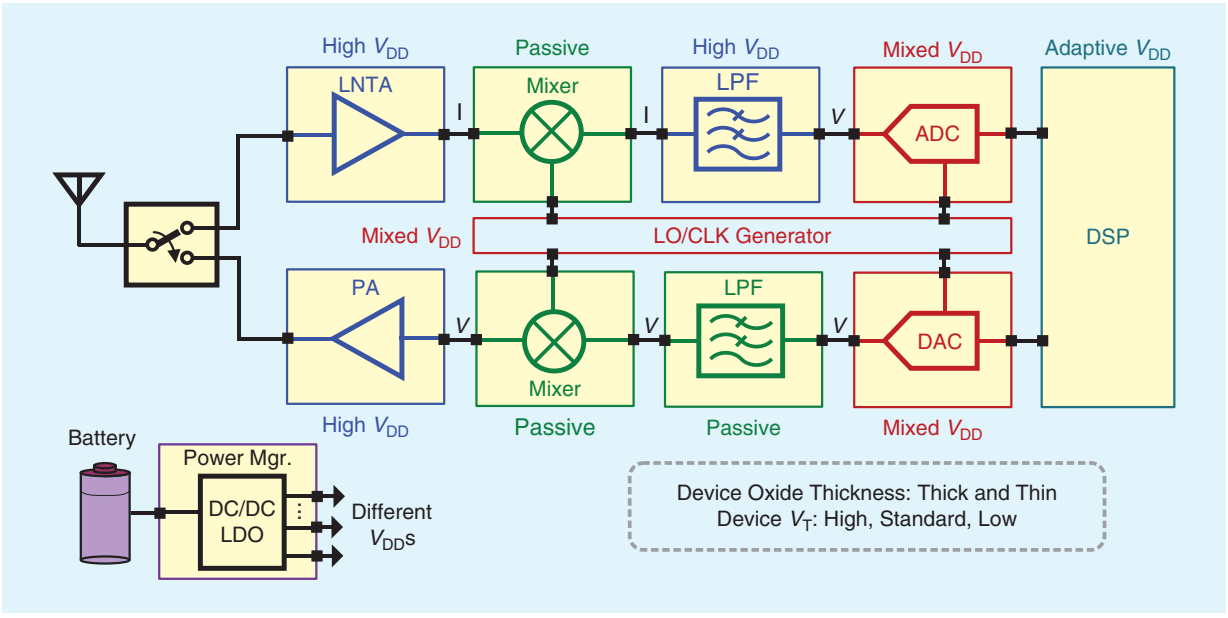


Figure 13. *A prospective mixed-V_{DD} mixed-device wideband transceiver for multistandard applications.*

transceiver architecture potentially suitable for multistandard applications (Figure 13). The features of such a transceiver architecture can be highlighted as follows: Inductorless design is already an obvious approach for area savings in RF receivers. When a high-V_{DD} is employed, a wideband LNTA can deliver the desired gain with high DR when driving a current-mode passive mixer. The first BB LPF using an OpAmp with *RC* feedback and working as a current-to-voltage converter can directly benefit from the gain and DR offered by a high-V_{DD}. With the advance in ADCs, $V_{DD,c}$ can already lead to excellent power efficiency for the requirements of most wireless applications (speed of 20–60 MS/s and resolution of –11 b). A mixed-$V_{DD,}$ however, will be more relevant when more resolution is designed to relax the required order of its preceding LPF, which is area inefficient. For instance, the nonlinearity of a sample-and-hold circuit of an ADC can be significantly reduced by using a thick-oxide MOS as the sampling switch driven by a high-V_{DD} clock [22]. Moreover, the OpAmps involved in the data converters can also benefit from a high-V_{DD} to achieve a higher dc gain and a wider signal swing (Table 3).

The use of a high-V_{DD} PA is a common system block in wireless transmitters to boost the output power while enhancing efficiency, especially for multiband communications where *LC* resonators should be avoided. For the mixers and BB lowpass filters, passive implementation is becoming more relevant to avoid distortion and minimize the output noise floor; both are critical parameters for wideband transceivers where external SAW filters are no longer cost efficient.

A fully on-chip power-management unit with multiple V_{DD} outputs, based on single-inductor dc-dc converters and/or LDOs, are necessary for the benefits of the mixed-V_{DD} design to become more obvious at the system level. In particular, inductorless and cap-less solutions

TABLE 3. Performance comparison of OpAmps: 1-V folded-cascode (FC), 1-V recycling folded-cascode (RFC) and 2-V RFC.

Parameters	1-V FC	1-V RFC	2-V RFC
Power (Bias current) [μA]	600	600	300
DC gain [dB]	45.3	54.0	**72.8**
Gain-bandwidth (GBW) [MHz]	68.2	157.8	97.5
Open loop phase margin (PM) [°]	86.6	60.9	70.7
Capacitive load [pF]	5.0	5.0	5.0
Slew rate (average) [V/μs]	53.3	96.6	65.4
1% Settling time [ns]	24.8	9.8	18.0
Gain precision (closed loop, ideal case is 1)	98.6%	99.4%	**99.8%**
IM3, 0.5 Vpp at 0.5 MHz [dB]	–49.7	–57.2	**–76.5**
Input referred noise (1 Hz–100 MHz) [μVrms]	74.4	64.3	**83.2**
Input offset Voltage [mV] (closed loop, gain = 1)	2.37	1.99	2.64

will be highly beneficial in silicon area savings, which is becoming increasingly expensive in ultrascale process nodes. A high PSRR over a wide bandwidth remains a challenging task for LDOs.

With a high-V_{DD}, the LOG can be based on an *LC* voltage-control oscillator with dual LDOs to enhance PSRR and reduce V_{DD} pulling (Figure 10). The frequency tuning can be increased through the use of thick-oxide varactors or MOS capacitors; both can withstand a wider tuning voltage. For the involved frequency dividers that operate as digital circuits, thin-oxide MOS and $V_{DD,c}$ are adequate.

A time-adaptive V_{DD} for the different digital blocks [23] should be an important aspect for global power reduction (e.g., a very low-V_{DD} in standby mode to minimize leakage power).

Concluding Remarks

Differing from digital design, analog and RF circuits will benefit more from technology scaling if the V_{DD} (high, low or adaptive) can be wisely chosen for certain critical blocks in a wireless SoC. Table 2 reviews the general ways to address performance metrics based on area, current, and supply. The transistor plan for each block can be further customized among the available types, such as thin- or thick-oxide devices, with high-, standard- or low-V_T options. Mixed-V_{DD} mixed-device combined solutions are becoming a new design art of wireless circuits and systems in nanoscale CMOS and will be reusable long-term when the technology continues to advance. This article serves only as a highlight of those prospective techniques, reminding the readers that there are broader resources of advanced CMOS that have not been fully explored. One critical aspect would be to guarantee the circuit reliability compliance with the foundry guidelines when considering the device size and bias schemes in both transient and steady states. It is believed this research direction will gain more momentum in the years to come.

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