Ultra-area-efficient three-stage amplifier using current buffer Miller compensation and parallel compensation

Z. Yan, P.-I. Mak, M.-K. Law and R.P. Martins

An ultra-compact three-stage amplifier is proposed by merging current buffer Miller compensation with parallel compensation, which achieves significant improvement in area efficiency without sacrificing the gain-bandwidth product (GBW) and power. Fabricated in 0.35 μm CMOS the amplifier measures 4.98 MHz GBW at 150 pF load while drawing 20 μA at 2 V. The entailed compensation capacitance is minimised to 1.5 pF and the chip size is merely 0.012 mm^2.

Introduction: Multi-stage amplifiers capable of driving over 100 pF capacitive load (C_L) have found productive applications in capacitorless low-dropout regulators [1], and more recently in audio power amplifiers and headphone drivers. All these impetuses continuously motivate research efforts on multi-stage amplifiers for better C_L drivability, gain-bandwidth product (GBW), and power and area efficiencies. In this Letter, a power- and area-efficient three-stage amplifier topology is proposed. The combination of current buffer Miller compensation and parallel compensation enables high-frequency pole-zero cancellation, allowing the use of ultra-small compensation capacitance and resistance without penalising the amplifier's GBW and power. Experimental verification in 0.35 μm CMOS shows that the measured performance is highly competitive with the state-of-the-art.

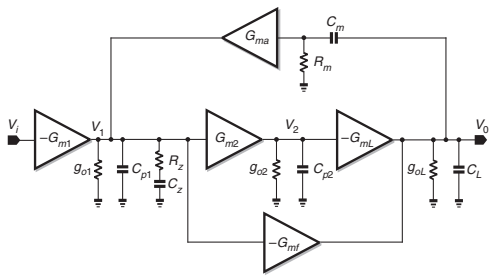

Fig. 1 *Block diagram of proposed three-stage amplifier*

Block-level design: The block diagram is depicted in Fig. 1. The three gain stages are labelled as G_{m1}, G_{m2}, and G_{mL}. The output conductance and lumped parasitic node capacitance of each stage are denoted by $g_{o1\text{-}2,\,L}$ and $C_{p1\text{-}3}$, respectively. C_{p3} is grouped into $C_L{\cdot}C_m$ and G_{ma} form the current buffer Miller compensation while R_m models the input resistance of G_{ma}. Current buffer Miller compensation is selected because it has vital advantages over the simple Miller compensation such as smaller compensation capacitance, higher C_L drivability, larger GBW and better PSRR [2]. The parallel compensation R_zC_z network is to realise local pole splitting and a useful left-half-plane (LHP) zero for pole-zero cancellation [3]. It is well-positioned at the output of the first gain stage, rather than the second one, because the pole $\omega_{p1} = g_{o1}/C_{p1}$ should be typically lower than $\omega_{p2} = g_{o2}/C_{p2}$. The feedforward stage G_{mf} is to boost the large-signal performance. Following the assumptions below:

$$\frac{G_{m1}}{g_{o1}}, \frac{G_{m2}}{g_{o2}}, \frac{G_{mL}}{g_{oL}}, \frac{G_{ma}}{g_{o1}} >> 1 \qquad g_{o1}R_{o1} << 1, R_m = \frac{1}{G_{ma}}$$
$$C_m >> C_{p1}, C_Z >> C_{p1}; C_m, C_Z << C_L \tag{1}$$

the transfer function of the proposed three-stage amplifier can be given by,

$$A_V(s) \simeq \frac{A_0(1+sR_ZC_Z)\left(1+s\frac{C_m}{G_{ma}}\right)\left(1+s\frac{G_{mf}C_{p2}}{G_{m2}G_{mL}}\right)}{\left(1+\frac{s}{\omega_{-3dB}}\right)\left(1+s\frac{g_{o2}}{C_{p2}}\right)\left(1+s\frac{g_{o2}C_ZC_L}{G_{m2}G_{mL}C_m}+s^2\frac{g_{o2}C_ZC_L}{G_{m2}G_{mL}G_{ma}}\right)}(1+sR_ZC_{p2}) \tag{2}$$

where $A_0 = (G_{m1}G_{m2}G_{mL})/(g_{o1}g_{o2}g_{oL})$ is the DC voltage gain, $\omega_{-3dB} = (g_{o1}g_{o2}g_{oL})/(G_{m2}G_{mL}C_m)$ is the dominant pole. The zero $\omega_{z1} = 1/R_zC_z$ generated by the parallel compensation network can be utilised to cancel the pole $\omega_{p2} = g_{o2}/C_{p2}$ associated with the second stage. Since another LHP zero $\omega_{z2} = G_{mf}C_{p2}/G_{m2}G_{mL}$ and pole $\omega_{p3} = 1/R_zC_{p1}$ lie at very high frequencies, their impact on the amplifier's frequency response can be safely ignored. Therefore, (2) can be simplified as

$$A_V(s) \simeq A_0 \frac{\left(1+s\frac{C_m}{G_{ma}}\right)}{\left(1+\frac{s}{\omega_{-3dB}}\right)\left(1+s\frac{C_{p2}C_L}{C_mG_{m2}R_ZG_{mL}}+s^2\frac{C_{p2}C_L}{G_{m2}R_ZG_{mL}G_{ma}}\right)} \tag{3}$$

From (3), GBW is calculated as $A_0 \cdot \omega_{-3dB} = G_{m1}/C_m$, and the LHP zero associated with the current buffer stage G_{ma} is $\omega_{z3} = G_{ma}/C_m$. Consider the second-order polynomial in the denominator of $A_v(s)$. If the two poles are widely separated, which means G_{ma}/C_m is pushed to much higher frequencies, the amplifier's GBW is only limited by the non-dominant pole $C_mG_{m2}R_zG_{mL}/(C_{p2}C_L)$, which is C_m/C_{p2} times larger than that of the structure proposed in [4]. This factor can be beneficially exchanged for a smaller value of R_z, simultaneously maintaining the given GBW and phase margin (PM). Furthermore, instead of stabilising the amplifier by under the Butterworth response, the low-power stability strategy in [5] is employed to achieve 60° PM while using a smaller G_{ma} (i.e. smaller power) and C_m (i.e. smaller area). The key dimension conditions are

$$G_{ma} = 2G_{m1} \quad \text{and} \quad C_m = \sqrt{\frac{1.16G_{m1}C_{p2}C_L}{G_{m2}R_ZG_{mL}}} \tag{4}$$

Circuit implementation: The transistor implementation is depicted in Fig. 2. The input stage G_{m1} is realised with a folded cascode transconductor formed by M_1-M_{10}, $M_{b1\text{-}b2}$, and $R_{1\text{-}2}$. Transistors M_{11} and M_{13}-M_{21} contribute to the amplifier's second stage G_{m2}. The output stage G_{mL} is provided by M_{25}, while M_{24} acts as the forward stage G_{mf}. The gate of M_{23} connected to the gates of M_9 and M_{10} not only produces another feedforward stage to boost the slewing performance of the second stage, but also avoids extra biasing branches and systematic offset of the amplifier [5]. G_{ma} is realised by M_3-M_8 and $R_{1\text{-}2}$, the transconductance of which can be efficiently boosted by its local feedback loop with small power budget [6]. The parallel compensation R_zC_z network is terminated to the power supply, rather than the ground, to improve the positive PSRR (i.e. from simulations, >30 dB improvement in the range 10 kHz to 10 MHz). The bias current in M_{17} is reused by cascading two current mirrors with amplification factors (M_{13}-M_{14} and M_{16}-M_{17}) in the signal path to increase G_{m2} and the factor $G_{m2}R_z$ so that a small G_{mL} is feasible.

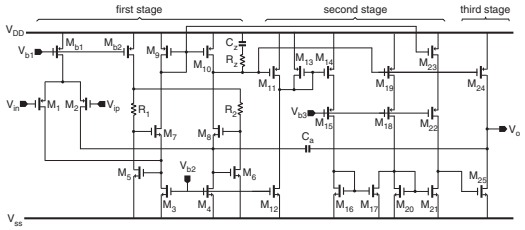

Fig. 2 *Circuit implementation of three-stage amplifier*

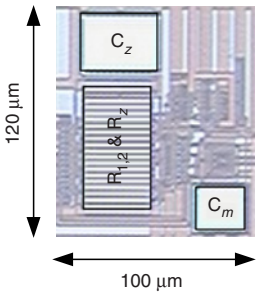

Fig. 3 *Chip photo*

Experimental results: The amplifier was fabricated in 0.35 μm CMOS. The die area is just 0.012 mm^2 (Fig. 3), which is 40% of that of the amplifier from [4] using the same technology node, mainly because the entailed resistance (including R_1 and R_2) is reduced to 389 kΩ while the resistance for parallel compensation in [4] is 750 kΩ. The AC responses are shown in Fig. 4*a*. At 150 pF C_L the amplifier shows a GBW of 4.98 MHz with 50° PM and 11.3 dB gain margin (GM). The step response is shown in Fig. 4*b*. The average slew rate and 1% settling time are 1.64V/μs and 1.97 μs, respectively.

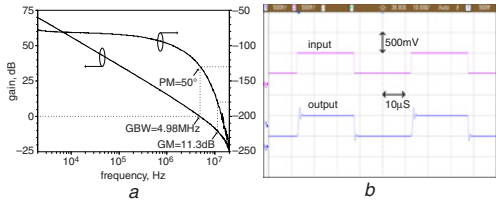

Fig. 4 *Measured performance at 150pF C_L*
a AC responses
b Transient response

A summary of the performance metrics and comparison with two recent works are given in Table 1. This work is advantageous for its smaller area, higher GBW at low power, and overall competitive figures-of-merit (FOMs) compared with [4] and [6].

Table 1: Performance summary and comparison

	This work	ISSCC'12 [6]	JSSC'11 [4]
Load C_L (pF)	150	1000	150
GBW (MHz)	**4.98**	1.37	4.4
Phase margin (°)	50	83.2	57
Gain margin (dB)	**11.3**	9.8	5*
Average SR (V/μS)	1.64	0.59	1.8
Average 1% TS (μS)	1.97	1.28	1.9
DC gain (dB)	>110	>100	110
Power (μW) at VDD (V)	40 at 2	144 at 2	30 at 1.5
Total C_t (pF)	**1.5**	2.6	1.6
Chip area (mm^2)	**0.012**	0.016	0.02
CMOS technology	0.35 μm	0.35 μm	0.35 μm
FOMS [(MHz · pF)/mW]	18675	9514	22000
FOML [(V/μS · pF)/mW]	6150	4097	9000
IFOMS [(MHz · pF)/mA]	**37350**	19028	33000
IFOML [(V/μS · pF)/mA]	12300	8194	13500

* Denotes extracted value from plot

Conclusion: A novel three-stage amplifier topology has been proposed. Current buffer Miller compensation and a well-positioned *RC* network for parallel compensation effectively shift up the pole-zero cancellation to a high frequency, resulting in very low power (40 μW) and small area (0.012 mm^2) in silicon realisation. The measured GBW at 150 pF load is 4.98 MHz.

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One or more of the Figures in this Letter are available in colour online.

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