An Optimum CMOS Switched-Capacitor Antialiasing Decimating Filter

R. P. Martins, *Member, IEEE*, José E. Franca, *Senior Member, IEEE*, and Franco Maloberti, *Senior Member, IEEE*

***Abstract*— An optimum switched-capacitor (SC) decimating filter is capable of achieving a high input sampling frequency while the time period for the settling of the operational amplifiers can be maximized with respect to the lower output sampling frequency. Thus, for the same speed of the operational amplifiers, the oversampling ratio of the input signal in optimum SC decimating filters is much larger than in conventional SC filtering circuits yielding a significant relaxation of the continuous-time prefiltering requirements. This is demonstrated considering the design of a second-order SC antialiasing decimating filter, with a threefold sampling rate reduction, which has been realized in a 1.8-μm CMOS double-poly technology. The experimental evaluation of prototype samples confirms the expected operation of the circuit.**

I. Introduction

ANALOG signal processing circuits for high-frequency and very-high-frequency operation represent an important research area due to the rapid technology developments of video signal processing, mobile communications, and high-speed data transmission [1], [2]. In such application areas, there have been significant efforts devoted to extend the operating frequency of CMOS switched-capacitor (SC) filters towards increasingly higher frequencies [3]–[7] and it has also been suggested that the development of optimum multirate SC decimating and interpolating techniques could push even further the limits of operation of such circuits [8]–[11]. In fact, such techniques make it possible to obtain SC circuits with a sufficiently high ratio between the sampling frequency and the maximum signal frequency of interest without increasing unnecessarily the speed requirements of the amplifiers. They are, therefore, particularly attractive for high-speed interfacing applications requiring a filtering function together with a sampling rate alteration. The purpose of this paper is to experimentally characterize and demonstrate the practical feasibility of one such SC antialiasing decimating filter, and discuss the practical advantages that can be gained with respect to more conventional SC filtering techniques.

Section II describes the architecture and practical design aspects of an SC decimator, with optimum implementation, that realizes a bilinear low-pass second-order z-transfer function and provides a reduction from an input sampling frequency of $3F_s$ to a lower sampling frequency of F_s, together with the appropriate rejection of the unwanted alias frequency components around F_s and $2F_s$. In this work we have chosen a low value ($M = 3$) of the decimating factor in order to simplify the corresponding IC realization described in Section III, particularly bearing in mind that we employed externally driven multiple switching waveforms to control the operation of the circuit in a flexible way for evaluation purposes. The results of such evaluation carried out on prototype samples manufactured using a 1.8-μm CMOS double-poly technology are presented in Section IV, demonstrating the overall good performance of the circuit. Experimental results are also shown with respect to the performance behavior of the SC decimator building block when timing errors are deliberately associated with the switching waveforms. The conclusions of this work are drawn in Section V.

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II. Circuit Architecture and Design

A. Architecture

For simplicity of explanation, we consider the architecture of the SC decimator circuit presented in this paper subdivided into a nonrecursive polyphase network and a two-integrator loop network, as indicated in Fig. 1(a). The two-integrator loop network alone is responsible for the realization of the poles of the filtering function, and in order to maximize the time period for the settling of the amplifiers its switching operation is controlled by the nonoverlapping waveforms corresponding to time slots 1 and 2 in time frame B, as shown in Fig. 1(b).[1] The zeros of the filtering function, on the other hand, are realized by the feedforward paths from the circuit input to the circuit output and therefore are jointly defined by the nonrecursive polyphase network together with the portions of the two-integrator loop network that convey the signal to the circuit output. The switching operation of the polyphase network is controlled by all waveforms in both time frames A and B. The waveforms corresponding to time slots 3, 4, and 5, in time frame A, control the switching operation of the switches which are responsible for the sampling of the input signal, whereas the waveforms corresponding to time slots 1 and 2, in time frame B, control the switching operation of the switches which allow charge transfer from the input capacitors to the feedback capacitors of the amplifiers. Here,

[1] The time slots of the switching waveforms correspond to the intervals when the signal is high.

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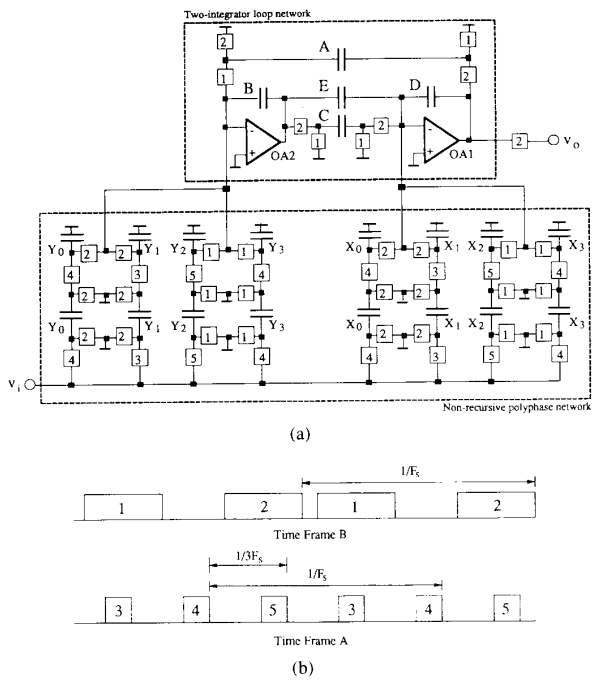


Fig. 1. Second-order SC low-pass decimator with $M = 3$. (a) Circuit. (b) Switching waveforms.

it is required that the width of the time slots 3, 4, and 5 can accommodate the charge settling of the input capacitors to within an error compatible with the required circuit accuracy. This can be achieved without too much difficulty by designing the input SC branches with very low time constants RC, where C is the value of the branch capacitance and R is the value of the ON resistance of the associated switches. Unlike in the previous situation, the speed of the charge transfer from the input capacitors to the feedback capacitors is determined primarily by the settling of the amplifiers. Hence, for a given switching frequency F_s, the wider we can make the width of time slots 1 and 2 the slower we can render the amplifiers in order to save power and even occupy a smaller die area.

From the previous circuit description we can easily see that in every period of the output signal sampled in time slot 2, the input signal is sampled in time slots 3, 4, and 5, i.e., at an effective rate of $3F_s$. Hence, for a maximum signal frequency of $f_{\max}$ and the same speed of the amplifiers, the above optimum SC decimator achieves an input oversampling ratio of $(3F_s/f_{\max})$ compared to only $(F_s/f_{\max})$ that would have been achieved with traditional SC filters, and therefore significantly relaxes the selectivity requirements of the continuous-time prefilters. Further increase of the oversampling ratio and consequent relaxation of the continuous-time prefiltering requirements can be achieved by designing optimum SC decimator building blocks with even higher decimating factors [9].

B. Design

According to the work reported in [9], the z-transfer function of the SC decimator circuit of Fig. 1, with $M = 3$, can be written as

$$T(z) = \frac{\sum_{m=0}^{6} a_m z^{-m}}{1 - b_1 z^{-3} + b_2 z^{-6}} \tag{1a}$$

where

$$\begin{aligned} a_0 &= \overline{X}_0 - (\overline{C} + \overline{E})\overline{Y}_0 & a_4 &= -\overline{X}_1 + \overline{E}\,\overline{Y}_1 \\ a_1 &= \overline{X}_1 - (\overline{C} + \overline{E})\overline{Y}_1 & a_5 &= -\overline{X}_2 + \overline{E}\,\overline{Y}_2 \\ a_2 &= \overline{X}_2 - (\overline{C} + \overline{E})\overline{Y}_2 & a_6 &= -\overline{X}_3 + \overline{E}\,\overline{Y}_3 \\ a_3 &= \overline{X}_3 - (\overline{C} + \overline{E})\overline{Y}_3 - \overline{X}_0 + \overline{E}\,\overline{Y}_0 \end{aligned} \tag{1b}$$

and

$$\begin{aligned} b_1 &= 2 - \overline{A}(\overline{C} + \overline{E}) \\ b_2 &= 1 - \overline{A}\,\overline{E} \end{aligned} \tag{1c}$$

represent, respectively, the numerator and denominator coefficients. In the above expressions the capacitance ratios are written as

$$\overline{Y}_i = \frac{Y_i}{B}, \quad \overline{A} = \frac{A}{B}, \quad \overline{X}_i = \frac{X_i}{D}, \quad \overline{C} = \frac{C}{D}, \quad \overline{E} = \frac{E}{D} \tag{1d}$$

and the unit delay period refers to the high input sampling frequency $(3F_s)$. This was designed to produce a bilinear second-order low-pass Tchebyshev amplitude response, with passband ripple of 0.01 dB and normalized cutoff frequency of $f_c/F_s = 0.013$. The corresponding z-transfer function is

$$H(z) = k\,\frac{1 - 2r_z \cos(\theta_z) z^{-1} + r_z^2 z^{-2}}{1 - 2r_p \cos(\theta_p) z^{-1} + r_p^2 z^{-2}} \tag{2}$$

whose coefficients are given in Table I. For optimum implementation, the above z-transfer function must be modified such that its denominator contains only the powers of z^{-M} and z^{-2M}, i.e., the samples at the output of the amplifiers are produced at the lower sampling frequency F_s [8]. This leads to

$$H'(z) = \frac{\sum_{m=0}^{6} a'_m z^{-m}}{1 - 2r_p^3 \cos(3\theta_p) z^{-3} + r_p^6 z^{-6}} \tag{3}$$

where the modified coefficients are indicated in Table II. Then, by equating (3) and (1), we arrive at the following design equations:

$$\begin{aligned} &A = C = [1 - 2r_p^3 \cos(3\theta_p) + r_p^6]^{1/2}, \quad E = \frac{1 - r_p^6}{A}, \\ &B = D = 1, \quad X_0 = EY_0 - a'_{32}, \quad X_1 = EY_1 - a'_4, \\ &X_2 = EY_2 - a'_5, \quad X_3 = EY_3 - a'_6, \quad Y_0 = -\frac{a'_0 + a'_{32}}{A}, \\ &Y_1 = -\frac{a'_1 + a'_4}{A}, \quad Y_2 = -\frac{a'_2 + a'_5}{A}, \quad Y_3 = -\frac{a'_{31} + a'_6}{A}. \end{aligned} \tag{4}$$

Reduced capacitance spread is achieved by making $a'_3 = a'_{31} + a'_{32}$ and $a'_{31} = a'_{32}$. After scaling for maximum signal handling capability we obtain the normalized capacitance values indicated in Table III yielding a total capacitor area of only 78.87 capacitance units.

TABLE I
COEFFICIENTS OF THE ORIGINAL DISCRETE-TIME EQUATION (2)

k	1.68340 e-3
$2 r_z \cos(\theta_z)$	-2
r_z^2	1
$2 r_p \cos(\theta_p)$	1.883221
r_p^2	0.889963

TABLE II
COEFFICIENTS OF THE MODIFIED DISCRETE-TIME EQUATION (3)

a'_0	1
a'_1	3.88322
a'_2	5.75970
a'_3	8.87234
a'_4	6.80059
a'_5	3.26006
a'_6	0.79203
$2 r_p^3 \cos(3\theta_p)$	1.65090
r_p^6	0.70488

TABLE III
NORMALIZED CAPACITANCE VALUES FOR THE SC DECIMATOR OF FIG. 1

A = 3.067	C = 3.349
B = 18.82	D = 10.11
———	E = 18.31
Y_0 = 1.040	X_0 = 1.163
Y_1 = 2.044	X_1 = 2.220
Y_2 = 2.043	X_2 = 2.099
Y_3 = 1	X_3 = 1
Capacitance Spread = 18.82	
Total Capacitor Area = 78.87 units	

C. Speed Requirements of the Amplifiers

One of the most important aspects affecting the high-frequency performance of SC circuits concerns the finite dc gain and bandwidth of the amplifiers [3], [7], [12]. For the envisaged 1.8-μm CMOS technology [13] and considering a maximum output sampling frequency close to $F_{s_{\max}} = 5$ MHz, we carried out a computer-based evaluation which led us to optimally tailor the design of the amplifiers such that the minimum dc gain (A_o) and gain–bandwidth product (GB) are $A_{o1} = 40$ dB and $GB_1 = 2.5F_s$ for amplifier OA1, and $A_{o2} = 80$ dB and $GB_2 = 3.5F_s$ for amplifier OA2. The computer-simulated amplitude response of the SC decimator circuit under such nonideal characteristics of the amplifiers is close to the specified nominal response, as shown in Fig. 2(a) and (b), respectively, for the passband and the overall baseband responses.

It is appropriate to recall here that if an input sampling frequency equivalent to the one of the decimating circuit described above, i.e., $3F_s$, was to be achieved using a conventional SC biquad design, then the required minimum GB values of the amplifiers would have been, respectively, $10.5F_s$ and $7.5F_s$ [12]. Such an advantage of SC decimating building blocks becomes even more significant as the decimating factor increases.

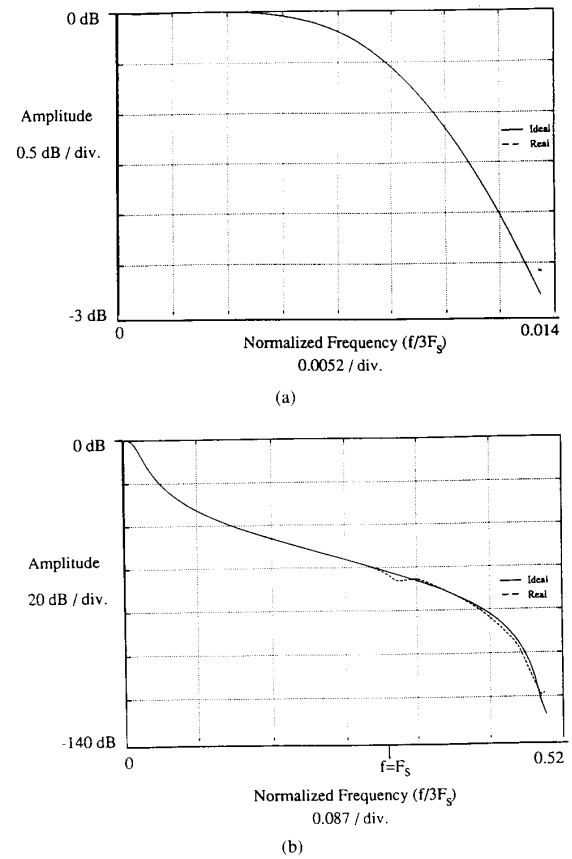


Fig. 2. Computer-simulated baseband amplitude responses of the SC decimator considering ideal and real characteristics of the amplifiers. (a) Passband. (b) Baseband from dc to $3F_s/2$.

D. Other Nonideal Aspects

Other aspects affecting the operation of SC decimating circuits at high frequency concern the timing errors associated with the switching waveforms. In order to explain the effects produced by such errors we have to recall [9], [14] that although the modified z-transfer function $H'(z)$ is equivalent to $H(z)$, this is achieved by means of an ideal pole–zero cancellation at frequencies around F_s and $2F_s$, as schematically illustrated in Fig. 3. Such pole–zero cancellation is particularly dependent on the accuracy of the input sampling instants determined solely by time slots 3, 4, and 5. This is illustrated by the computer-simulated results presented in Fig. 4 corresponding to a timing error of $\pm 0.05T_s$ deliberately introduced in time slot 4. Similar results are observed for time slots 3 and 5. On the contrary, as expected, no variations are observed when a similar timing error is introduced in both time slots 1 and 2 [14]. It will be shown later, in Section IV,

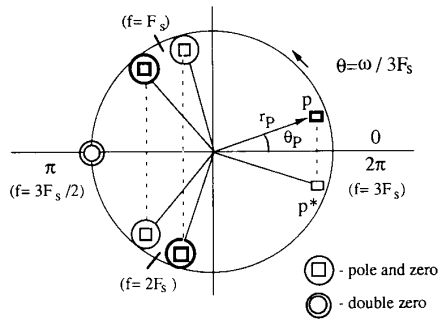


Fig. 3. Pole–zero pattern representation of the modified z-transfer function $H'(z)$.

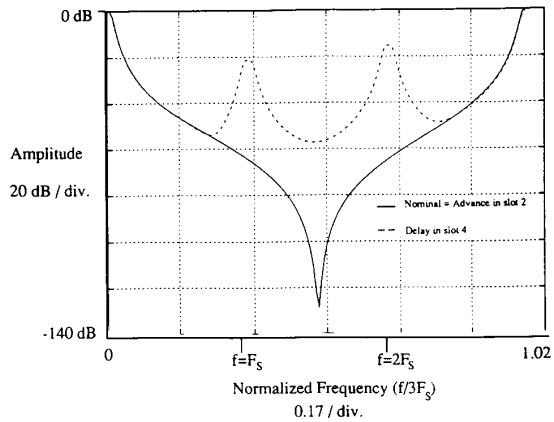


Fig. 4. Computer-simulated amplitude response of the SC decimator of Fig. 1 considering timing errors of $\pm 0.05T_s$ introduced in time slots 2 and 4.

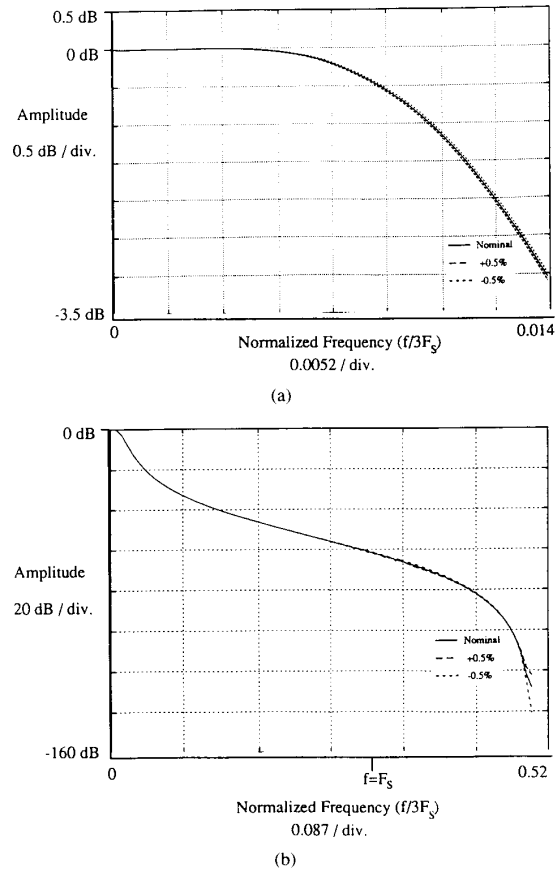


Fig. 5. Computer-simulated amplitude response of the SC decimator of Fig. 1 considering nominal values and $\pm 0.5\%$ variation in capacitors B and E. (a) Passband. (b) Baseband.

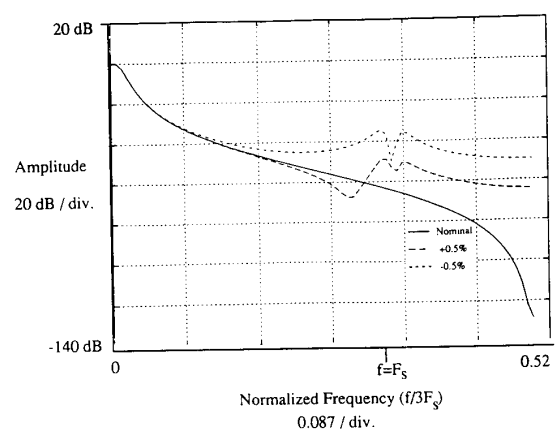


Fig. 6. Computer-simulated baseband amplitude response of the SC decimator of Fig. 1 considering nominal values and $\pm 0.5\%$ variation in capacitors X_1 and Y_2.

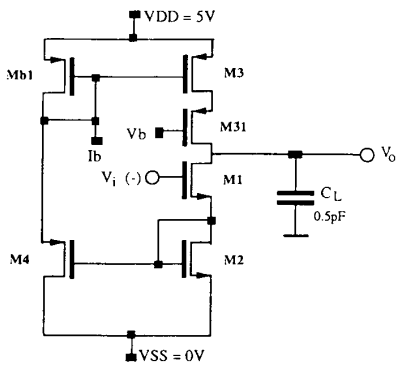
that these results are also corroborated by the experimental evaluation of a number of prototype IC's manufactured for demonstration purposes.

The nominal frequency response of the SC decimator building block can also be affected by capacitance mismatch errors in the circuit, as illustrated by the computer-simulated results presented in Figs. 5 and 6. In Fig. 5, we can observe that $\pm 0.5\%$ variation of the nominal capacitance values of capacitors B and E essentially produce passband errors related to variations of the pole frequency and pole Q factor. Such conclusions apply to capacitance mismatch errors associated with the remaining capacitors A, D, and C that form the two-integrator loop. On the other hand, Fig. 6 shows that $\pm 0.5\%$ variation of the nominal capacitance values of capacitors X_1 and Y_2 produce frequency response errors in the bands around F_s and $2F_s$ which are again related to variations of the pole–zero cancellation. Similar results are obtained for the remaining input capacitors.

III. Integrated Circuit Implementation

A. Operational Amplifiers

Based on the previous discussion on the speed requirements of the amplifiers, we adopted two different architectures for designing OA1 and OA2. For OA1 we adopted the architecture shown in Fig. 7, consisting of a simple inverter stage that can achieve very high operating speeds although with relatively modest values of the dc gain [15]. For OA2 we adopted instead the single-stage folded-cascode architecture shown in



Transistor	(W/L) (μm)
M1	165/2.5
M2	165/2.5
M3	100/4
M31	400/4
M4	200/4
Mb1	100/4

Fig. 7. Single inverter cascode CMOS amplifier.

Fig. 8, which can exhibit a much larger dc gain [15]. Here, we have considered a triple-cascode output stage to increase the amplifier gain even further by means of boosting the effective output resistance at the expense of an acceptable reduction of the output voltage swing [16]. For the 1.8-μm CMOS technology used for IC implementation [13], Table IV indicates the simulated performance characteristics obtained for both amplifiers. In order to reduce amplifier performance degradation related to transistor mismatching as well as to minimize the capacitance values of the drain–bulk and source–bulk capacitors associated with the transistors, which are particularly important at high frequency, both amplifiers are laid out using a stacked format [17]–[19].

B. Capacitors

High-precision capacitors have been designed with guard rings around the top plate in order to minimize etching and fringing effects. In order to maximize the accuracy of larger capacitance ratios, we employ an association of unit capacitors where the unit capacitance is approximately 0.2 pF (18 μm $\times$ 18 μm). According to the normalized capacitance values of Table III for the SC decimator of Fig. 1, such unit capacitance implies a maximum capacitance value of 3.764 pF, for capacitor B, and a minimum capacitance value of 0.2 pF, for capacitors X_3 and Y_3.

C. Analog Switches

The specifications for designing the analog switches are basically determined by the ON resistance needed to achieve the required speed of operation. The transistors for the switches in the loop of the circuit are primarily designed to withstand large charge pulses whereas the input switches are primarily designed for very fast charging of the input capacitors. Considering again the maximum values envisaged for the input and output sampling frequencies, respectively 15 and 5 MHz, we designed the faster switches to be controlled by 10-ns-wide time slots 3, 4, and 5 and the slower switches to be controlled by 95-ns-wide time slots 1 and 2. Considering furthermore that the input sampling and charge transfer operations have to settle within approximately 7 time constants for negligible errors, this leads to maximum time constants of $\tau_f \approx 1.43$ ns and $\tau_s \approx 13.57$ ns, respectively, associated with the faster and slower switches. Then, considering the maximum capacitance values of $X_1 = 0.444$ pF, for the input polyphase network, and $B = 3.76$ pF in the two-integrator loop network, we obtain the maximum values of $R_{ON_f} = 3.25$ kΩ and $R_{ON_s} = 3.61$ kΩ, respectively, for the faster and slower switches. This is achieved by designing the analog switches as indicated in Fig. 9 for nominal operating voltage of 5 V. For improved matching a stacked layout technique has also been adopted for both the parasitic insensitive and parasitic-compensated types of SC branches employed in the SC circuit of Fig. 1.

D. Final Architecture

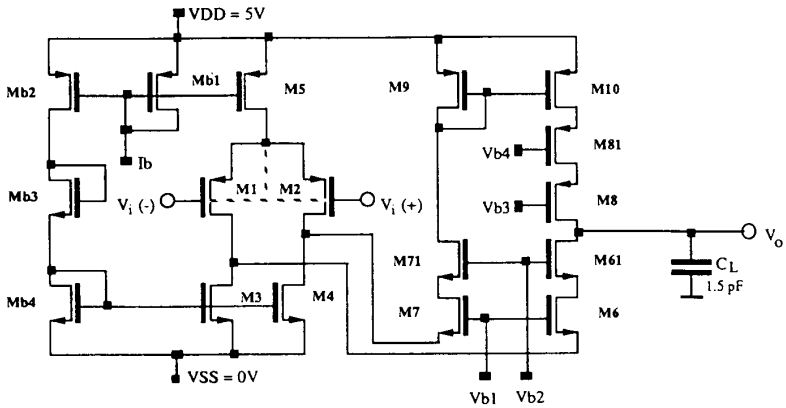
In order to experimentally study the nonideal effects associated with the switch timing, we have planned the prototype IC in such a way that both the switching frequency F_S and the complete switch timing can be externally controlled in order to generate different patterns of the time slots. The photomicrograph of the prototype IC comprising four SC decimator building blocks is shown in Fig. 10. The overall silicon area of each SC decimator building block (considering only the active core, without pads) is $550 \times 460\,\mu\text{m}^2 \approx 0.25\,\text{mm}^2$.

IV. Experimental Results

Testing was carried out using an experimental board containing all the circuitry necessary to generate the bias currents and the biasing voltages for the amplifiers, whereas the appropriate switching waveforms are generated by a digital pattern generator. The output signal of the SC decimator is monitored through an active probe with an input capacitance of 3.5 pF. The total power consumption of one SC decimator building block is approximately 1.25 mW at 5 V.

A. Baseband Measurements

Baseband frequency measurements of multirate circuits are obtained when the input signal generator and output detector are both tuned to the same frequency [20]. For an output sampling frequency of $F_s = 347.22$ kHz the resulting amplitude response of the SC decimator circuit, shown in Fig. 11, agrees closely with the nominal characteristic. Similar results are obtained for output sampling frequencies up to $F_s = 2.78$ MHz, as also illustrated in Fig. 12, when the resulting widths of the time slots are well above the limit for comfortable operation of the amplifiers. For an output sampling frequency of $F_s = 5.56$ MHz, yielding 80-ns-wide time slots 1 and 2 which are already out of the designed limits of operation of the amplifiers, the circuit exhibits some deviations that can be observed also in Fig. 12. The corresponding input sampling frequency is 16.59 MHz. This suggests that by designing even faster operational amplifiers which would be capable of achieving an output sampling frequency of the order of 30 MHz [17], [19], this SC decimator building block could achieve an input sampling frequency close to 100 MHz, which is within the reach of current CMOS technology [21].



Transistor	(W/L) (μm)	Transistor	(W/L) (μm)
M1	100/2	M10	48/1.8
M2	100/2	M61	72/1.8
M3	80/2	M71	72/1.8
M4	80/2	M81	48/1.8
M5	48/1.8	Mb1	48/1.8
M6	72/1.8	Mb2	24/1.8
M7	72/1.8	Mb3	20/2
M8	48/1.8	Mb4	40/2
M9	48/1.8		

Fig. 8. Folded-cascode CMOS amplifier.

TABLE IV
COMPUTER-SIMULATED CHARACTERISTICS OF THE AMPLIFIERS FOR A 1.5-pF CAPACITANCE LOAD

Characteristics	*Amplifier OA1*	*Amplifier OA2*
DC-Gain (dB)	40	89
GB (MHz)	80	18
Phase Margin (o)	> 90	65
Settling Time (ns) (1 V within 0.1%)	50	82
Input Offset (mV)	----	16
Bias Current (μA)	100	150
Area (μm) ^{2}	160 x 140	140 x 180

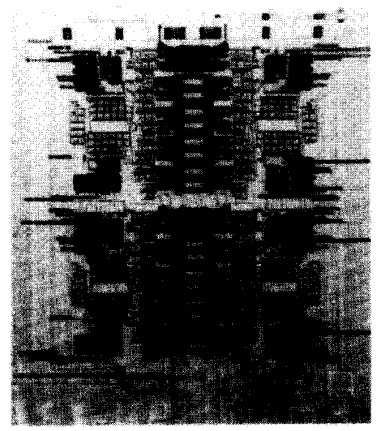


Fig. 10. Microphotograph of the prototype IC.

Switches	(W/L) (μm)	
	M1	M2
Input branches	4.8 / 1.8	5.4 / 1.8
Loop branches	5 / 2	6 / 2

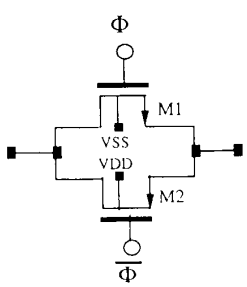
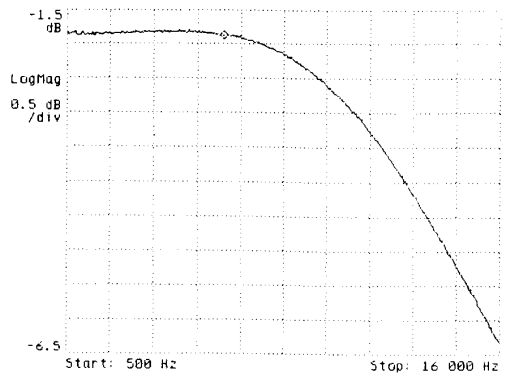


Fig. 9. CMOS analog switches.

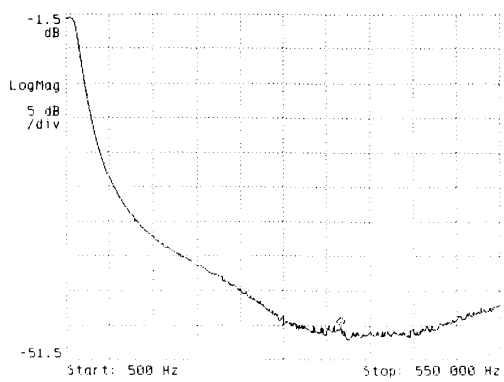
For the input sampling frequency of $3F_s = 4.17$ MHz and output sampling frequency of $F_s = 1.39$ MHz, the measured passband noise floor is -49 dB below an output signal reference level of 0 dBm. Since the maximum output signal level before amplifier clipping is approximately 11 dBm, the resulting output signal-to-noise ratio is 60 dB, which is adequate for many practical high-frequency antialiasing filtering applications [4]–[6].

B. Aliasing Measurements

Aliasing frequency measurements of multirate circuits are obtained when the input signal generator is tuned in one aliasing band, for example, around F_s and $2F_s$, and the output detector is synchronously tuned in the baseband [20]. We have observed before that this SC decimator circuit attenuates alias frequency components around F_s and $2F_s$, which cannot at all be attenuated by conventional SC filters. This situation is illustrated in Fig. 13, again for an output sampling frequency $F_s = 347.22$ kHz, when the source generator produces input signal components from 347.22 to 367.22 kHz corresponding to the first aliasing band and the output signals are synchronously detected in the baseband from dc to 20 kHz. Here, we can observe both the nominal response obtained by computer simulation employing finite GB values for the operational amplifiers and the measured alias response obtained for the nominal switch timing controlling the operation of the circuit. Our investigations led us to attribute this error to frequency-dependent mismatch errors arising in the input polyphase structures which are expected to be eliminated in future implementations. However, in practical applications such error may not be too serious since the alias components around F_s will always suffer a complementary attenuation due to the continuous-time prefilter. The results obtained for the rejection of the alias frequency components in the second alias band around



(a)



(b)

Fig. 11. Measured baseband amplitude responses of the SC decimator of Fig. 1 with an output sampling frequency of $F_s = 347.22$ kHz. (a) Passband. (b) Baseband (dc to $3F_s/2$).

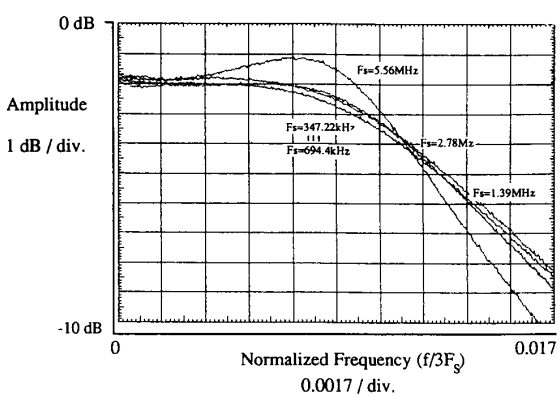


Fig. 12. Measured passband amplitude responses with output sampling frequencies varying from $F_s = 347.22$ kHz up to $F_s = 5.56$ MHz.

$2F_s$ are consistent with the ones shown here for the first alias band and in agreement with our theoretical predictions [14].

C. Imaging Measurements

Complementary to the above aliasing measurements, imaging frequency measurements of multirate circuits are obtained when the input signal generator is tuned in the baseband and the output detector is synchronously tuned in each of the imaging bands. Here, the imaging response is solely shaped by the sample and hold format of the output signal. For the first and second imaging bands we have observed that the signals are attenuated by minimum values of, respectively, 35.6 and 39.3 dB, in close agreement with the theoretical predictions. Further results are presented in Table V.

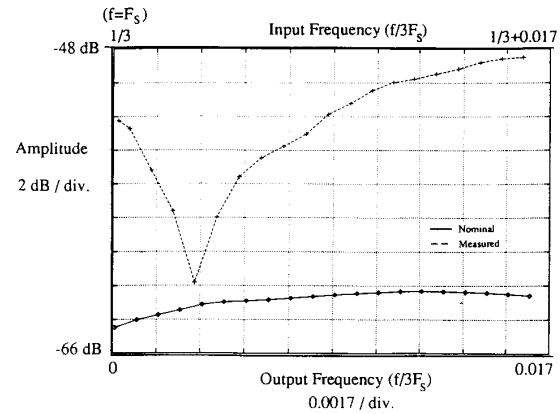


Fig. 13. Aliasing response in the passband corresponding to input frequencies in the first aliasing band around $F_s = 347.22$ kHz.

TABLE V
IMAGING MEASUREMENTS AROUND THE FIRST AND SECOND IMAGING BANDS

Input Frequencies (kHz)	Output Frequencies (kHz)	Attenuation (dB)	Output Frequencies (kHz)	Attenuation (dB)
0.25	347.5	36.05	695.5	39.82
0.75	348	35.63	696	39.33
1.75	349	35.98	697	40
2.75	350	36.12	698	40.11
4.75	352	36.76	700	41.26
8.75	356	37.93	704	41.51
16.75	364	38.14	708	42.13
Passband	1st. Imaging band @ Fs		2nd. Imaging band @ 2Fs	

D. Effects of Switch Timing Errors

Besides the above characterization of the baseband and frequency-translated amplitude responses of the antialiasing SC decimator circuit, we have also investigated in the laboratory the influence of switch timing errors that might arise in association with the multiple switching waveforms controlling the operation of the circuit. For such evaluation we have changed the nominal switching waveform pattern by introducing larger guard intervals between time slots 1, 2, and 4.

The experimental baseband measurements shown in Fig. 14(a) indicate that the influence of switch timing errors associated with time slots 2 and 4 is negligible in the passband, as we would have expected by the results discussed in Fig. 4. However, as also expected from that discussion, the timing error associated with time slot 4 will change the amplitude

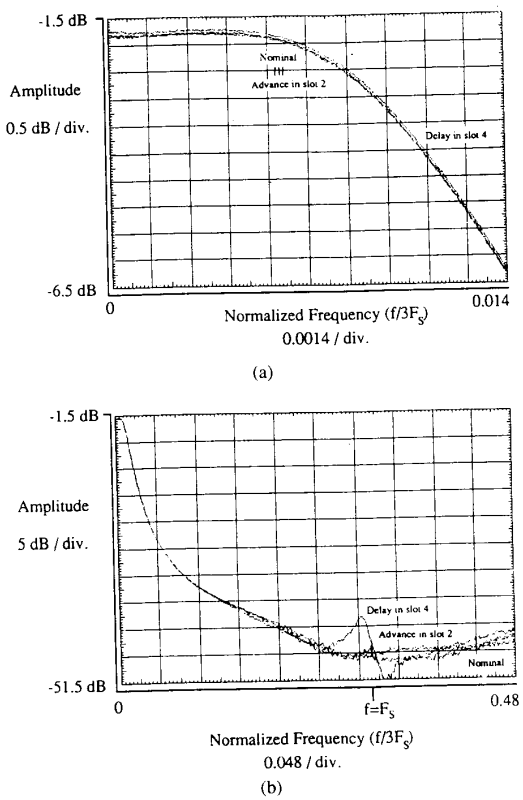


Fig. 14. Measured baseband amplitude responses of the SC decimator of Fig. 1 considering timing errors of $\pm 0.05T_s$ introduced in time slots 2 and 4.

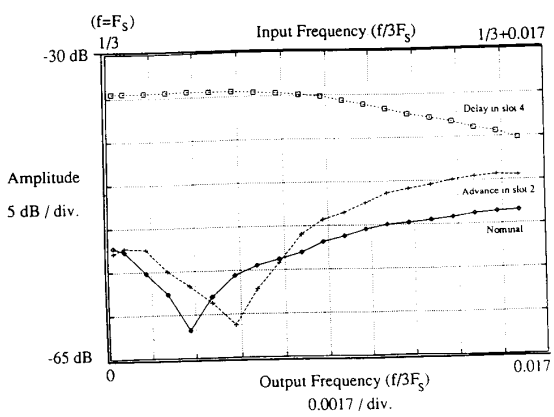


Fig. 15. Measured aliasing response in the passband corresponding to input frequencies in the first aliasing band around $F_s = 347.22$ kHz considering timing errors of $\pm 0.05T_s$ introduced in time slots 2 and 4.

response around F_s and $2F_s$, as illustrated in Fig. 14(b) [9], [14]. The experimental aliasing measurements results shown in Fig. 15 confirm such performance of the SC decimator for errors deliberately introduced in the switch timing. As referred to before, this arises because the aliasing response is strongly dependent on the timing accuracy of time slot 4 and which, being responsible for the modification of the frequency zeroes in the aliasing bands, may lead to significant variations of the level of rejection of the alias frequency components. Similar results are obtained for time slots 3 and 5, which are also responsible for sampling the input signal. The results obtained for timing errors introduced in time slot 2 show only a small error when compared with the nominal response, and which is consistent with our previous analysis.

V. Conclusions

We have demonstrated in this paper the practical feasibility of an SC decimator building block whose optimum implementation makes it possible to maximize the time period for the settling of the operational amplifiers with respect to the lower output sampling frequency. It was shown that for the same speed of the amplifiers this achieves an input oversampling ratio higher than in conventional SC filter designs and therefore leads to simpler continuous-time prefiltering requirements. The results obtained through the detailed evaluation of experimental IC prototype samples realized using a 1.8-μm CMOS technology confirm the robustness of the circuit under nonideal characteristics of both the amplifiers and the switching waveform generators controlling the operation of the circuit.

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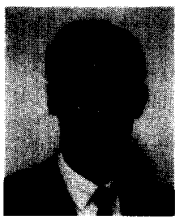

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