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MIXED SIGNAL LETTER

Double recycling technique for folded-cascode OTA

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Abstract Presented is a double-recycling folded cascode (DRFC) operational transconductance amplifier (OTA), demonstrating another phase of significant performance enhancement over the existing folded cascode, recycling folded cascode and improved recycling folded cascode counterparts. Theoretical treatments and computer simulations under the same 65 nm CMOS technology justify fairly the merits of the proposed DRFC OTA.

Keywords Operational transconductance amplifier (OTA) · Current recycling · Folded-cascode · CMOS

1 Introduction

Under the low-voltage constraints of nm-length CMOS technologies, current recycling has been emerged as a power- and area-efficient technique improving the general performances of folded-cascode (FC) operational transconductance amplifier (OTA). R. Assaad et al. [1] observed that $M3$ and $M4$ in the input stage of FC OTA (Fig. 1), originally just serving as bias current sources, can be exploited better in generating the effective transconductance. The resulting recycling folded cascode (RFC) OTA (Fig. 2a) demonstrates visibly increments of gain, bandwidth and slew rate without extra power or area. The significance of improvement is related with the factor K, which denotes the size ratio of the added current mirror ($M3$a–$M3$b or $M4$a–$M4$b). K is upper-bounded by the constraint of a symmetrical output slew rate in differential implementation, i.e., bias current of the input and output stages should be matched [2]. As such, the boosting factor of RFC's transconductance is practically limited to <3, no matter how large is the chosen K.

Recently, Y. L. Li et al. [3] proposed an improved recycling folded cascade (IRFC) OTA. As shown in Fig. 2(b), extra shunt current sources $M3$c and $M4$c are added to the input stage ($M13$ and $M14$ are entailed for matching the bias currents). Since the bias currents in the diode-connected transistors $M3$b and $M4$b are reduced, while those of $M1$b and $M2$b remain unaltered, this change allows using a higher K of 6. In this Letter, a double-recycling folded cascode (DRFC) OTA is proposed, which recycles the bias current of those shunt current sources once again, rendering itself higher performances with respect to those existing topologies. The details are described as follows.

2 Proposed DRFC OTA

Figure 3 shows the proposed DRFC OTA. The differential input pair is now replaced by a triplet ($M1$a–$M2$a, $M1$b–$M2$b, and $M1$c–$M2$c) and the shunt current sources ($M3$c–$M4$c) in Fig. 2(b) are replaced by current mirrors ($M3$c–$M3$d and $M4$c–$M4$d). In this way, the shunt bias currents can be re-used once again for further performance improvements, with no power and area overheads.

Since RFC, IRFC and the proposed DRFC OTAs are modified from the original FC OTA (Fig. 1), properly setting the current mirror ratios can lead to fair comparison of the four types of OTAs in terms of effective transconductance, output resistance and slew rate. Suppose the

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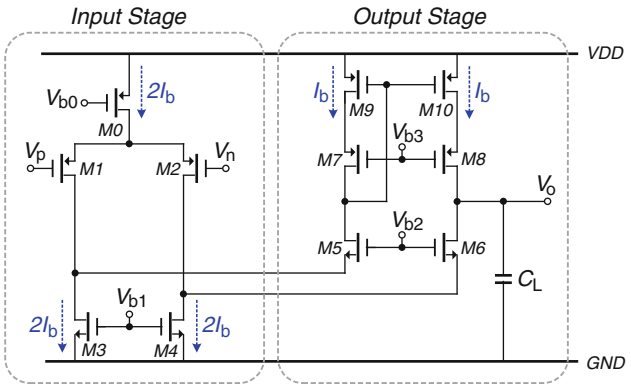

Fig. 1 A typical FC OTA

transconductance of FC OTA is G_m, then the effective transconductances of RFC, IRFC and DRFC OTAs can be given by,

$$G_{mRFC} = \left[1 + \frac{2(K-1)}{K+1}\right] \cdot G_m \tag{1}$$

$$G_{mIRFC} = \left[1 + \frac{2(K-1)(M+1)}{K+M+1}\right] \cdot G_m \tag{2}$$

$$G_{mDRFC} = \left[1 + \frac{2[K(2M+1) - (M+N+1)]}{K+M+N+1}\right] \cdot G_m \tag{3}$$

As mentioned before, the maximum G_{mRFC} cannot exceed three times of G_m due to the symmetric slew-rate constraint. The IRFC features much freedom (i.e., factor M) due to the added shunt current sources, but the improvement can be more substantial by recycling such shunt current sources once again. For instance, with practical values of K, M, and N as 5, 2, and 1, respectively, the transconductance improvement of the proposed DRFC is 5.67/2.43/1.42 times higher than FC/RFC/IRFC. Consequently, the gain and gain-bandwidth product (GBW) of the proposed DRFC are the highest among them.

For the output resistances of the four OTAs, they are given by,

$$R_{oFC} \approx g_{m6} r_{ds6} (r_{ds2} // r_{ds4}) // g_{m8} r_{ds8} r_{ds10} \tag{4}$$

$$R_{oRFC} \approx g_{m6} r_{ds6} \left(\frac{K+1}{K-1} r_{ds2} // \frac{K+1}{K} r_{ds4}\right) // g_{m8} r_{ds8} r_{ds10} \tag{5}$$

$$R_{oIRFC} \approx g_{m6} r_{ds6} \left(\frac{K+M+1}{K-M-1} r_{ds2} // \frac{K+M+1}{K} r_{ds4}\right) // g_{m8} r_{ds8} r_{ds10} \tag{6}$$

$$R_{oDRFC} \approx g_{m6} r_{ds6} \times \left(\frac{K+M+N+1}{K-M-N-1} r_{ds2} // \frac{K+N+M+1}{K} r_{ds4}\right) // g_{m8} r_{ds8} r_{ds10} \tag{7}$$

For the same values of K, M, and N as listed above, and with practical assumptions of $g_{m6} r_{ds6} \approx g_{m8} r_{ds8}$, $r_{ds10} \approx r_{ds2} // r_{ds4}$, and $r_{ds2} \approx r_{ds4}$, the output resistance of DRFC is roughly 1.8/1.2/1.13 times higher than that of FC/RFC/IRFC, due to the further reduced bias current in $M1a$, $M2a$, $M3a$, and $M4a$. This fact further secures the gain-enhancement feature of the proposed DRFC.

For the slew rates of the four OTAs, suppose the FC OTA has a slew rate of SR_{FC}, the corresponding slew rates of RFC, IRFC, and DRFC are given by,

$$SR_{RFC} = K \cdot SR_{FC} \tag{8}$$

$$SR_{IRFC} = \frac{K(K+1)}{(K+M+1)} \cdot SR_{FC} \tag{9}$$

$$SR_{DRFC} = \frac{K(M+1)}{(M+N+1)} \cdot SR_{FC}. \tag{10}$$

For the same values of K, M, and N as listed above, SR_{DRFC} (also SR_{IRFC}) is just 0.75 times of SR_{RFC}, but is still three times higher than SR_{FC}. Nevertheless, these slew rates are just theoretical maximum values. In practice, the

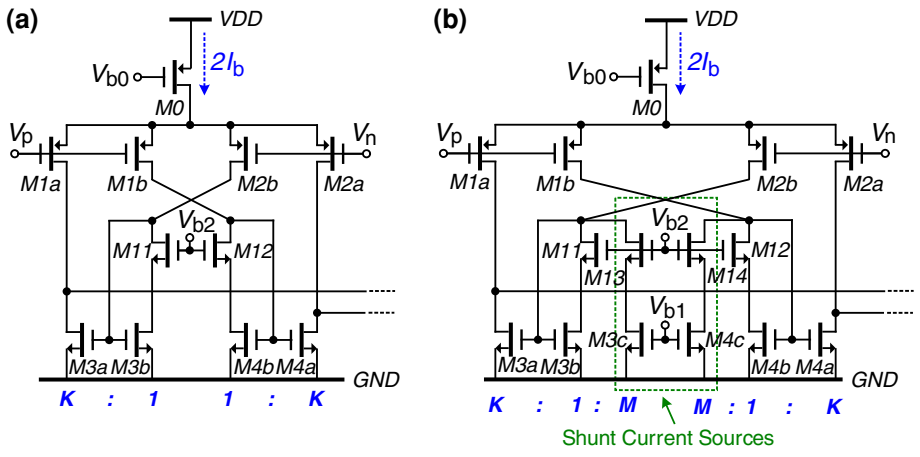

Fig. 2 **a** RFC OTA [1] and **b** IRFC OTA [3]. Output stage identical to FC OTA is omitted for clarity

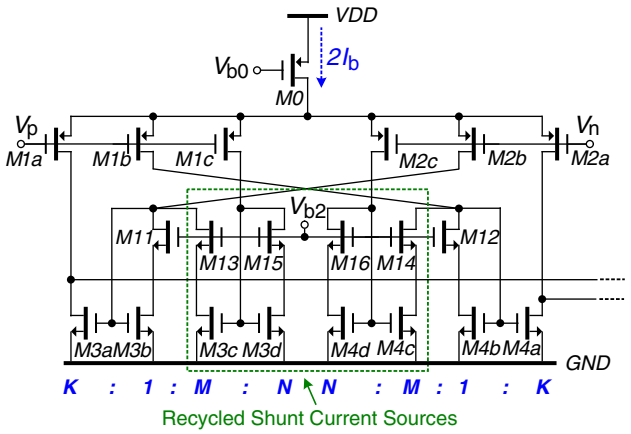

Fig. 3 Proposed DRFC OTA. Output stage identical to FC OTA is omitted for clarity

negative slew rate should be limited by the size and gate bias voltage of *M*6 while the positive slew rate could be restricted by the supply voltage. Furthermore, the duration of OTA's quasi-linear operation can contribute a significant portion to the settling behaviors. Due to the highest GBW of the proposed DRFC, its settling time should still be superior.

3 Simulation results

For a fair comparison among the four OTAs (FC, RFC, IRFC, and DRFC), they are designed under the same mirror factors ($K = 5, M = 2$ and $N = 1$), power and area budgets in a 65 nm CMOS technology. The closed-loop test is of inverting unity-gain feedback configuration [1, 3]. As shown in Fig. 4(a), the DRFC shows roughly 20/10/4 dB higher DC gain than that of FC/RFC/IRFC. The GBW of DRFC, also shown in Fig. 4(a) is boosted by 4.6/2.1/1.4 times in comparing with that of FC/RFC/IRFC. In the step-response tests (Fig. 4c), due to the highest gain and largest GBW of the proposed DRFC, it also exhibits the most accurate and fastest setting behaviors among them.

Other performance metrics are summarized in Table 1. The proposed DRFC, due to enhanced gain and GBW, also shows better close-loop linearity, input-referred noise and figure-of-merits (FOMs). The slew rates are of the similar level as IRFC as expected. Due to the higher GBW of the proposed DRFC, its phase margin appears worse than that of RFC and IRFC (Fig. 4b). However, if they are compared at the same GBW (203 MHz), the incurred phase margin reduction is limited to 6°/1.5° comparing with RFC/IRFC.

The recycling technique can be further expanded by shunting *M*3d and *M*4d with other current mirrors. The degree of performance improvement is subject to the targeted phase margin.

4 Conclusion

A DRFC OTA showing another step of significant performance enhancement over the existing FC, RFC and IRFC

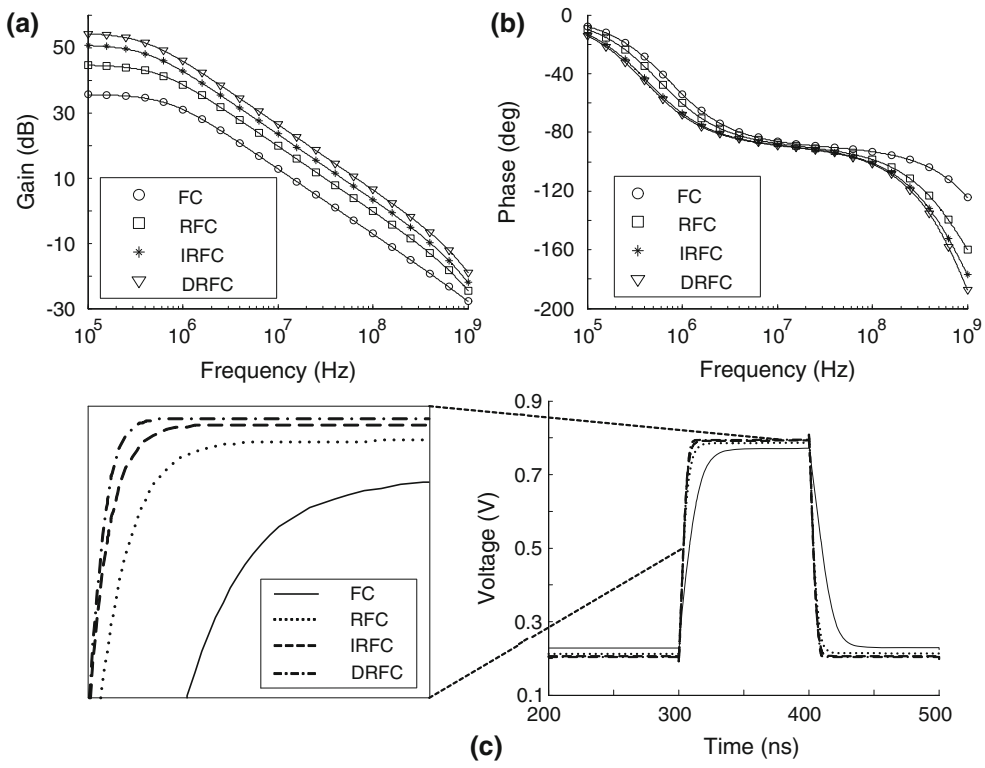

Fig. 4 Simulated (**a**) gain, **b** phase and **c** step responses of the proposed DRFC with respect to FC, RFC and IRFC OTAs

Table 1 Performance comparison of the four OTAs in the same 65 nm CMOS process

Parameters	FC	RFC	IRFC	DRFC
Supply voltage (V)	1			
Bias current (μA)	800			
Estimated area (μm^2)	20 × 24			
Capacitive load (pF)	10			
DC gain (dB)	35.6	44.7	50.8	54.5
GBW (MHz)	44.2	97.6	146.1	203.2
Phase margin (deg)	89.4	81.8	73.9	66.2
SR+/SR− (V/μs)	27.2/26.8	69.6/79.7	84.9/88.1	84.1/91.6
1% Settling time (T_s+/T_s-) (ns)	37.4/35.8	17.7/15.5	12.9/11.4	10.7/9.54
IM3, 0.6V_{pp} at 1 MHz (dB)	−38.6	−45.1	−51.1	−54.4
Input referred noise (1 Hz–100 MHz) (μV_{rms})	36.0	31.6	26.0	25.8
FoM_1 (MHz·pF/mA)	552.5	1,220	1,826	2,540
FoM_2 [(V/μs)·pF/mA]	337.5	746.5	865.0	878.5

Average slew rate (SR) is used to calculate FoM_2

counterparts is proposed. By recycling the shunt current sources in the input stage of IRFC OTA once again, the effective gain and GBW can be further boosted with no extra power and area, yet small reduction of phase margin. The results have been justified systematically and computationally in 65 nm CMOS.

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