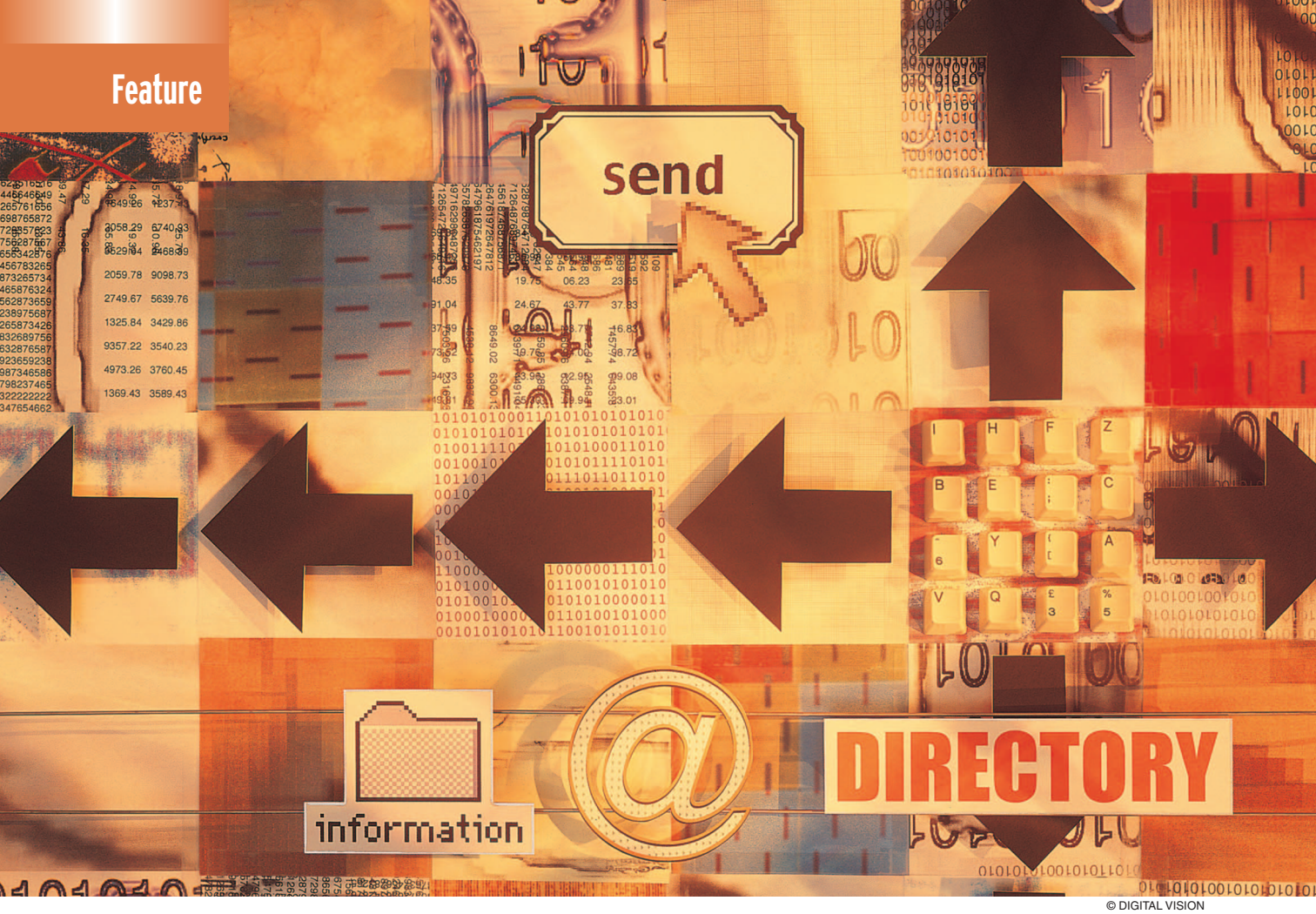

Two-Stage Operational Amplifiers:

Power-and-Area-Efficient Frequency Compensation for Driving a Wide Range of Capacitive Load

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Abstract

Operational amplifiers (OpAmps) have found extensive applications in analog circuits and systems for communications, consumer electronics, controls and signal conversion. Two-stage OpAmps with frequency compensation are popular for driving capacitive loads while ensuring sufficient gain and stability. Frequency compensation techniques have been evolving over the last decades in distinct applications. In particular, power-and-area-efficent two-stage OpAmps capable of driving a wide-range capacitive load are demanded for low-dropout regulators (LDOs) or LCD-panel drivers. *Capacitor multipliers* (CMs) have emerged as one of the best solutions to implement such kind of OpAmps.

This article reviews, for the first time, the state-of-the-art CMs for two-stage OpAmps before describing a novel embedded-CM technique, i.e., the CM as being part of the input stage of the OpAmp, effectively minimizing the physical size of the compensation capacitors while improving the slew-rate with no extra power consumption. Moreover, unlike the classical Miller compensation technique that can lead to an undesired right-half-plane (RHP) zero, a constructive left-half-plane (LHP) zero, is created, that can improve the phase margin (PM). Comparing with the state-of-the-art current-buffer and CM compensation topologies the proposed solution also features simpler circuitry. The technique can be further incorporated with a class-AB output stage to speed up the OpAmp's transient responses with low quiescent power. A descriptive design example capable of driving capacitive loads $\geq$ 50 pF is systematically optimized in a 0.35-μm CMOS process. Finally, a few techniques are outlined which allow the combination of current-buffer-based Miller compensation with more sophisticated CMs, or a pole-zero pair (lead network), to further enhance the driving capability of two-stage OpAmps.

I. Introduction

Operational amplifiers (OpAmps) have been at the core of a wide range of analog circuits such as analog-to-digital converters, low-dropout regulators (LDOs) and active filters [1]. Portable systems, as the wireless transceivers, integrate most of these functions, appealing for more high-performance OpAmps to meet the increasingly tight power and area budgets. Particularly, OpAmps for LCD panels or headphone drivers require a wide-range capacitive load driving capability [2]–[3]. A low-quiescent-power small-area OpAmp that supports a *wide* range of load capacitance constitutes the motivation of improving the existing frequency compensation techniques. The conventional multi-stage OpAmp topology (gain stages $\geq$3) does not appear as a wise choice since the frequency compensation leads to large reduction of the gain-bandwidth (GBW) product, and almost none of the published topologies are suitable for driving a wide range of capacitive load with low-power consumption [4]. On the other hand, a two-stage OpAmp topology [Fig. 1(a)] is selected as it exhibits more sensible and simpler tradeoffs among the DC gain, GBW, quiescent power and output swing. As it is well known, two-stage OpAmps also require frequency compensation to obtain a stable closed-loop operation. However, to the authors' knowledge, during the past several decades only four compensation schemes shown in Fig. 1(b)–(e) have been developed, mainly with the aim of eliminating the right-half-plane (RHP) zero as shown in Fig. 1(a), rather than handling highly variable capacitive loads [5]–[18]. To choose an optimum topology coping with this challenge, the local feedback loops of these circuit structures can be interpreted as being able to cut the loops according to that in Fig. 1(a).

The magnitude plots of the loop gain $T(s)$ of the different schemes (from Fig. 1) are given in Fig. 2. Comparing them, SMC, MCVB, MCNR, and MCFT have the same unity-gain frequency (UGF) ω_μ while the UGF of MCCB is C_m/C_{p1} times higher than them under the same configuration of circuit parameters. The abundant UGF of MCCB can be used to trade for small power and area. Therefore, MCCB is essentially more power-and-area efficient than other compensation schemes, though the capability of driving small capacitive loads is limited by the parasitic pole $(C_L + C_m)/(R_c C_L C_m)$ generated by the current buffer. Another issue associated with MCCB is related with the fact that when the capacitive load is heavy, in the order of hundreds of pF, the compensation capacitor C_m must be set to a large value for driving the load, and more importantly maintaining a reasonable gain of the first stage [19]. Moreover, large C_m not only occupies a great amount of silicon area but significantly lowers the OpAmp's slew rate. A feasible solution to overcome this difficulty utilizes capacitor-multipliers (CMs), since CMs minimize the physical size of the capacitors while retaining the effective

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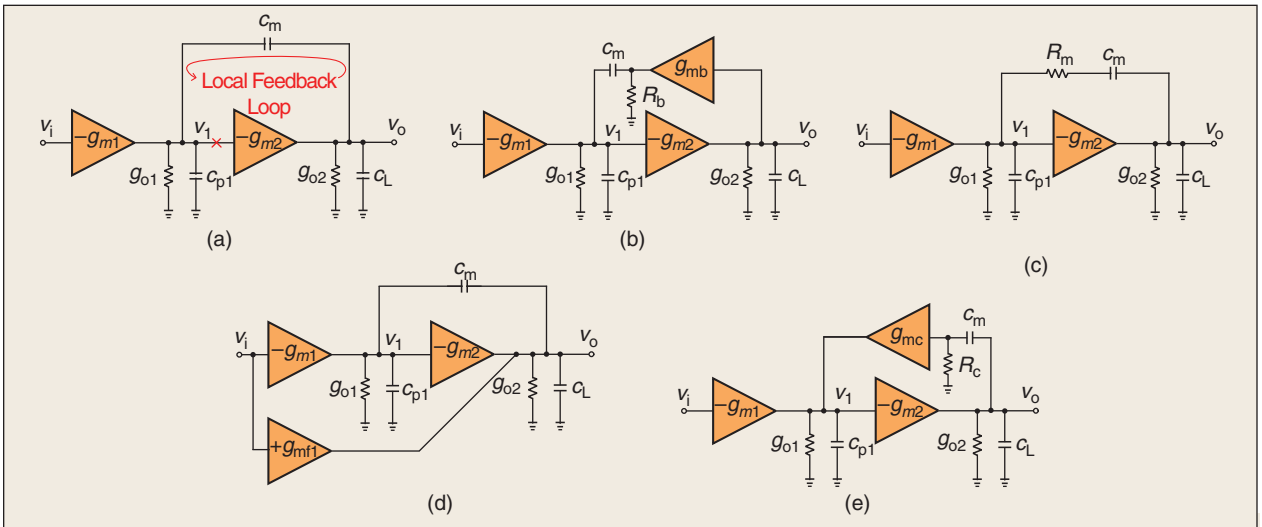

Figure 1. Compensation schemes for two-stage OpAmps: (a) simple Miller compensation (SMC), (b) Miller compensation with voltage buffer (MCVB), (c) Miller compensation with nulling resistor (MCNR), (d) Miller compensation with feedforward transconductance (MCFT), and (e) Miller compensation with current buffer (MCCB).

capacitance required. Until now, many effective CMs have been proposed. For instance, in [20], a current-mode CM based on current mirrors was reported. However, this method still cannot achieve a high multiplication factor owing to the power and bandwidth constraints. Although the approaches from [21]–[23] boost the multiplication factor by at least an order of magnitude, they introduce additional poles located at relatively low frequencies, degrading the speed of the OpAmp. In addition, to realize the bidirectional CM in [24] a complicated voltage buffer is entailed, increasing the circuit complexity and calling for additional power. Last but not least, most of the aforementioned current-buffers or CMs require add-on bias circuits and subsequently incur in systematic offset voltage and larger parasitic capacitance [25].

Addressing the above concerns a two-stage OpAmp with embedded CM frequency compensation is proposed. The key features of the proposed OpAmp are: 1) no unwanted RHP zero, while a useful left-hand-plane (LHP) zero is induced into the OpAmp's frequency response to improve the stability, resulting in a highly stable OpAmp over a wide-range of capacitive loads (≥50 pF in the design example); 2) no extra bias circuit and power are required as the CM is embedded into the input stage of the OpAmp; 3) the two compensation capacitors are reduced to a very reasonable sub-pF range, leading to a very fast transient response and compact implementation.

This article is organized as follows: Section II reviews the state-of-the-art CM techniques. The embedded CM technique is introduced and analyzed in Section III. Section IV describes the design details and results of a design example. Section V depicts two potential compensation techniques to further extend the range of driving capacitive loads. The summary is drawn in Section VI.

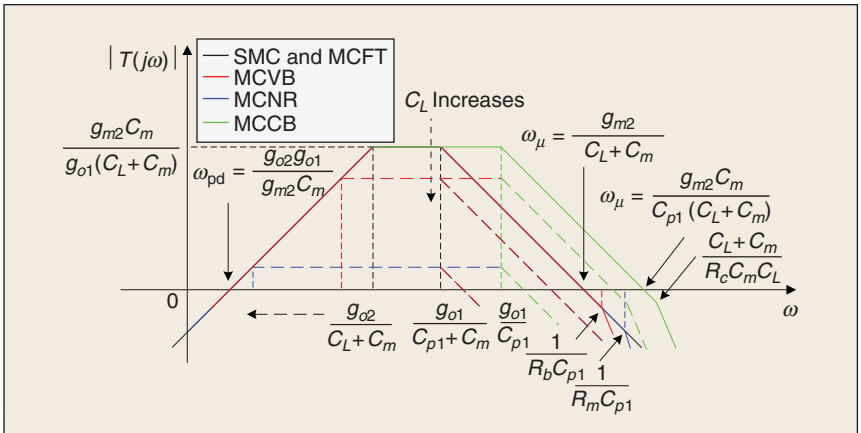

Figure 2. Magnitude responses of the local feedback loops, with existing compensation techniques, in two-stage OpAmps.

II. Review of State-of-the-Art CM Techniques

A. Generalized Operation Principles

The principles of CM are based on scaling the impedance or admittance seen from the input port of the π circuit as shown

in Fig. 3(a). If more input current is produced under the same input voltage, the equivalent input admittance increases since the effective input admittance of π is proportional to its input current. In case of a capacitive admittance, larger equivalent capacitance is achieved.

There are in general two alternatives to boost the effective capacitance, which are depicted in Figs. 3(b), and (c), respectively [26]. In Fig. 3(b), a voltage-controlled voltage source (VCVS) is connected in series with a capacitor C. The voltage gain, $-A_v$, of the VCVS amplifies the admittance of the capacitor, sC, yielding the corresponding input admittance,

$$Y_{in} = \frac{I_{in}}{V_{in}} = s(A_v + 1)C. \tag{1}$$

Figure 3(c) shows the idea of another method that exploits a current-controlled current source (CCCS) in parallel with C to directly increase the current flowing into the input. Since the current gain of the CCCS is K, the equivalent capacitance is determined by the following equations,

$$Y_{in} = \frac{I_{in}}{V_{in}} = s(K+1)C \Rightarrow C_{eq} = (K+1)C. \tag{2}$$

The method depending on a VCVS is usually called a voltage-mode capacitor multiplier (V-CM) while the other relying on a CCCS is termed as a current-mode capacitor multiplier (C-CM) as the embodiments of a VCVS and a CCCS are corresponding to voltage and current amplifiers, respectively.

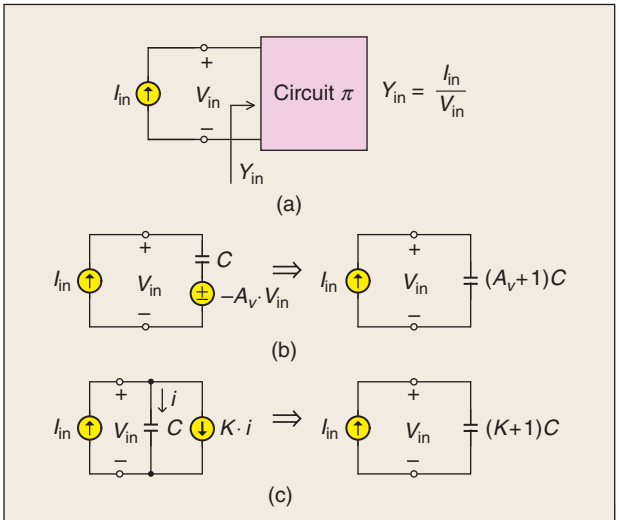

Figure 3. Operation principles of CM: (a) impedance scaling, (b) CM based on VCVS, (c) CM based on CCCS.

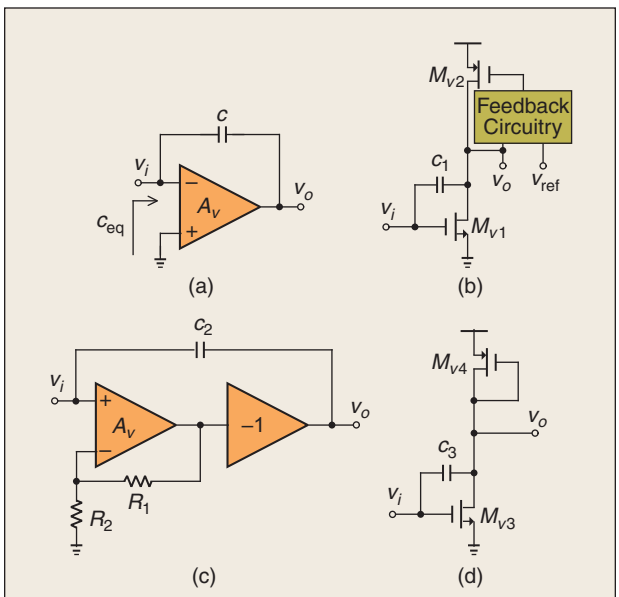

Figure 4. (a) Basic schematic of V-CM and its alternative circuit implementations: (b) [4], (c) [28], and (d) [29].

B. CM Realization

1) Voltage-Mode CMs

When considering the circuit implementation of V-CMs, they are common for compensating feedback circuits such as amplifiers, phase-locked loops (PLLs) and power converters by employing the well-known Miller effect [27]–[29]. According to Fig. 4(a), the effective capacitance of the input is capacitor C multiplied by a factor of $1+A_v$. The remarkable advantage of V-CM is its convenience in obtaining a large effective capacitance value from a small physical capacitor. Yet, the voltage at the output might be pulled up or down to the power rails since the amplifier is normally a high-gain stage. The circuit is also susceptible to instability if there is no extra feedback loop applied to control the dc operating point, as shown in Fig. 4(b) [4]. The feedback circuitry calls for extra elements and increases the power. Figure 4(c) suggests a circuit realization that overcomes this problem [28]. A non-inverting CMOS amplifier with a series-resistor feedback is able to solve the issue, but the multiplication factor is still limited by a small resistor ratio. Besides, an inverting unity-gain buffer is needed to ensure no input dc current because such dc current leads to large leakage and voltage spurs in PLLs. Although only a small multiplication factor is achieved, the V-CM shown in Fig. 3(d) exhibits a good balance between complexity, bandwidth, and quiescent current consumption [29]. Generally, V-CMs are unsuitable for large-swing applications.

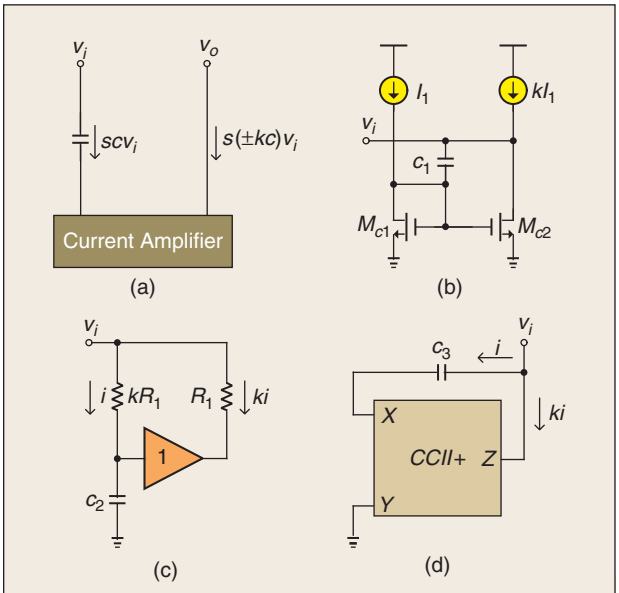

Figure 5. (a) Basic schematic of C-CM and its alternative circuit implementations: (b) [20], (c) [24], [35], and (d) [38].

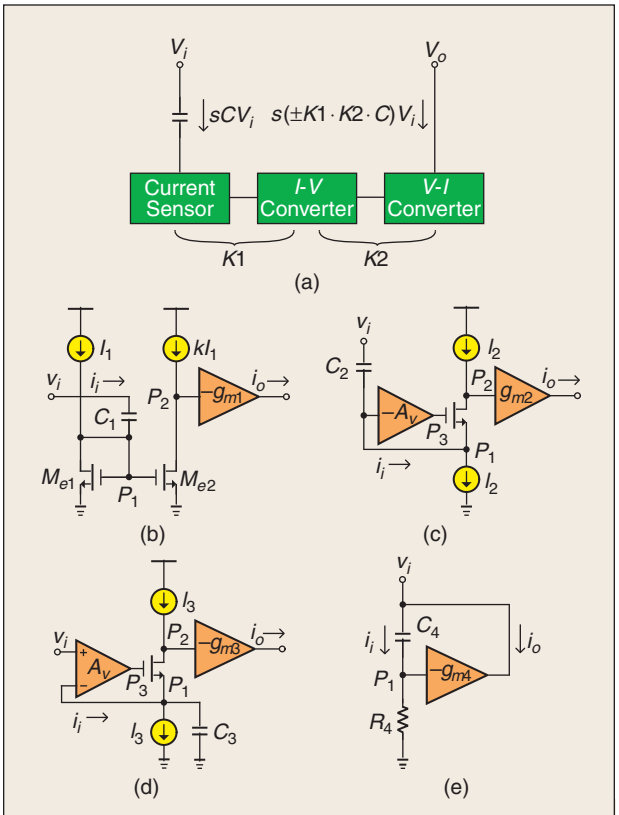

Figure 6. (a) Basic schematic of enhanced C-CM and its alternative circuit implementations: (b) proposed, (c) [21], [22], (d) [23], [33], and (e) [3].

2) Current-Mode CMs

The C-CMs shown in Fig. 5(a) have no similar restriction on the output voltage and, consequently, have gained more attention recently, in realizing active filters, PLLs and DC-DC converters, than V-CMs. The current-mirror based structure depicted in Fig. 5(b) obtains accurate capacitance multiplication, owing to its inherent simplicity. Also, a large amplification factor can be achieved if the constraints of power consumption and the parasitic pole at the mirror are relaxed [20]. Cascode current mirrors with long-channel transistors are utilized to minimize the leakage current at the output [30]–[34]. To amplify a grounded capacitor, different implementations have been proposed [24], [35]–[38]. The method shown in Fig. 5(c) utilizes a voltage follower and resistors with ratio k to emulate a current amplifier. Thus, an equivalent capacitance is obtained by the value of C_2 multiplied by k. But large resistors are required to minimize the current leaking into the follower's output terminal. Since the current through the terminal X of the second generation current conveyor (CCII) is amplified and dumped out at the terminal Z, and the voltage at X also follows that at Y, the CCII befits both floating and grounded capacitors (only CCII+ is shown in Fig. 5(d)). Recently, in order to reduce the area of a frequency synthesizer considerably, a capacitance multiplication factor of around 2000× is achieved in [39] by adopting a general impedance converter (GIC). However, these techniques are mainly targeted for low-frequency applications because the auxiliary components such as the voltage buffers in [24] and [28] introduce low-frequency parasitic poles that severely limit their frequency responses. Besides, the GIC requires two additional high-performance OpAmps and a big resistor of 2 MΩ, further aggravating the overheads.

3) Enhanced Current-Mode CMs

The concept of enhanced C-CMs combining the beneficial characteristics of both V-CMs and C-CMs are depicted in Fig. 6(a). A current sensor composed of a low-impedance element (typically a current buffer) is employed to convert the input voltage V_i into current i_i. i_i is then amplified in the voltage domain by a current-to-voltage (I-V) converter. Next, a voltage to current (V-I) converter turns the amplified voltage back into current for further magnification. Since the realization of a simple *I-V* converter or *V-I* converter can be done by several transistors, the enhanced C-CMs induce less circuit overhead while achieving a high multiplication factor. The basic architecture of the proposed CM is depicted in Fig. 6(b). The $-g_{m1}$ cell is as simple as a MOS transistor but the multiplication factor is as large as $g_{m1}r_{o1}$ (r_{o1} represents the output resistance of the previous *I-V* converter). However, $g_{m1}r_{o1}$ cannot be too large to make the effect of the parasitic pole

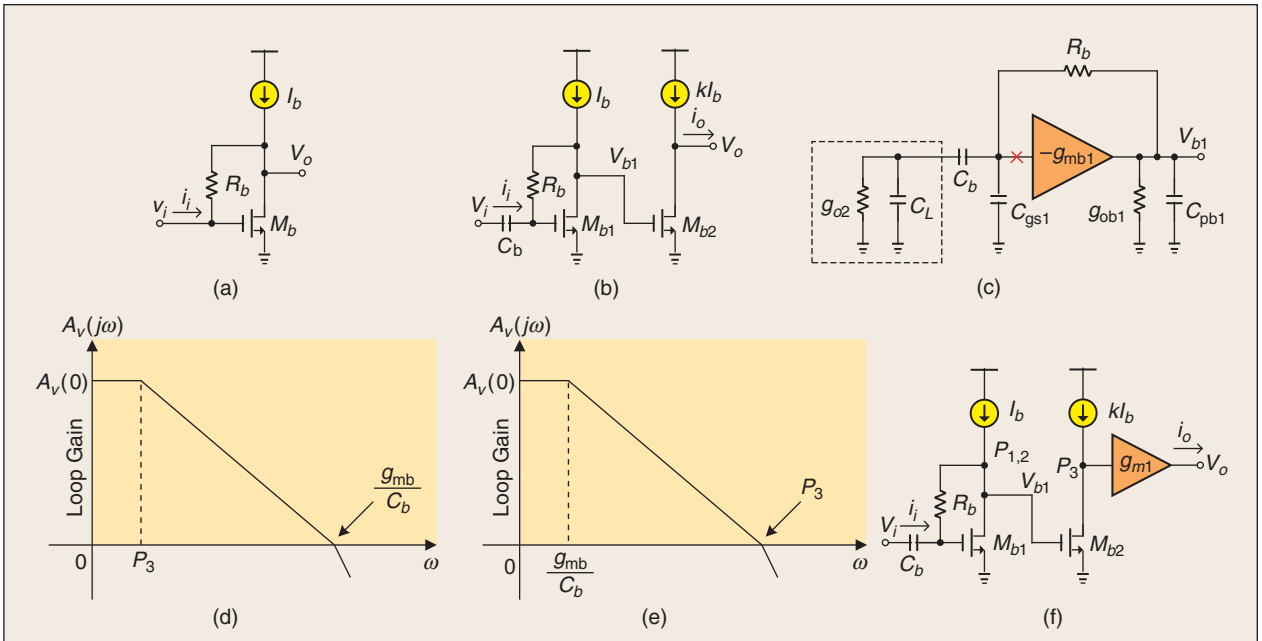

Figure 7. (a) Advanced I-V converter, (b) Proposed CM, (c) Small-signal equivalent circuit of the input part in the proposed CM, (d) Frequency characteristics of the local feedback loop: case I, (e) Case II, (f) Proposed enhanced CM with the advanced I-V converter.

P_2 (formed at the input of the $-g_{m1}$) obvious. Another drawback of this structure is that the input impedance of the current sensor is insufficiently low, which introduces another parasitic pole P_1 (formed by C_1 and the input resistance of the current mirror). To push P_1 at a much higher frequency, the implementations in Figs. 6(c) and (d) utilize local feedbacks to reduce the input impedance at the feedback nodes [21]–[23], [33]. Although the above-mentioned impedance-attenuation technique is more power efficient than just a decrease in the impedance (through increasing bias current), a third parasitic pole P_3 (introduced by the local feedback amplifier) is induced in the feedback loop, lowering the stability of the overall circuit. A simpler solution is presented in Figure 6(e) which exhibits a passive-oriented realization that employs a relative small resistor R_4 as a current sensor and an *I-V* converter [3]. In addition, a more reasonable multiplication factor ($g_{m4}R_4 + 1$) is obtained with just one parasitic pole P_1 (formed through C_4 and R_4) induced at high frequency.

III. Embedded CM Technique

The core principle underlying the proposed CM is to employ an advanced *I-V* converter with moderate gain and excellent frequency characteristic, to replace the current sensors or *I-V* converters as discussed previously. The *I-V* converter is shown in Fig. 7(a), which is widely adopted for transforming photodiode current into voltage in optical receivers [40], [41]. The resistive feedback across M_b not only ensures the input with low impedance $1/g_{mb}$ (g_{mb} is the transconductance of M_b) but provides flexible output impedance approximately equal to R_b, which can be more accurately controlled than the output resistance of a transistor. Furthermore, the voltage gain of the *I-V* converter is ($g_{mb}R_b - 1$) while the UGF is approximately g_{mb}/C_{pb}, where C_{pb} is the parasitic capacitance at the output node. This suggests that the gain and bandwidth of the *I-V* converter can be adjusted independently. This degree of freedom turns this CM into the best choice for achieving a small on-chip capacitor and highest bandwidth, simultaneously, among existing CMs.

Fig. 7(b) depicts the proposed CM [42]–[44]. The capacitance multiplication factor can be further boosted by the following *V-I* converter with larger bias current kI_b. Since R_b introduces a local feedback, the stability of this loop should be checked first to ensure that it would be stable when the proposed CM is applied to compensating OpAmps. As shown in Fig. 7(c), the small-signal equivalent circuit models the input part of the proposed CM and the dashed part (g_{o2} and C_L) represents the open-loop output impedance of uncompensated two-stage OpAmps. C_{gs1} denotes the parasitic capacitance at the gate of M_{b1}. g_{ob1}, and C_{pb1} are the parasitic capacitance and output conductance at the drain of M_{b1}, respectively. The loop transfer function

$T_i(s)$ is calculated by cutting the loop at the input of $-g_{mb1}$, and it would be approximately given by

$$T_i(s) \approx -\frac{g_{mb1}}{g_{ob1}\left(1+s\frac{C_b}{g_{ob1}}\right)(1+sR_bC_{pb1})} \text{ if } \frac{g_{o2}}{C_L} \ll \frac{g_{ob1}}{C_b} < \frac{1}{R_bC_b}. \tag{3}$$

Apparently, g_{ob1}/C_b is the dominant pole while $1/(R_bC_{pb1})$ is the non-dominant pole. To achieve a PM $\geq 45°$, the non-dominant pole must be higher than the loop's GBW, which means that the following inequality should hold,

$$\frac{1}{R_bC_{pb1}} \geq \frac{g_{mb}}{C_b} \Leftrightarrow \frac{C_b}{C_{pb1}} \geq g_{mb}R_b. \tag{4}$$

This requirement is easily satisfied because $g_{mb}R_b$ is typically in the order of ten and C_b is much larger than C_{pb1}. In contrast, the conditions on compensating local feedback loops in former enhanced CMs, illustrated in Figs. 6(c) and (d), are quite stringent. In practice, the local feedback amplifier is commonly realized by one transistor or a simple differential-to-single-ended amplifier. Its frequency response can be well described by a single-pole system, i.e.,

$$A_v(s) = \frac{A_v(0)}{1+\frac{s}{P_3}} = \frac{g_mr_o}{1+\frac{s}{r_oC_p}}, \tag{5}$$

where g_m, r_o and C_p are the local amplifier's transconductance, output resistance, and output capacitance, respectively. There are two alternatives to stabilize the local loop with the assumption of unity-gain in the source follower stage. First, as depicted in Fig. 7(d) the dominant pole of the local loop is P_3 located at the output of the local amplifier. The non-dominant pole occurring at the source follower must be beyond the loop's GBW to obtain a PM of at least 45°, which is mathematically expressed as

$$\frac{g_{mb}}{C_b} \geq A_v(0)\cdot P_3 = \frac{g_m}{C_p} \Leftrightarrow C_p \geq \frac{g_m}{g_{mb}}C_b. \tag{6}$$

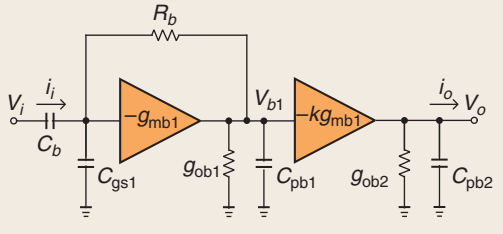

Figure 8. Small-signal equivalent circuit of the proposed CM.

According to (6), the size of C_p is required to be nearly as large as C_b, given that g_m and g_{mb} have the same order of magnitude, increasing the silicon area. Moreover, the closed-loop bandwidth is not improved in comparison with a simple source follower. Thus, this case will not be effective in the reduction of the size of CM's physical capacitor.

In a second possibility, the loop is characterized with P_3 as the non-dominant pole in Fig. 7(e) and the above phase-margin requirement changes to,

$$\frac{1}{r_oC_p} \geq A_v(0)\cdot\frac{g_{mb}}{C_b} \Leftrightarrow C_b > (g_mg_{mb}r_o^2)C_p. \tag{7}$$

Obviously, this case is also not suitable for capacitance multiplication with very small C_b. For instance, assuming C_p is 10 fF, and g_mr_o and $g_{mb}r_o$ are both equal to ten, roughly the same as $g_{mb}R_b$, the resulting condition of $C_b \geq 1$ pF would still be required, while (4) for the proposed CM will be sufficiently fulfilled in this case.

Therefore, the proposed CM is the most desirable for reducing the dimension of the physical capacitor and it is more powerful in terms of building an enhanced CM, as shown in Fig. 7(f).

In order to compare the high-frequency performance between the proposed CM and other types of CMs and choose a proper mirroring factor k, the small-signal equivalent model of the proposed CM is given in Fig. 8, with g_{ob2} and C_{pb2} denoting the parasitic capacitance and output conductance at the drain of M_{b2}, respectively. Under the assumptions that $C_b \gg C_{gs1}$, C_{pb1} and $(1/g_{ob1}) \gg R_b > (1/g_{mb1})$, the transfer function of the CM can be approximately given by,

$$Y_i = \frac{i_o}{v_i} \approx \frac{sMC_b}{1+\frac{s}{a_0}+\frac{s^2}{a_0a_1}}, \tag{8}$$

where $M = k(g_{mb1}R_b - 1)$ is the multiplication factor, a_0 and a_1 are g_{mb1}/C_b and $1/(R_bC_{pb1})$, respectively. The effective bandwidth of a CM, B_{CM}, is defined at the frequency where the phase magnitude drops by 45° (for a positive CM, its phase magnitude decreases from 90° to 45° while an inverting CM has 45° reduction from –90° to –135°). Hence, the B_{CM} is determined by,

$$\arctan\left[\frac{\frac{B_{CM}}{a_0}}{1-\frac{(B_{CM})^2}{a_0a_1}}\right] = 45°. \tag{9}$$

Solving (9), B_{CM} is obtained as,

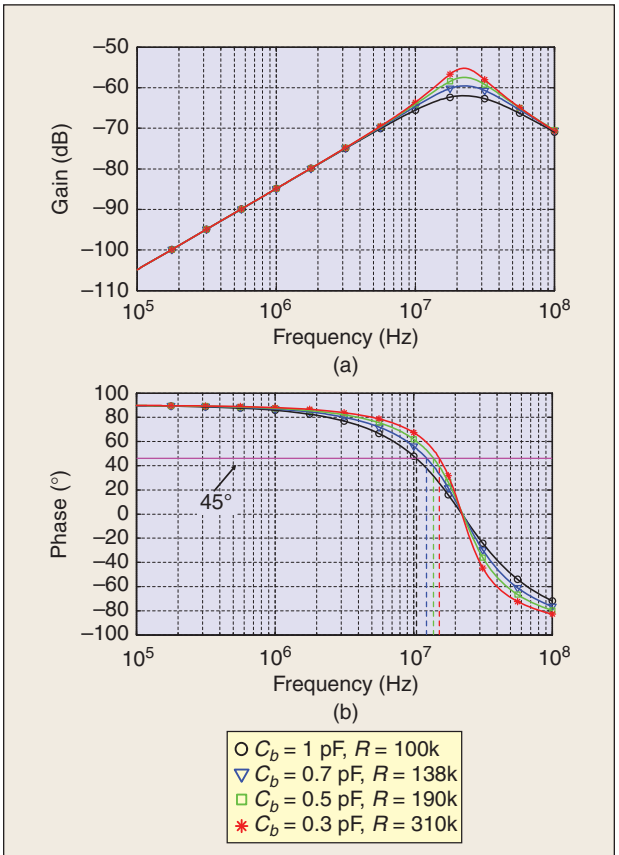

Figure 9. (a) Magnitude responses of the proposed CM under different C_b and R_b. (b) Phase responses of the proposed CM under different C_b and R_b.

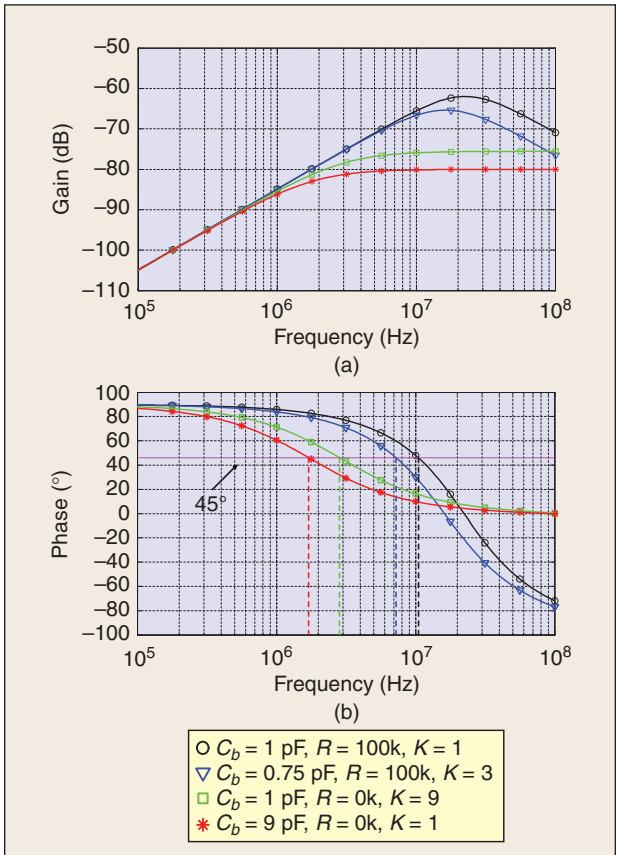

Figure 10. Frequency performance comparison between current-mirror CM and the proposed CM: (a) Magnitude responses; (b) Phase responses.

$$B_{CM} = \frac{\sqrt{a_1^2 + 4a_0a_1} - a_1}{2}. \tag{10}$$

It can be observed that B_{CM} is not affected by the type of poles, no matter they are two real poles or a complex pair (the damping factor must be no less than 1/2 according to (4)). Providing that the effective capacitance is a given constraint, the B_{CM} can be extended by increasing the value of a_0 (i.e. reducing the value of C_b while increasing R_b to fully utilize the characteristic of small parasitic C_{pb}). For example, if $a_1 \geq 2a_0$ is the requirement for a stable local loop, B_{CM} is $\geq 0.732a_0$ (i.e. 0.732 (g_{mb1}/C_b)).

In terms of the power budget, the bias current can be accurately measured by the transconductance of all transistors [17]. The total transconductance of each CM is $2g_{mb1}$. The current-mirror CM's bandwidth B_{CM-1} is given by,

$$B_{CM-1} = \frac{2g_{mb1}}{(M+1)C_b}. \tag{11}$$

From (11), it would be possible to demonstrate that the frequency performance of the proposed CM is superior, when compared with the current-mirror CM because M must be set to be greater than one to perform capacitance amplification. As for other complex CMs, due to the existence of parasitic low-frequency poles, their bandwidth is even smaller than that of a current-mirror CM.

To prove the forgoing assertions, different designs aiming to obtain 9-pF effective capacitance with 10-μA quiescent current dissipation are carried out. Figure 9(a) and (b) shows the frequency characterization of the proposed CMs with different values of R_b and C_b. As shown in Fig. 9(b), B_{CM} of the proposed CM's increases with a larger R_b that corresponds to a smaller C_b. However, the magnitude peaking also grows fast as shown in Fig. 9(a); the upper boundary of B_{CM} is limited by the stability imposed by the local resistive feedback.

Figure 10(a) and (b) shows the magnitude and phase responses of different CMs, respectively. Notice that the phase responses of the basic current mirror and current-mirror CM are intentionally inverted from drop, beginning

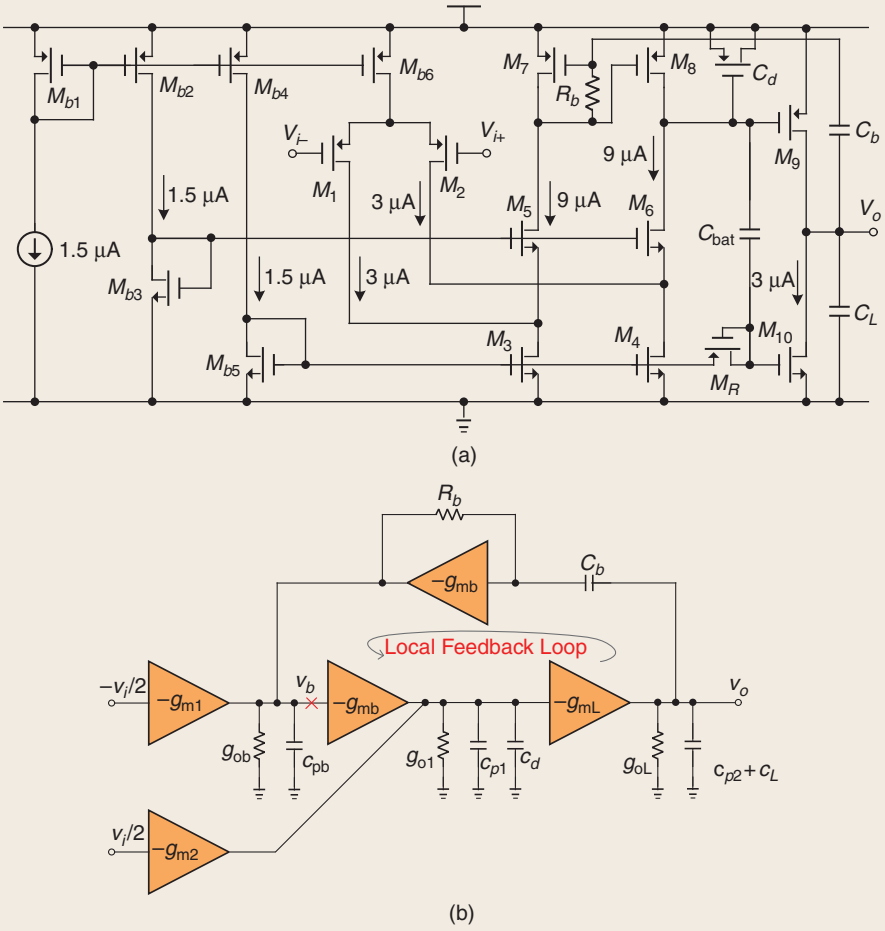

Figure 11. (a) Proposed two-stage OpAmp and (b) its equivalent small-signal model.

at –90° and going to 90° for benchmarking. The basic current mirror without the capacitance multiplication capability features the lowest bandwidth. The bandwidth of the current mirror CM, marked by the red line, is much narrower than that of the proposed CM, denoted by the black line. The blue curve describes the frequency performance of the proposed CM with $k = 3$. Although this CM uses a C_b of only 0.75 pF, its bandwidth decrease will be larger than 25%. Thus, for wide-band applications, the proposed CM with a mirror ratio $k = 1$ it is the preferred choice.

Finally, from the viewpoint of circuit realization, embedding the proposed CM has four advantages: *1) no extra voltage headroom; 2) no additional static power dissipation; 3) no systematic offset voltage, and 4) no add-on parasitic capacitance*, because the function of mirroring current in the two branches is maintained, regardless of the feedback resistor R_b. Therefore, it can be utilized as a general cell inserted in circuits, with the existing current mirrors in the signal path, to achieve capacitance multiplication. A good example is that given in [42] where the cell is embedded in the first stage of the error amplifier to realize a high-speed, area-and-power efficient LDO for large-load current applications.

IV. Two-Stage OpAmp with Embedded CM Frequency Compensation

The full schematic of the proposed two-stage OpAmp is shown in Fig. 11(a). The first stage is a folded cascode OTA composed by transistors M_{b6}, and $M_1 - M_8$. The embedded CM is realized by reusing a current mirror $M_7 - M_8$ with a resistor R_b connected between the gate and drain of M_7. C_b is the key compensation capacitor. Transistors M_9 and M_{10} realize the second stage of the OpAmp. In order to obtain symmetrical slew-rates, a class-AB output stage is adopted. The class-AB function is provided by adding a diode-connected PMOS transistor M_R and a capacitor C_{bat} [45]. Since M_R acts like a very large resistor, the charging and discharging time at the gate of M_{10} is relatively long in comparison with the circuit operating speed. Therefore, the voltage variation at the gate of M_9 can be transferred to the gate of M_{10} with negligible loss during dynamic operation. Figure 11(b) shows the

small-signal equivalent model of the OpAmp. g_{m1} and g_{m2} represent the transconductance of M_1 and M_2, respectively, with $g_{m1} = g_{m2}$. The transconductance of M_7 and M_8 is g_{mb}. g_{mL} is the sum of M_9 and M_{10}'s transconductance, which includes the ac effect of the class-AB stage. The output conductance of each stage is denoted by g_{ob}, g_{o1}, and g_{oL}, respectively. C_{pb}, C_{p1}, and C_{p2} that lumped into the load capacitor C_L, represent the parasitic capacitances at the corresponding stages. A small C_b amplified by the proposed CM has large effective capacitance and causes the two poles associated with the input and output nodes of the second stage to split apart, leading to widely spaced dominant and non-dominant poles. The purpose of C_d is to adjust the position of the first non-dominant pole and handle a wide range of load capacitance. An area-efficient MOSCAP befits C_d for area reduction.

A. Local Feedback Loop

Analysis of the Proposed OpAmp

When the proposed CM is incorporated into the two-stage OpAmp, it introduces a local feedback loop around the second stage. To analyze the stability of the OpAmp under varying capacitive load, the local loop is broken at the node V_b as shown in Fig. 11(b). In addition to the assumptions made for analyzing the proposed CM, the local transfer function $T_L(s)$ is calculated with the following assumptions:

1) The gain of all the stages are much greater than 1;
2) The parasitic capacitance C_{pb}, C_{p1}, and C_{p2} are much smaller than C_b, while C_L is much larger than C_b.

Hence, $T_L(s)$ is given by,

$$T_L(s) \approx -\frac{sg_{mL}(g_{mb}R_b - 1)C_b}{g_{o1}g_{oL}\left(1+\frac{s}{\omega_{pd}}\right)\left(1+\frac{s}{\omega_{p1}}\right)\left(1+s\frac{C_b}{g_{mb}}+s^2\frac{C_bR_bC_{pb}}{g_{mb}}\right)}. \quad (12)$$

The magnitude plot of $T_L(s)$ is shown in Fig. 12 with increasingly large C_L. The dominant pole of the local loop is $\omega_{pd} = g_{oL}/C_L$ while the first non-dominant pole is $\omega_{p1} = g_{o1}/(C_{p1} + C_d)$. ω_μ is the UGF of the local loop and other two high-frequency poles are produced by the CM, which are g_{mb}/C_b, and $1/(R_bC_{pb})$, respectively. Of course, they might exhibit the form of two complex poles.

As described in Fig. 12, when C_L is small, ω_μ might be located close to, g_{mb}/C_b and $1/(R_bC_{pb})$. With much smaller C_L, the PM of the local loop worsens to cause a significant peaking in the overall transfer function of the OpAmp [27]. Therefore, the OpAmp has a lower limit for driving capacitive loads. To evaluate the limit, the PM

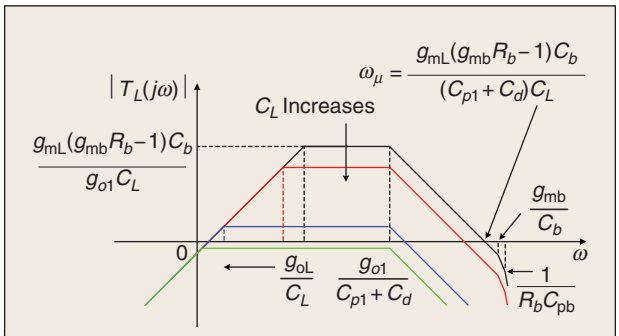

Figure 12. Magnitude response of the local loop in the proposed OpAmp as C_L increases.

of the local loop is assumed to be larger than 45°, and expressed as

$$\mathrm{PM}_{\mathrm{local}} \approx 90° - \arctan\frac{\frac{\omega_\mu}{g_{mb}/C_b}}{1-\frac{\omega_\mu^2}{g_{mb}/C_b}R_bC_{pb}} \geq 45°. \quad (13)$$

From (4), g_{mb}/C_b is set to be equal to $1/(R_bC_{pb})$ to make full use of the proposed CM. Solving (13) with this condition, implies that the minimum C_L that ensures a stable local loop is

$$C_L = \frac{(\sqrt{5}+1)g_{mL}(g_{mb}R_b - 1)C_b^2}{2g_{mb}(C_{p1}+C_d)}. \quad (14)$$

If C_d is not added, the minimum C_L is still very large. So the OpAmp is unable to handle small capacitive load without C_d.

Since ω_μ, g_{mb}/C_b, and $1/(R_bC_{pb})$ determine the high-frequency poles of the OpAmp's overall transfer function, a larger ω_μ suggests a larger PM. As C_L increases, ω_μ is reduced, as shown in Fig. 12. Although the local loop's PM improves, the OpAmp's PM degrades. This trend continues until the mid-band local loop gain becomes less than the unity, which is given by

$$\frac{g_{mL}(g_{mb}R_b - 1)C_b}{g_{o1}C_L} < 1. \quad (15)$$

Under this condition, the local loop fails to control the high-frequency behavior of the OpAmp. Therefore, the transfer function of the OpAmp is obtained by merely considering the open loop given below:

$$A_v(s) \approx \frac{g_{m1}g_{mL}\left(1+s\frac{(g_{mb}R_b+1)C_b}{2g_{mb}}\right)}{g_{o1}g_{oL}\left(1+s\frac{C_{p1}+C_d}{g_{o1}}\right)\left(1+s\frac{C_L}{g_{oL}}\right)}. \quad (16)$$

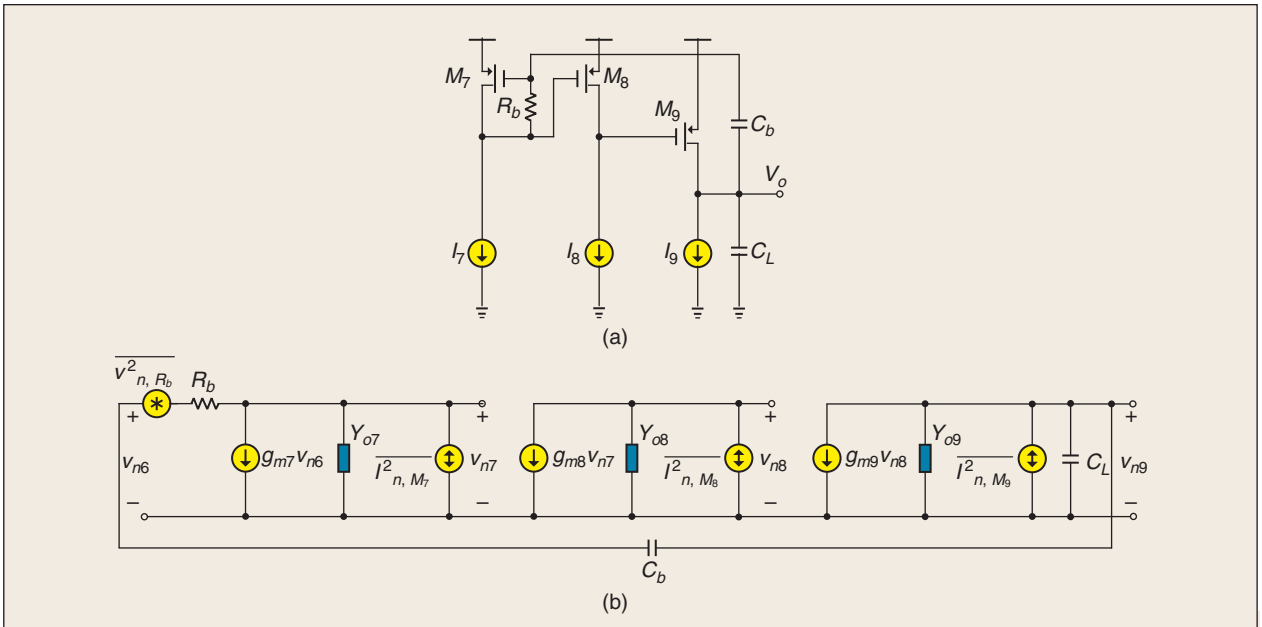

Figure 13. (a) Simplified schematic of the proposed OpAmp for noise analysis and (b) its small-signal equivalent circuit.

A LHP $\omega_{z1} = 2g_{mb}/[(g_{mb}R_b + 1)C_b]$ is generated in the OpAmp. The appearance of ω_{z1} is not due to the existence of the local feedback loop. Physically, the presence of such an LHP zero derives from the fact that one part of the signal at the output of g_{m1} stage is bypassed by the resistor R_b and this part of the signal is in-phase with the signal passing through the main path. From (16) and neglecting the impact of ω_{z1} because of its high location in frequency, the PM of the OpAmp is expressed as

$$\mathrm{PM} \approx \arctan\frac{\omega_{p1}}{A_{dc}\cdot\omega_{pd}} = \arctan\frac{g_{o1}^2 C_L}{g_{m1}g_{mL}(C_{p1}+C_d)}. \quad (17)$$

Investigating eq. (17), if C_L increases further, the position of the dominant pole g_{oL}/C_L is shifted to the left while the non-dominant pole $g_{o1}/(C_{p1}+C_d)$ remains unchanged. Thus, the PM of the OpAmp increases. For this case, if the proposed OpAmp is stable for the given value of C_L, it is also unconditionally stable for any larger C_L.

From the varying course of PM versus C_L in the above cases, a minimum PM of the OpAmp occurs at $|T_L(jw)| = 1$ which is equivalent to

$$C_L = \frac{g_{mL}(g_{mb}R_b - 1)C_b}{g_{o1}}, \quad (18)$$

Substituting (18) into (17) with the dominant pole ω_{pd} and ω_{p1} which changes to $g_{oL}/(2C_L)$, and $2g_{o1}/(C_{p1}+C_d)$, respectively, the minimum PM is

$$\mathrm{PM}_{min} \approx \arctan\frac{4g_{o1}(g_{mb}R_b - 1)C_b}{g_{m1}(C_{p1}+C_d)}. \quad (19)$$

The requirement in (19) indicates there are two possibilities to obtain a good PM_{min} for the OpAmp. One is to reduce the first stage gain of the OpAmp, while increasing OpAmp's offset and noise and lowering the overall gain, and leading to a limited reduction in g_{m1}/g_{o1}. The other is to enlarge the ratio $[(g_{mb}R_b - 1)C_b]/(C_{p1}+C_d)$ although with a limitation. As observed from Fig. 12, ω_μ is proportional to this ratio and ω_μ also increases with decreasing C_L. The increased ω_μ will approach the values of the high-frequency poles, and significantly degrading the PM of the local loop. Therefore, the design effort will imply trade-offs among the first stage gain, power, and the size of C_b and C_d.

B. Capacitor Size and Unity-Gain Frequency

It is worth it to mention that the proposed CM technique further decreases the size of physical capacitor by $(g_{mb}R_b - 1)$ when compared with the MCCB technique for single-value load capacitance. In other words, with the same size of C_b the proposed compensation scheme is capable of driving capacitive load that is larger than that of MCCB, by an order of magnitude, because $(g_{mb}R_b - 1)$ is easily sized to a magnitude of ten. To cover the range of smaller capacitive load, a small C_d would be necessary.

The UGF of the OpAmp is almost equal to GBW as given by $(g_{m1}/[(g_{mb}R_b - 1)C_b])$ for small C_L. As mentioned

before, there is an LHP zero ω_{z1} in the transfer function. To guarantee the stability of the overall loop, ω_{z1} must be located above the GBW, thus contributing to the OpAmp's PM, which is translated to the following condition,

$$\frac{g_{m1}}{g_{mb}} < \frac{2(g_{mb}R_b - 1)}{g_{mb}R_b + 1} \approx 2. \tag{20}$$

C. Design Considerations for the Class-AB Output Stage

A class-AB output stage [45] is employed to enhance the transient performance of the OpAmp. The role of C_{bat} is twofold. First, it can be exploited to increase the gain of the OpAmp because it is by means of C_{bat} that the transconductance of M_{10}, g_{m10}, takes effect. In order to increase the low-frequency gain, a larger C_{bat} is desired. Second, a larger C_{bat} is critical to ensure an accurate voltage transfer from the gate of M_9 to that of M_{10}. Hence, C_{bat} larger than $10C_{gs10}$ is selected.

The saturation voltage V_{dsat} of M_9 has to be the same as that of M_{10} so that M_9 and M_{10} have equal current boost capability during transients. Besides, a relatively low V_{dsat} can reduce the drastic change of voltage at the output of the first stage, decreasing or avoiding the conduction of parasitic diode in M_R, or diode-connected M_R itself.

D. Noise Analysis

Knowing the internal noise transfer functions of the OpAmp eases the device sizing. The simplified schematic of the proposed OpAmp and its small-signal equivalent circuit for the noise analysis are shown in Fig. 13(a) and (b), respectively. Y_{oi} represents the lumped admittance at the corresponding node. The noise generated by the tail current source M_{b6} is

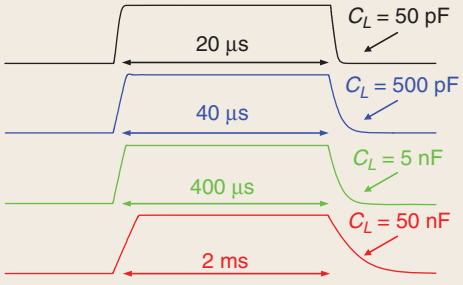

Figure 15. Unity-gain step responses of the OpAmp for different values of C_L under 500-mV input step.

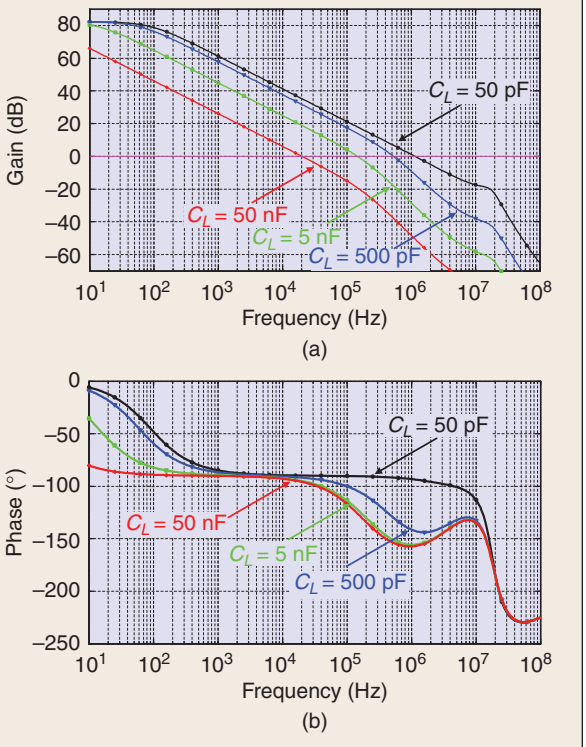

Figure 14. Proposed OpAmp AC responses with different C_L. (a) Magnitude. (b) Phase.

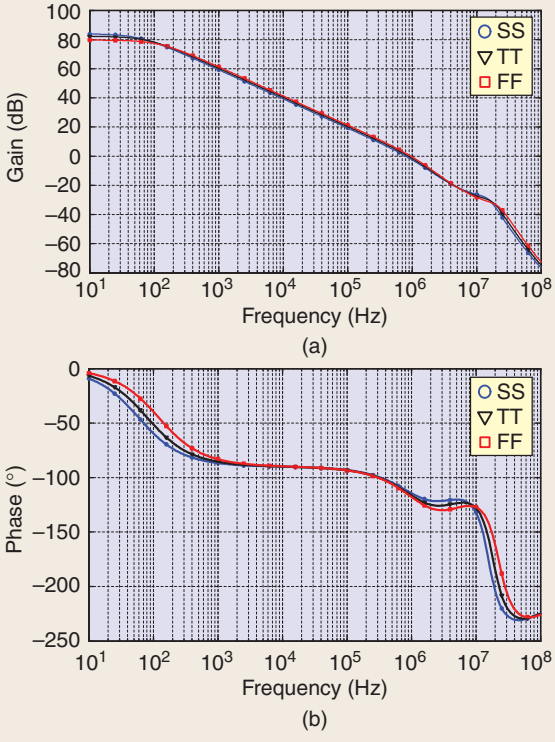

Figure 16. Proposed OpAmp AC responses with C_L = 150 pF under different process corners. (a) Magnitude. (b) Phase.

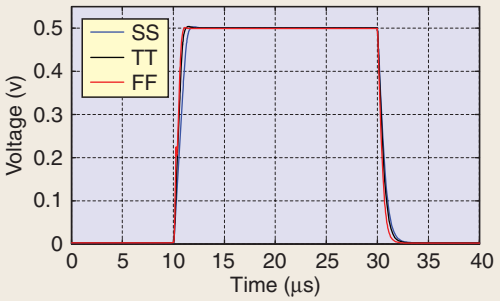

Figure 17. Unity-gain step responses of the OpAmp with C_L = 150 pF and 500-mV input step under different process corners.

Table 1.
Component sizes of the proposed OpAmp.

Device	Size	Device	Size
M_1/M_2	8 × (6 μm/1 μm)	M_{b5}	2 μm/1 μm
M_3/M_4	8 × (2 μm/1 μm)	M_{b6}	8 × (4 μm/2 μm)
M_5/M_6	6 × (2 μm/0.4 μm)	M_R	1 μm/1 μm
M_7/M_8	6 × (4 μm/0.8 μm)	C_b	0.8 pF
M_9	2 × (4 μm/0.8 μm)	R_b	85 kΩ
M_{10}	2 × (2 μm/1 μm)	C_{bat}	0.5 pF
$M_{b1}/M_{b2}/M_{b4}$	2 × (4 μm/2 μm)	C_d	~ 0.6 pF
M_{b3}	1 μm/8 μm		

negligible at the frequencies of interest. Also the noise contribution of cascode transistors M_5 and M_6 is less significant. Hence, the analysis mainly focuses on the noise contribution of R_b, M_7, M_8, and M_9 as the noise of transistors M_1, M_2, M_3, and M_4 can be easily referred to the input stage, using an equivalent input-referred voltage noise source. The input-referred noise transfer functions of the noise sources: R_b, M_7, M_8 and M_9, are respectively given by,

$$|A_{n,R_b}(s)|^2 = \left| \frac{g_{m8}}{g_{m1}} \cdot \frac{1 + s\dfrac{C_b}{g_{m7}}}{1 + s\dfrac{(g_{m7}R_b + 1)C_b}{g_{m7}}} \right|^2 \cdot |A_v(s)|^2 \qquad (21)$$

$$|A_{n,M_7}(s)|^2 = \left| \frac{g_{m8}}{g_{m1}} \cdot \frac{1 + sR_bC_b}{1 + s\dfrac{(g_{m7}R_b + 1)C_b}{g_{m7}}} \right|^2 \cdot |A_v(s)|^2 \qquad (22)$$

$$|A_{n,M_8}(s)|^2 = \left| \frac{g_{m8}}{g_{m1}} \cdot \frac{\left(1 + s\dfrac{C_b}{g_{m7}}\right)(1 + sR_bC_{pb})}{1 + s\dfrac{(g_{m7}R_b + 1)C_b}{g_{m7}}} \right|^2 \cdot |A_v(s)|^2 \qquad (23)$$

$$|A_{n,M_9}(s)|^2 = \left| \frac{g_{o8} + sC_{p8}}{g_{m1}} \cdot \frac{\left(1 + s\dfrac{C_b}{g_{m7}}\right)(1 + sR_bC_{pb})}{1 + s\dfrac{(g_{m7}R_b + 1)C_b}{g_{m7}}} \right|^2 \cdot |A_v(s)|^2 \qquad (24)$$

where $A_v(s)$ is the transfer function of the proposed amplifier. From eqs. (21)–(24), it can be observed that the noise due to R_b, M_7 and M_8 generates the major portion of the thermal noise within the GBW of the amplifier, while the noise contribution of M9 is suppressed by the gain of the first stage.

Table 2.
Typical Performance Summary of the Proposed OpAmp. The Results are Obtained with Cd = ~ 0.6 pF.

Technology	AMS 0.35-μm CMOS			
V_{DD} (V)	1.5			
Total Quiescent Current (μA)	31.5			
DC Gain (dB)	82			
Input-Referred Noise Voltage from 1 to 10 MHz (μV_{rms})	484.7			
Loading Capacitance (pF)	50	500	5000	50000
Unity-Gain Frequency (MHz)	1.15	0.53	0.146	0.02
PM (degree)	86°	51°	58°	85°
Gain Margin (dB)	−22	−44	−64	−84
SR+/SR−(V/μs)	0.73/0.73	0.2/0.17	0.021/0.012	0.002/0.0011
1% TS+/TS− (μs)	1/1.2	3.3/7.7	24.34/89.25	242/1000
FoM_S (MHz · pF/mA)	1825	8413	23175	31746
FoM_L (V/μs · pF/mA)	1159	2937	2619	2460

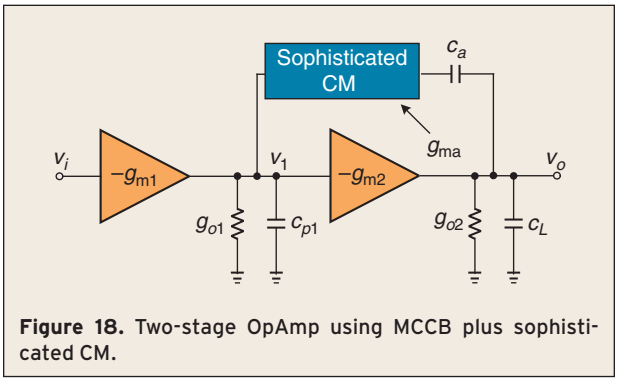

Figure 18. Two-stage OpAmp using MCCB plus sophisticated CM.

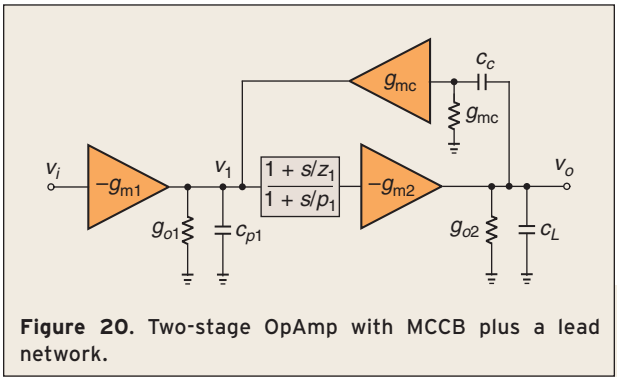

Figure 20. Two-stage OpAmp with MCCB plus a lead network.

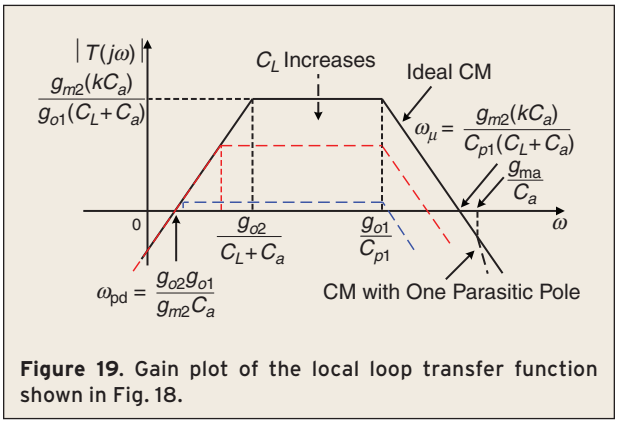

Figure 19. Gain plot of the local loop transfer function shown in Fig. 18.

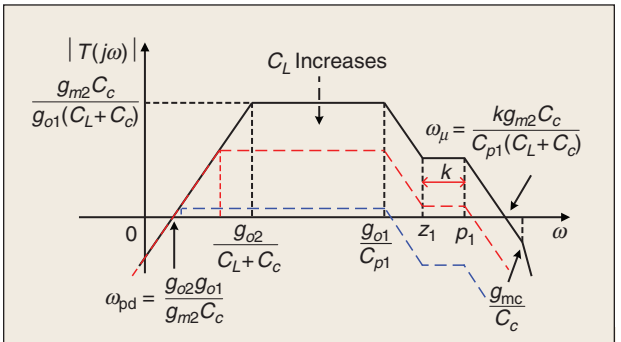

Figure 21. Gain plot of the local loop transfer function shown in Fig. 20.

E. Simulation Results

The overall performance of the OpAmp has been verified in 0.35-μm CMOS under a 1.5-V supply. To demonstrate the effectiveness of the proposed CM, the OpAmp has been tested under a wide range of large capacitive loads. Table 1 summarizes the component sizes of the OpAmp. With a biasing current set to 1.5 μA and all other drain currents shown in Fig. 11(a), the total current consumption is 31.5 μA. During the simulation, R_b, and C_b have been tuned to 85 kΩ, and 0.8 pF respectively, to achieve an effective Miller capacitance of 7.9 pF with $g_{mb} = 128\,\mu S$. The other parameters (g_{m1}, g_{m9} and g_{m10}) are 61 μS, 43 μS, and 45 μS, respectively. The value of C_{bat} is chosen to be 0.5 pF which is much larger than the total gate-capacitance of M_{10} (~13 fF). C_d is close to 0.6 pF to implement a highly stable OpAmp for a broad range of load capacitance ($\geq$50 pF). A small diode-connected PMOS transistor M_R with source and substrate terminal connected behaves like an extremely high resistor. Fig. 14 shows the frequency responses of the OpAmp with C_L = 50 pF, 500 pF, 5 nF, and 50 nF. The PM is larger than 50° for all cases. The corresponding transient responses are shown in Fig. 15 indicating that the proposed OpAmp is very stable without any oscillation and ringing when the input is stimulated by a 500-mV step. To validate the robustness of the OpAmp against process corners (slow-slow, typical-typical and fast-fast), a 150-pF load is adopted. It can be observed from the AC [Fig. 16] and step [Fig. 17] responses that the proposed OpAmp is also very stable with little performance variations.

A performance summary obtained with the variation of the capacitive load from 50 pF up to 50 nF is given in Table 2. For $C_L > 50$ nF, the OpAmp becomes more stable from the above analysis although the UGF is significantly reduced.

V. Potential CM and Other Frequency Techniques Extending Wide-Range Capacitive Driving Capability

Among the existing Miller compensation techniques, Miller compensation with current buffer (MCCB) features the highest potential to lead further improvement of two-stage OpAmp in driving a large or wide-range capacitive load. However, one drawback of this topology is that the gain of the first stage strongly relies on the size of the compensation capacitor C_m. CM techniques have been employed here to reduce the physical size of C_m. But, the proposed CM still possesses two high-frequency poles and thus further smaller load capacitance cannot be handled. If more sophisticated CMs without parasitic poles or with just one very high-frequency pole are proposed, a large-range capacitive-load stable OpAmp with

high power-and-area efficiency can be accomplished. Alternatively, if a zero-pole pair or lead network could be inserted in the forward path of the OpAmp, the UGF of the local feedback loop can be further improved. The extended bandwidth can be utilized to save the power of the 2nd stage and enhance its capacitive driving capability. The following sub-sections describe these two techniques and their associated challenges:

A. Sophisticated CM Without Parasitic Poles or With Only One High-Frequency Pole in the Local Loop

Fig. 18 describes a two-stage OpAmp using MCCB in conjunction with a sophisticated CM. In a sophisticated CM, if there is no parasitic pole, the two-stage OpAmp is able to handle any value of load capacitance with k-fold smaller C_a in comparison with the pure MCCB OpAmp, as shown in the gain plot Fig. 19. A parasitic pole associated with g_{ma} and C_a is induced by the sophisticated CM. When compared with the pure MCCB OpAmp, this pole is pushed to a high-frequency position due to the reduced value of C_a. This structure is superior to the previously proposed CM because that has an extra high-frequency pole. The extra pole is the prime cause for instability when the load capacitance is greatly decreased. For instance, even a 10° reduction in PM of the local loop leads to a great amount of peaking in the transfer function of the OpAmp [27] if the minimum PM of the local loop is 45°. When the load capacitor is small, the step response of the OpAmp will exhibit significant high-frequency ringing or oscillation as observed in [19]. Therefore, one of the future research trends in frequency compensation techniques would be related with the development of more sophisticated CMs extending OpAmp's driving capability to small capacitive loads.

B. Inserting a Lead Network in the Forward Path

A lead network can be utilized to further increase the bandwidth of the MCCB's control loop. If the local loop of the OpAmp is cascaded by a lead network, the UGF of the local loop will be boosted. However, the lead network cannot be in the feedback path since it will become a lag network in the overall transfer function when the local loop is closed. Thus, the lead work should be inserted in the forward path. The block diagram of the concept is illustrated in Fig. 20. The Bode plot of the local loop is given in Fig. 21, if the ratio of p_1/z_1 is k, the UGF of the local loop can be k-fold enlarged. The extended bandwidth is useful for driving a big capacitor while dissipating less power. Moreover, when a high-frequency lead network is located after the pole g_{mc}/C_c, the range of the capacitive load can be increased, providing that the poles induced by the lead network are located at sufficient high frequencies beyond g_{mc}/C_c. The realization (passive or active) of the lead network determines the efficiency of the technique in practice.

VI. Summary

Frequency compensation is essential for two-stage and multi-stage operational amplifiers (OpAmps). In this article, for the first time, state-of-the-art frequency compensation techniques for two-stage OpAmps to drive a wide-range capacitor load are revisited in detail. Their key features are analyzed and justified according to the corresponding area-and-power efficiency. With the knowledge of the exisitng techniques, a new embedded capacitor multiplier (CM) is introduced as a feasible alternative. The input stage of the OpAmp features an embedded CM minimizing the size of the physical compensation capacitors, improving the slew rate and inducing a useful LHP zero to enhance the circuit stability. No extra bias circuit and power are required by this embedded CM. A detailed mathematical analysis and circuit vertifications of all performance metrics provide insights in circuit dimensioning and confirm the feasibility of the OpAmp. This simple yet effective two-stage OpAmp architecture can be widely useful for different applications.

As it can be foreseen, frequency compensation techniques of two-stage and multi-stage OpAmps will continuously evolve by combining them with other techniques such as advanced current buffer, and more sophiscated CMs, in a trend to boost the driving capability over a large or wide-range capacitive load with minimum power and area.

Acknowledgments

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