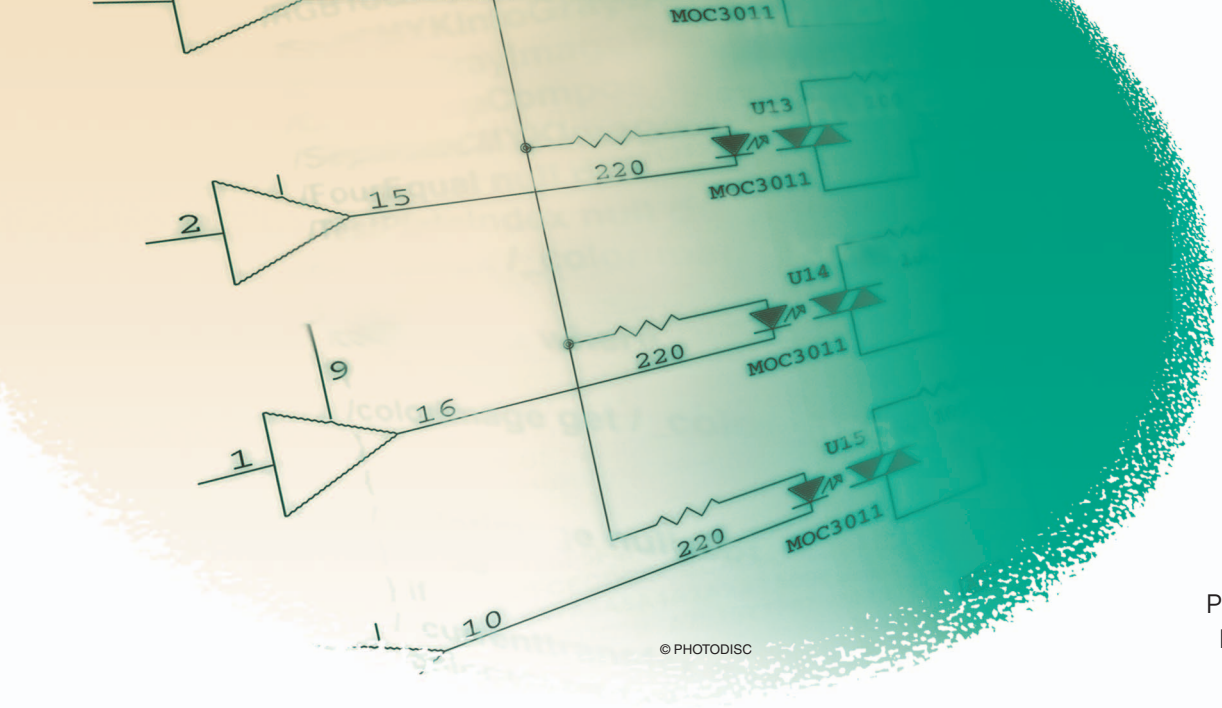

Pui-In Mak and
Rui P. Martins

High-/Mixed-Voltage RF and Analog CMOS Circuits Come of Age

Abstract

Instead of blindly tracking the rapid downsizing of supply voltage (V_{DD}) in technology scaling, high-/mixed-voltage radio-frequency (RF) and analog CMOS circuits have emerged as a prospective alternative comes of age. An elevated V_{DD}, or a hybrid use of I/O and core V_{DD}'s, in conjunction with thin- and thick-oxide MOS transistors open up many possibilities in defining circuit topologies, while maintaining the speed and area benefits of advanced processes. Circuit reliability can be guaranteed through advanced circuit techniques. This paper aims to provide a glimpse of the basic concept, system design considerations and circuit examples. A wide variety of RF and analog CMOS circuits designed based on such techniques are examined and new topologies are proposed. Those circuit topologies comprise the RF power amplifier, the low-noise amplifier, the mixer, operational-amplifier-based analog circuits, the sample-and-hold amplifier and, finally, the line driver. Reliability considerations such as oxide breakdown, hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and bias temperature instability (BTI) will be discussed, and their implications in different types of circuits will be justified. The outlined principles are extendable to other RF and analog circuits, motivating the adoption of new voltage-conscious topologies in ultra-scaled CMOS processes.

I. Introduction

Rapid downscaling of CMOS has led to more compact and faster radio frequency (RF) and analog circuits but with deteriorated linearity and accuracy due to the associated low-voltage constraints. The value of the supply voltage (V_{DD}) predominantly defines the number of transistors that can be placed in cascode for an amplifier. Entered into the sub-1V nanoscale regime, the downsizing of threshold voltage (V_T) is decelerated due to transistor variability, matching and leakage issues. Insufficient voltage headroom makes cascoding of transistors very inefficient. Cascading of transistors, on the other hand, demand more power and achieves lower operating speed. Innovative techniques befitting sub-1V nanoscale processes must be investigated in order to keep driving up circuit performances along with technology advancements.

In this article, high-/mixed-voltage CMOS circuits are presented as the technology comes of age. *The research goal is to enlarge the design headroom through the elevation of V_{DD} in ultra-scaled CMOS processes and the hybrid use of thin- and thick-oxide transistors.* In advanced processes, thin-oxide transistors are for core design that have a voltage limit the same as the standard supply $V_{DD,c}$. Thick-oxide transistors are for I/O

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Bringing thick-oxide transistors, and their associated $V_{DD,IO}$, into the RF and analog circuit design portfolio appears to be a handy option to increase the design flexibility.

design that can work at a higher supply voltage $V_{DD,IO}$. When design-for-reliability (i.e., no overstress on any device) is included in the design flow, an elevated V_{DD} outpacing the technology roadmap can reliably enlarge the voltage headroom ($V_{DD} - V_T$) as depicted in Fig. 1.

II. System Considerations

A general perception of mixed-voltage wireless system-on-chip (SoC) for portable applications is depicted in Fig. 2. Thin-oxide transistors powered by $V_{DD,c}$ exhibit the simplest structure to maximize the speed-to-power efficiency of digital functions such as the digital signal processor. However, RF and analog circuits such as the RF power amplifier and the baseband operational amplifier are not that efficient to work under the same $V_{DD,c}$, which in the latest technologies, such as the 65 and 40-nm CMOS, has values in the order of 1 to 0.9 V [1], respectively. Such $V_{DD,c}$ leads to small voltage headroom burdening the performance optimization, especially in multistandard wireless systems that demand high-linearity low-noise wideband RF circuits [2]. Consequently, the exploration of a voltage islanding concept in a power management unit would become essential for distribution of the supply voltages to different functions appropriately.

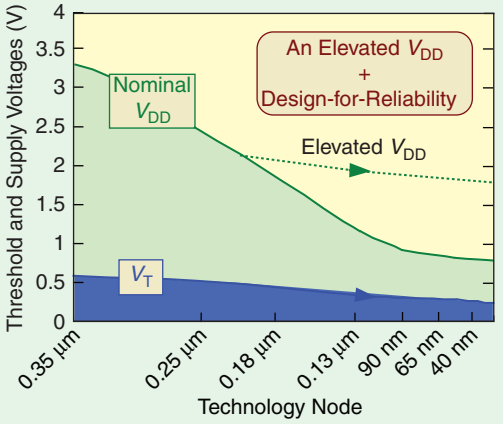

Figure 1. Voltage headroom increment through an elevated V_{DD}.

On the other hand, since many peripherals do not scale synchronously with the silicon technologies, thick-oxide transistors are still kept available in advanced processes to facilitate I/O communications. Thus, bringing thick-oxide transistors, and their associated $V_{DD,IO}$, into the RF and analog circuit design portfolio appears to be a handy option to increase the design flexibility. Thick-oxide transistors can be considered as devices from previous technology nodes: 0.25 and 0.18 μm. Their reliable operating voltages are 2.5 and 1.8 V, respectively. Both are much more comfortable values for RF and analog circuit design and can be easily generated by a 3.6/3.7-V Li-ion battery. Obviously, circuits built with purely thick-oxide transistors are not preferred as they cannot profit from the speed and area benefits of advanced processes. A hybrid use of thin- and thick-oxide transistors, $V_{DD,c}$ and $V_{DD,IO}$, emerges then as a new art in electronics that should be adopted with a sensible balance. In the latter sections, before we describe the high-/mixed-voltage-enabled circuits for wide types of RF and analog functions, the key device reliability concerns are discussed first.

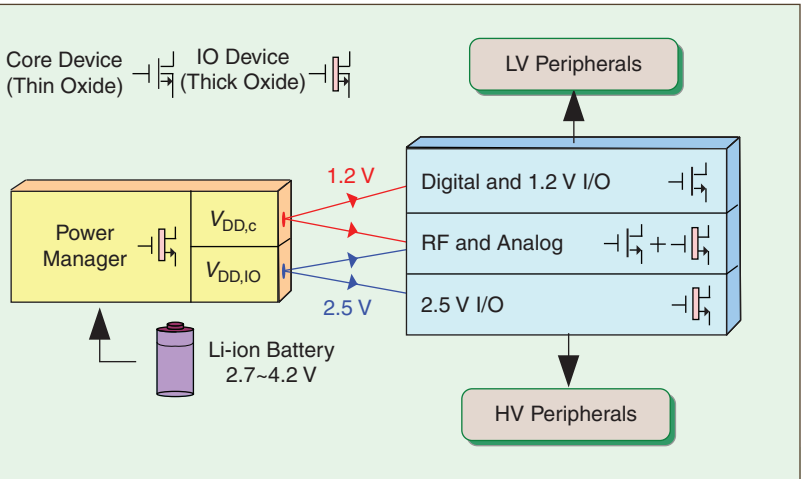

Figure 2. Increase RF and analog circuit design flexibility with add-on I/O supply voltage and thick-oxide transistor.

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Punchthrough is a critical concern in high-power circuits such as the power amplifier (PA), but it can be avoided for low-power low-swing RF circuits such as the low-noise amplifier (LNA).

III. Device Reliability in Ultra-Scaled Process

The technology Design Rule Manual provides the key device reliability concerns including the absolute maximum rating (AMR), hot carrier injection (HCI), electrostatic discharge (ESD), time dependent dielectric breakdown (TDDB), bias temperature instability (BTI) and punchthrough effect. Complying with them in the design indeed translates the term "design for reliability" into "voltage-conscious design", highly simplifying the design and verification methodologies [3]. Furthermore, in the topology formation phase, their implications to the circuits can be easily justified.

A. AMR

The AMR corresponds to the maximum voltage applied to a minimum-gate-length device with no unrecoverable hard failure. AMR is concerned mainly with the gate-oxide breakdown voltage as it is 3 to 4 times smaller than the junction breakdown voltage [3]. A device biased close to the AMR limit may also lead to a deviation in device parameters, degrading the long-term reliability. The tolerable AMR is continuously reducing with the technologies (e.g., 1.6 V in 90-nm CMOS), complicating the design of ESD protection in high-frequency pins.

B. HCI Lifetime

Degradation of MOS device characteristics occurs as a result of exposure to a high V_{DS} with a large drain current. Examples of degradation are a shift of V_T and a shorter gate-oxide breakdown lifetime. HCI normally happens in high-power circuits such as the power amplifier, where the worst HCI bias conditions: $V_{DS} \geqq V_{GS} \geqq V_T$ and $V_{DS} \geqq V_{DD}/2$ are concurrently satisfied. HCI degradation can be reduced by lowering the drain current or increasing the device channel length (L).

C. TDDB

TDDB is the wear-out of insulating properties of silicon dioxide in the CMOS gate, leading to the formation of a conducting path through the oxide to the substrate. In order to protect the circuit against TDDB the catastrophic destruction of gate oxides induced by the maximum DC gate oxide voltage at different temperatures must be considered. According to the maximum DC gate oxide voltages of 90- and 65-nm CMOS given in Table 1, NMOS has a higher voltage standing capability than PMOS for all cases to prevent TDDB. Thus, NMOS is preferable when considering TDDB in circuit design.

D. NBTI

BTI degradation happens under steady-state conditions. It is design dependent in analog and RF circuits and primarily only PMOS devices are subjected to BTI stress, namely negative BTI (NBTI). In a V_{DD}-upscaled design, analyzing NBTI involves detecting, in all modes of operation (DC and small signal), which PMOS device is exposed to a peak or rms voltage value exceeding the standard V_{DD}, which is around 1 V in 90 and 65-nm CMOS. Thus, NMOS is also preferred when implementing analog switches.

E. Punchthrough

Transistor gate length should be increased wherever possible to prevent the drain-source depletion regions from punchthrough. In 90-nm CMOS, for a transistor having an aspect ratio (W/L) of 10/0.1, a strong increment of drain current due to punchthrough effect starts at a value of $|V_{DS}|$ around 2.3 V. Although the punchthrough effect is not intrinsically destructive it can accelerate, in the long term, the gate oxide breakdown because of the induction of hot carriers. Punchthrough is a critical concern in high-power circuits such as the power amplifier (PA), but it can be avoided for low-power low-swing RF circuits such as the low-noise amplifier (LNA).

IV. Extend the Voltage Capability of Thin- and Thick-Oxide Transistors

With respect to the above-mentioned reliability concerns, individual thin (thick)-oxide transistors can withstand maximally just one $V_{DD,c}$ ($V_{DD,IO}$) voltage difference for any of the two terminals. In order to extend their voltage capability, stacking of devices can be applied. The concept is illustrated in Fig. 3. In steady state, the possible structures can be a stack of two (or

Table 1.
Maximum DC gate oxide voltage to prevent TDDB.

90 nm CMOS			65 nm CMOS		
	45°C	150°C		45°C	150°C
GP NMOS	1.43 V	1.28 V	GP NMOS	1.35 V	1.23 V
GP PMOS	1.29 V	1.17 V	GP PMOS	1.23 V	1.11 V

One basic request of this technique is that the bulk should be tied to the source terminal to avoid overstress between them, implying the need of a triple-well process for NMOS to have an isolated bulk.

more) thin-oxide transistors, thick-oxide transistors, or a hybrid use of both. Generally, the voltage capability across the drain and source terminals can be multiplied by the number of stacked transistors. One basic request of this technique is that the bulk should be tied to the source terminal to avoid overstress between them, implying the need of a triple-well process for NMOS to have an isolated bulk.

Among the three structures shown in Fig. 3 only pure stack of thin-oxide transistors and a hybrid stack of thin- and thick-oxide transistors are relevant to balance the speed and voltage capability. Pure stack of thick-oxide transistors cannot take advantage of the area and speed features of advanced technologies. In the hybrid case the thin-oxide transistor can serve as the amplification device for minimization of the loading effect to the previous stage. The thick-oxide transistor serves as the cascode device thus increasing the voltage capability. High-/mixed-voltage RF and analog circuits are generally based on these two stacking structures.

In addition to steady-state overstress, transient-state overstress should not be allowed too. Depending on the nature of the signal processing, large-signal circuits (e.g., line driver) requires checking the trajectory of all nodes. Alternative solutions are to employ voltage-biased and self-biased circuit topologies; both of them have the benefit that the internal node voltages can be easily controlled during power up/-down transients. Examples of the techniques will be discussed in the next section.

V. High-/Mixed-Voltage RF and Analog Circuits

A. Power Amplifier and Wideband Balun-LNA (High-V_{DD} 1 Mixed-Transistor)

V_{DD}-upscaling circuits have appeared in the literature for many years. The most common application is on the PA. As shown in Fig. 4(a) a hybrid use of thin- and thick-oxide devices in cascode permits high speed operation and the use of an elevated V_{DD} (3.3 V) to maximize the possible output power in 0.13-μm CMOS [4].

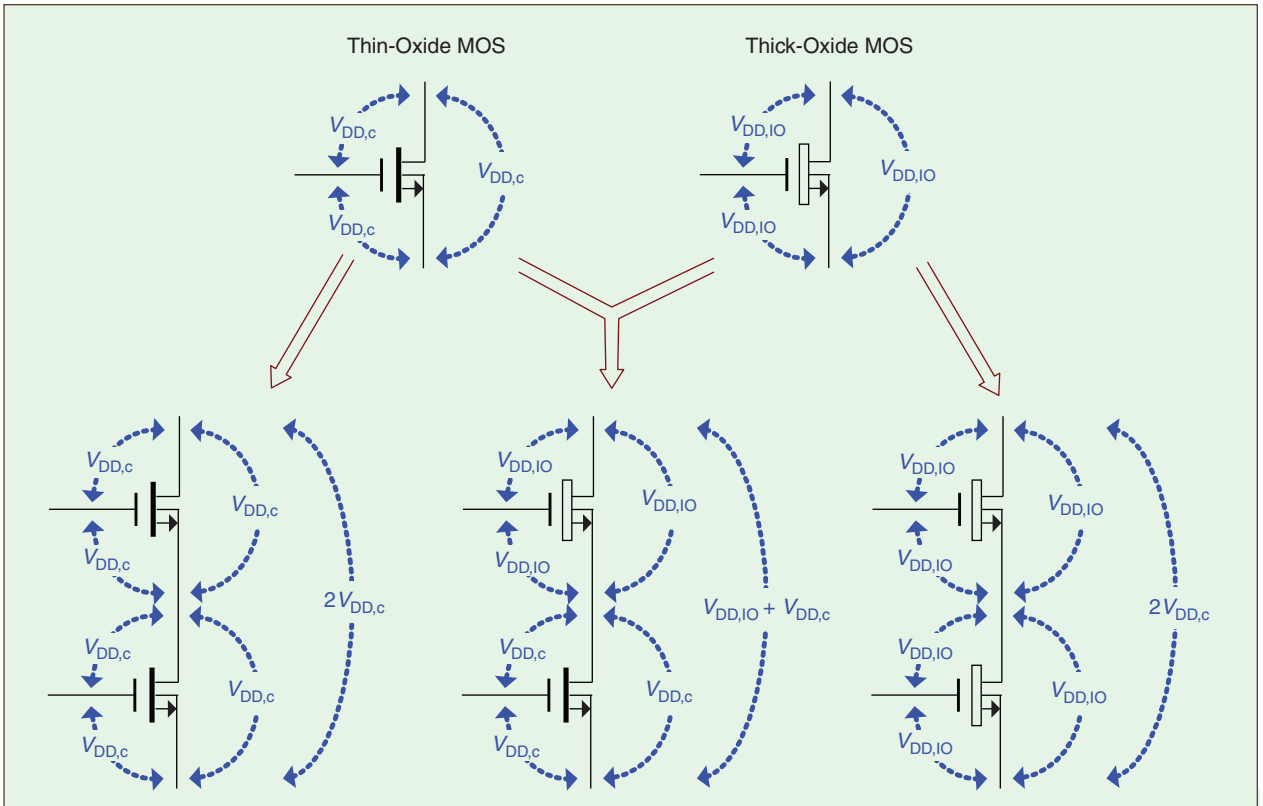

Figure 3. Extending the voltage capability of thin-and thick-oxide transistor through stacking.

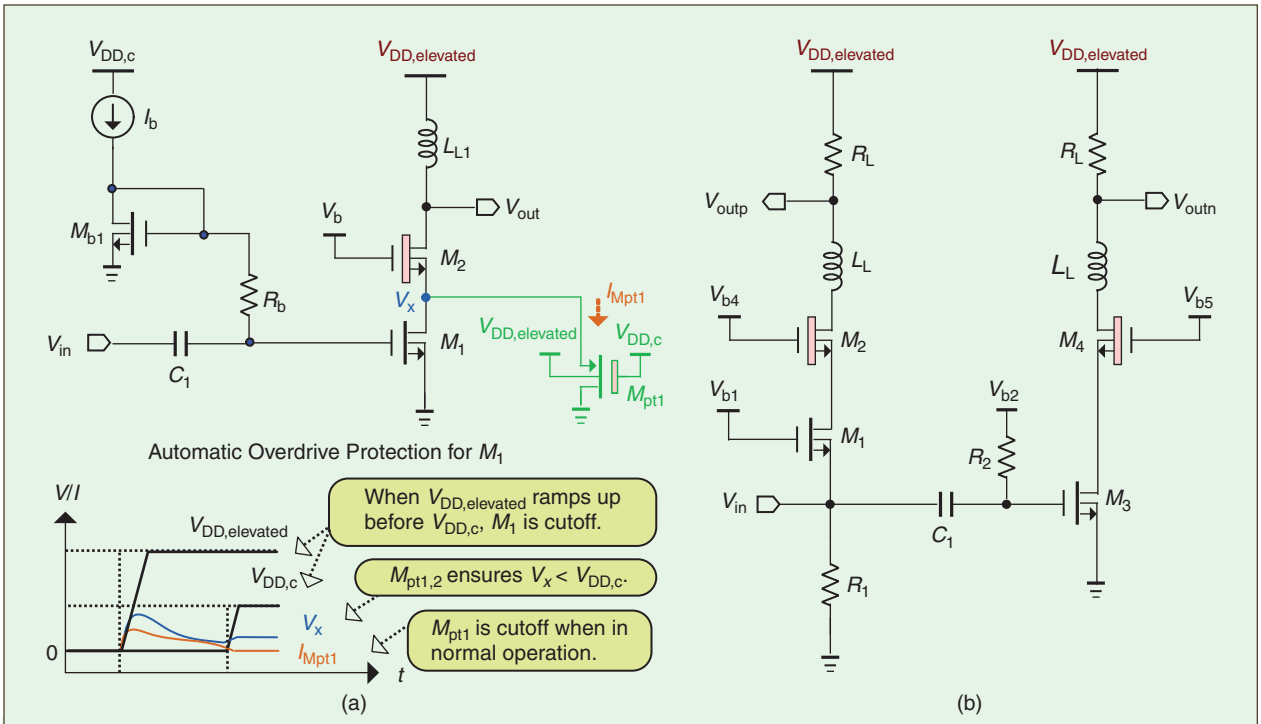

Figure 4. RF circuits using an elevated V_{DD}. (a) Power amplifier with automatic protection of M_1 from being overstress. (b) Wideband balun LNA.

This topology successfully prevents steady-state overstress. On the other hand, in order to protect M_1 from overstress automatically during the power-up/down transients, we propose to add a thick-oxide device M_{pt1} at V_x node. Its size is not critical as it is to ensure $V_x <$ $V_{DD,c}$ when $V_{DD,elevated}$ is activated first and can be turned off when $V_{DD,c}$ has caught up automatically.

Mixed-transistor circuit topologies also found applications in small-signal linearity-demanding RF circuits [5]–[7]. A 90-nm CMOS ultra-wideband balun low-noise amplifier (LNA) [5] based on an elevated V_{DD} (2.5 V) increases the output dynamic range while allowing more voltage drop at the resistive load R_L [Fig. 4(b)], achieving both high gain and high linearity but a smaller output bandwidth due to an increased R_L. A gain-peaking inductor L_L can be exploited to extend the output bandwidth. M_{pt1} in Fig. 4(a) can also be applied to this topology to protect M_1 and M_3.

B. ESD-Protected LNA (Mixed-V_{DD}+ Thin-Oxide Transistor)

Figure 5 depicts the simplified schematic of a PMOS-based, open-source-input ESD-protected ultra-wideband (UWB) LNA for full-band mobile TV [8]. Reverse-biased P^+-diffusion diode D_P, and N^+-diffusion diode D_N, are adopted for pin-to-rail ESD clamp. The aim of choosing a PMOS-based input structure is to take advantage

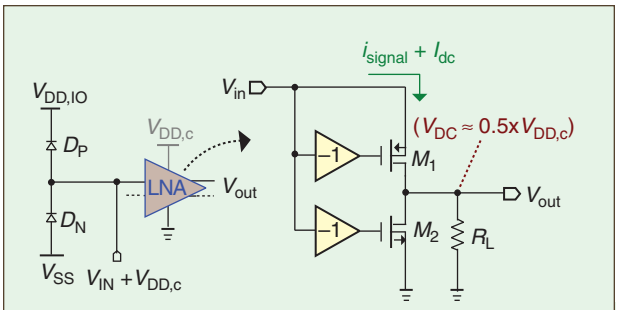

Figure 5. Mixed-voltage ESD-protected LNA (simplified).

of the presence of $V_{DD,IO}$ and comparison features with a NMOS-based structure are described next.

In case NMOS is selected as the input device together with an input common-mode voltage $V_{CM,IN}$ set to 0.6 V with respect to a 1.2 V $V_{DD,c}$ in a 90-nm CMOS process [Fig. 6(a)], the input swing is optimum as it is midway the rail-clamp supply that is the $V_{DD,c}$. Regrettably, $V_{CM,IN}$ = 0.6 V will offset the output common-mode level by the same amount, resulting in a limited output swing. Though $V_{CM,IN}$ = 0 V can resolve such an output swing limitation [Fig. 6(b)], D_N at such a $V_{CM,IN}$ is at a higher risk of forward bias, unavoidably sacrificing part of the input swing.

Conventionally, the above tradeoff cannot be resolved by using PMOS devices as shown in Fig. 7(a), but the presence of $V_{DD,I/O}$ enables the use of a higher ESD

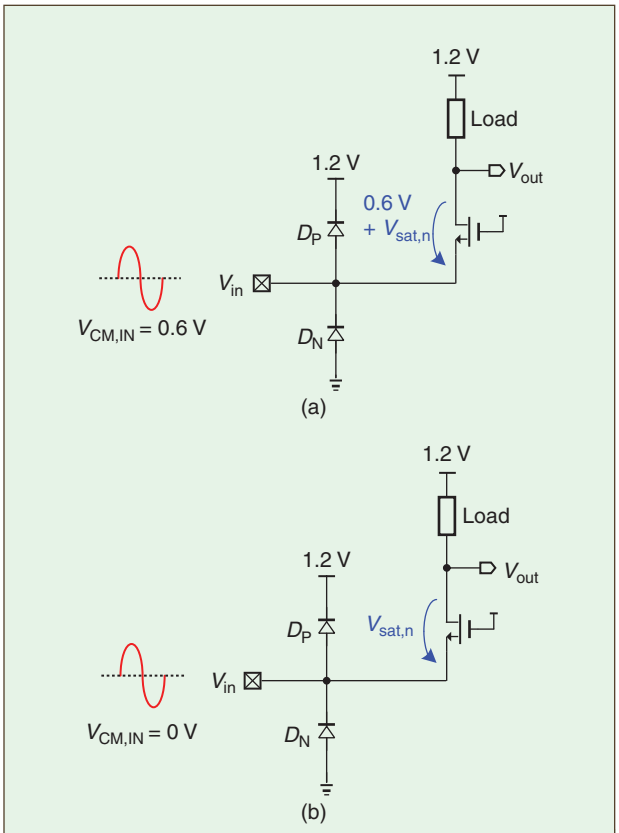

Figure 6. Diode clamps with a NMOS-input structure: (a) $V_{CM,IN}$ = 0.6 V and (b) $V_{CM,IN}$ = 0 V.

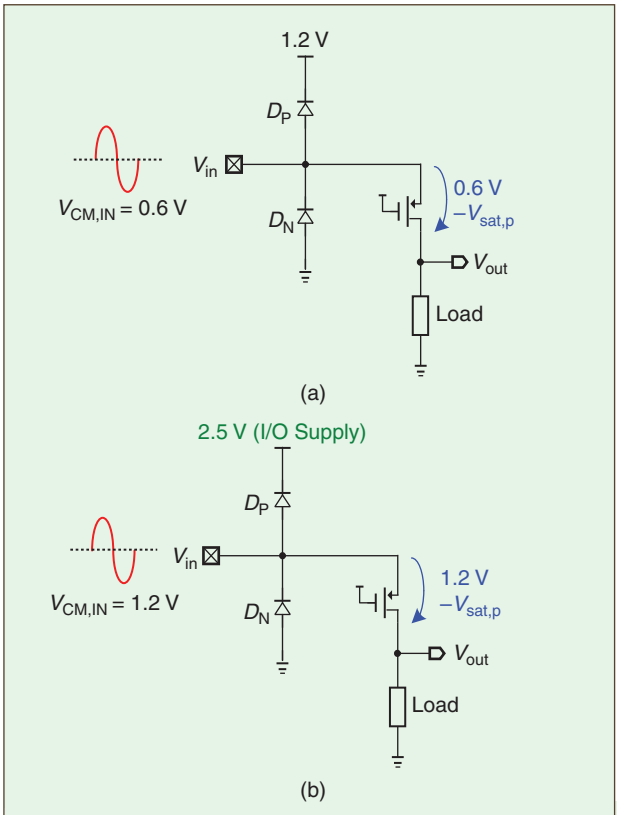

Figure 7. Diode clamps with a PMOS-input structure: (a) $V_{CM,IN}$ = 0.6 V and (b) $V_{CM,IN}$ = $V_{DD,C}$ = 1.2 V but the clamping voltage is the $V_{DD,I/O}$ = 2.5 V.

protection rail. For a $V_{DD,I/O}$ of 2.5 V, the I/O swings can be concurrently maximized as shown in Fig. 7(b). The improvement is illustrated by plotting the diode-clamp I/O transfer curves and their 1st derivatives at typical and extreme temperatures [Fig. 8]. With $V_{CM,IN}$ = V_{DD} = 1.2 V, the linear input [v_{sig}(t)], even at the highest temperature, has a swing of roughly 3 V_{pp} in the PMOS case, while it is just roughly 0.8 V_{pp} in the NMOS case with $V_{CM,IN}$ = GND (0 V). Besides, considering the ESD robustness, $V_{CM,IN}$ = $V_{DD,c}$ balances the discharge capability of ± zapping events.

C. Cascode-Inverter LNA (High-V_{DD}+ Thin-Oxide Transistor)

HV-enabling circuit techniques are normally based on stacked transistors to lower the voltage stress on each device. Consequently, only one transistor can serve as the amplification device. A 90-nm CMOS cascode-inverter LNA was proposed [9]–[10] to enhance the gain-to-power efficiency and boost up the voltage withstand capability. The formation of the circuit is illustrated by introducing a V_{DD} partitioning concept. In order to reliably bias the thin-oxide transistors under an elevated supply it is design-convenient to equally divide the supply into four regions,

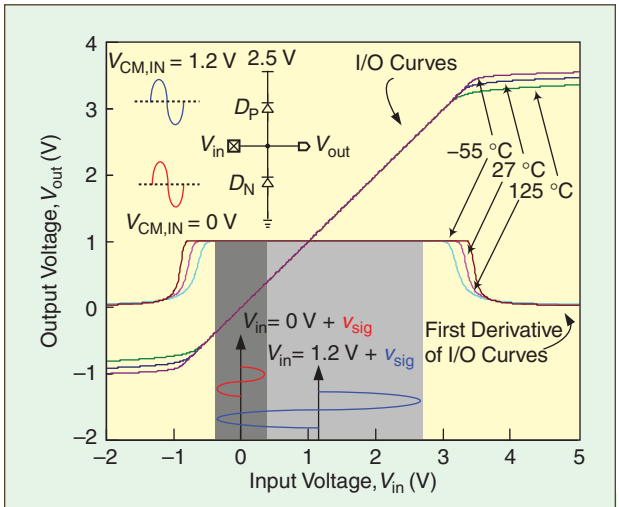

Figure 8. Diode-clamp I/O transfer curves and their 1st derivatives at different temperatures, showing the linear input swing versus the selected $V_{CM,IN}$.

as shown in Fig. 9. On the left, a 1×V_{DD} inverter-type amplifier (IA_1 to IA_3) can be connected in three different ways without affecting the performance and reliability. Such an amplifier is self-biased by a feedback resistor. It can be observed that the inter-rail voltage levels (0.5×V_{DD}, 1×V_{DD}

By doubling the supply to $2\times V_{DD}$ as shown in Fig. 11(b), the overdrive voltage of the MOS switches is maximized to the technology allowable limit.

and $1.5\times V_{DD}$) call for additional circuitry supply rails. This overhead, however, can be avoided by exploiting a cascode of two identical inverter amplifiers (IA_4 and IA_5). The intermediate point is still the RF input node, self-biased to a value close to $1\times V_{DD}$ because of voltage division. Due to a matched I/O DC level, the voltage gain can be enhanced further by cascading the cascoded inverter amplifiers (IA_6 to IA_9), without needing any ac-couplings.

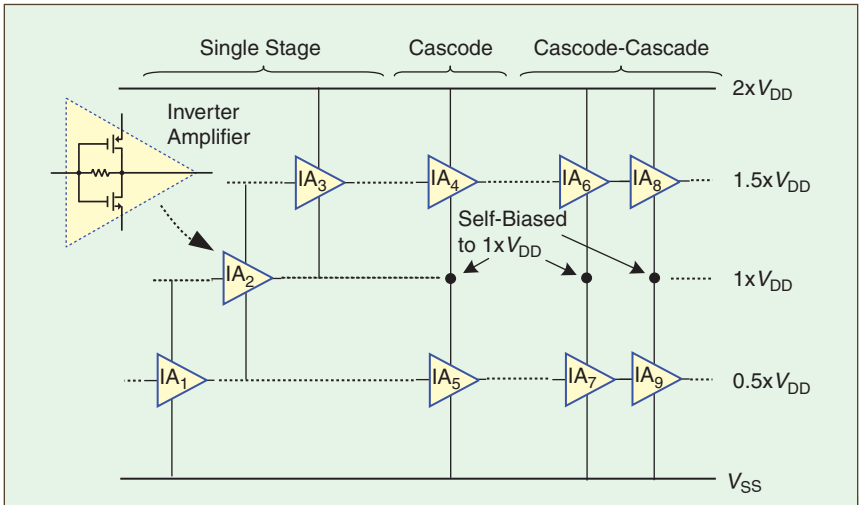

Figure 9. Three $2\times V_{DD}$ partitioning schemes for the LNA.

Figure 10(a) shows the schematic of a cascode-inverter LNA that is enabled to work underneath a $2\times V_{DD}$ supply with no reliability issue. The common source node of M_2 and M_3 provides an input impedance match. Assuming a differential input is available, the overall transconductance can be boosted by applying the inverting input to the gate of M_1–M_4. Every transistor shares a voltage drop of $0.5\times V_{DD}$, ensuring reliability in both steady and transient states [Fig. 10(b)] without needing additional biasing circuits. The dual outputs can be passively summed by a capacitor C_{sum} to halve the output impedance, or actively summed in current mode by using transistors to further enhance the gain.

Self-based inverter-based circuits are sensitive to process, voltage and temperature (PVT) variation. The back-gate control scheme highlighted in [11] is an effective solution for this problem. It keeps the supply current constant and reduces the sensitivity to supply ripple by returning the correcting signals to $V_{p,bulk}$ and $V_{n,bulk}$. A triple-well process is required to isolate the bulk of NMOS from the substrate.

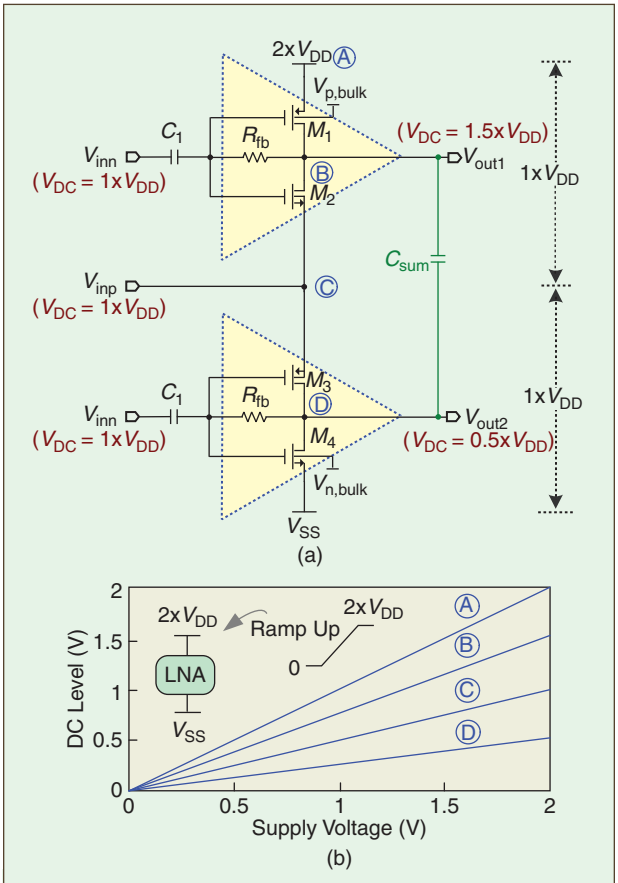

Figure 10. (a) A $2\times V_{DD}$ cascode-inverter LNA and (b) its internal node voltage varation when V_{DD} ramps up.

D. Passive Mixers (High-V_{DD}+ Thin-Oxide Transistor)

A passive current-mode downconversion mixer can be implemented with a resistor R_{ff} in-series with a MOS switch, and terminated with a virtual ground through the use of an operational amplifier (OpAmp). The OpAmp provides linear I-V conversion and first-order lowpass filtering at the output. In order to achieve a rail-to-rail output swing the output dc-level should be at half of the supply. For a generic $1\times V_{DD}$ design as shown in Fig. 11(a), the clocked MOS switch can only have a maximum overdrive voltage of $0.5\ V_{DD}$. However,

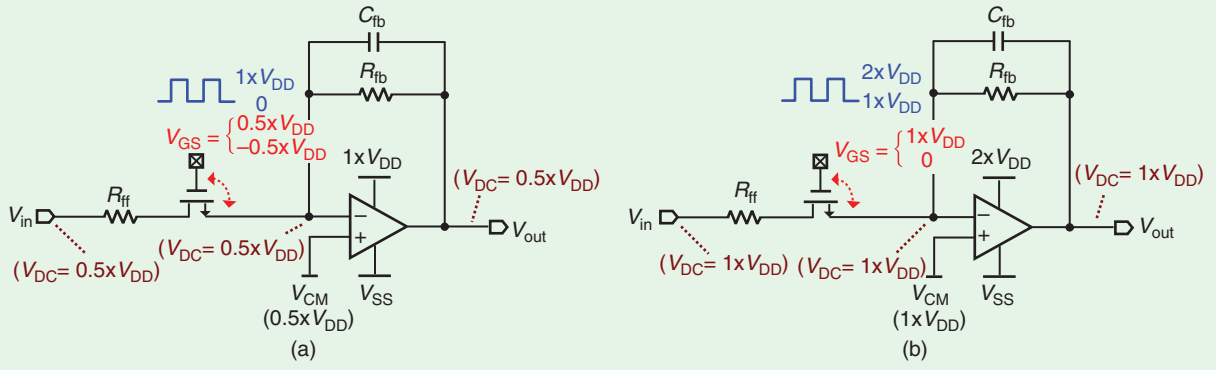

Figure 11. Downconversion passive mixers: (a) $1\times V_{DD}$ design. (b) $2\times V_{DD}$ design.

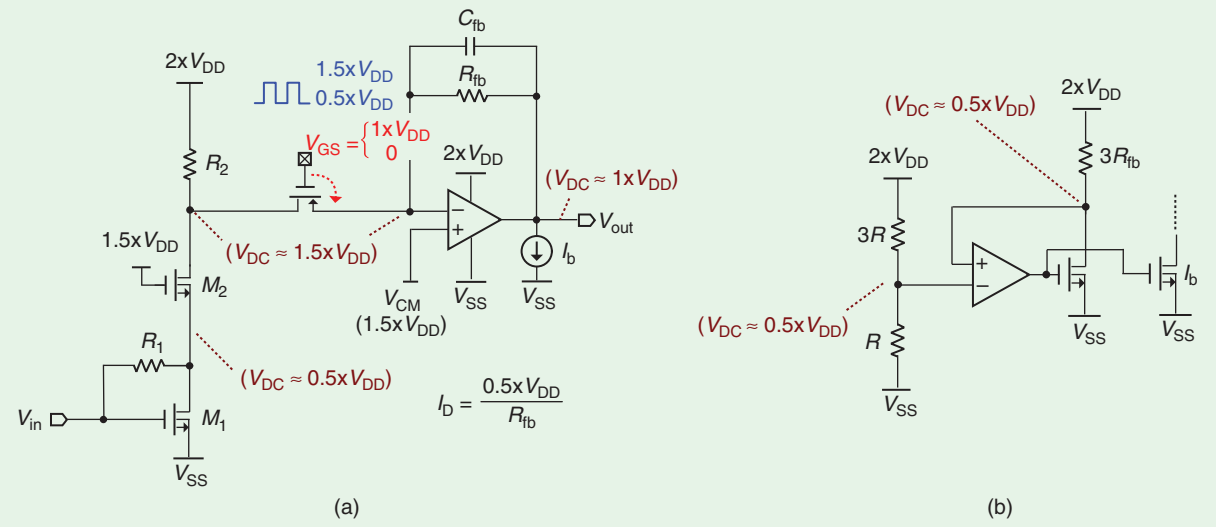

Figure 12. (a) $2\times V_{DD}$ passive mixer with mixer driver and its (b) Ib generation circuit.

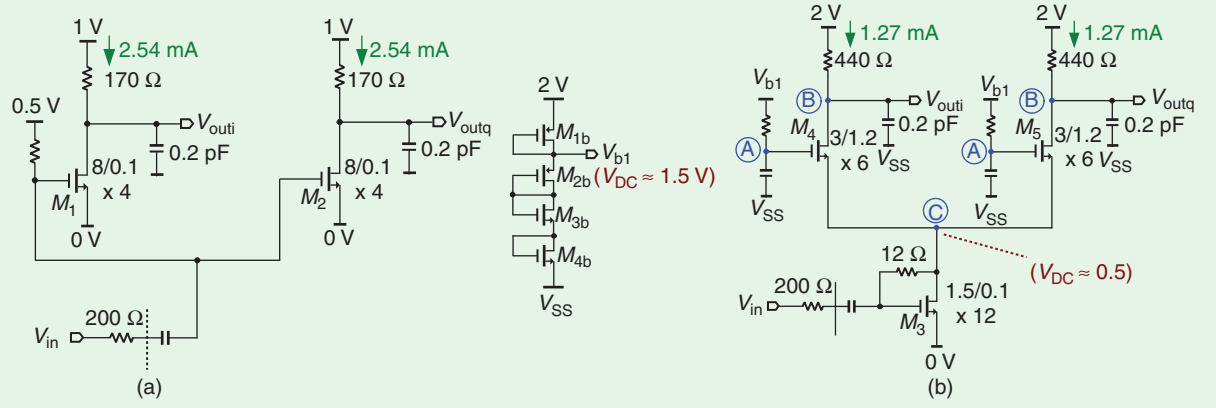

Figure 13. The reference schematics of two types of I/Q mixer drivers: (a) 1-V common-source amplifier and (b) 2-V cascode amplifier.

Given the same voltage gain requirement, power budget, source and load impedances, the first advantage of the $2\times V_{DD}$ design is that it exhibits 2.8-dB higher IIP3 than the $1\times V_{DD}$ one.

by doubling the supply to $2\times V_{DD}$ as shown in Fig. 11(b), the overdrive voltage of the MOS switches is maximized to the technology allowable limit, i.e., $1\times V_{DD}$. This act significantly reduces the size of the MOS switch and its induced nonlinearity.

Another type of $2\times V_{DD}$ passive mixer with a mixer driver is shown in Fig. 12(a). A $2\times V_{DD}$ 90-nm CMOS cascode amplifier serves as the mixer driver improving the linearity and reverse isolation [10] but the output dc-level is up-shifted to $1.5\times V_{DD}$. Under a $1.5\times V_{DD}$ dc-level PMOS is preferred as the mixing MOS to maximize the overdrive voltage. The unmatched input and output dc-levels of the OpAmp require an extra bias current I_b to sink out the excess dc-current in the feedback loop. Since I_b depends on the absolutely value of R_{fb}, a resistance-tracking bias circuit can be utilized for this purpose. As shown in Fig. 12(b), an error amplifier together with a $3R_{fb}$ and a current mirror generates the required value of $I_b = 0.5\times V_{DD}/R_{fb}$. It should be noted that no device is under overstress.

It is also of interest to compare the performances between 1-V and 2-V I/Q 90-nm CMOS mixer drivers. Figures 13(a) and (b) illustrate the schematics of two types of I/Q mixer drivers with the respective component parameters shown. The former is based on typical $1\times V_{DD}$ common-source amplifiers whereas the latter is based on $2\times V_{DD}$ cascode amplifiers with a shared input device (M_3) between I and Q channel to minimize the input capacitance. M_4 and M_5 are voltage-biased using a MOS-based divider as shown on the left. Figure 14 shows the simulated internal node voltages of the I/Q mixer drivers [markers correspond to Fig. 13(b)] when the $2\times V_{DD}$ ramps up from 0 to 2 V. The potential differences of all internal nodes are within the reliable limits given by the Design Rule Manual.

A performance summary of Figures 13(a) and (b) is presented in Table 2. Given the same voltage gain requirement, power budget, source and load impedances, the first advantage of the $2\times V_{DD}$ design is that it exhibits 2.8-dB higher IIP3 than the $1\times V_{DD}$ one. It can be observed that although M_1–M_3 can be biased to have the same V_{GS} close to 0.5 V, only M_3 can have a $V_{DS} = V_{GS}$ while maintaining an output swing of around 0.8 V_{pp}, given that $V_T =$ 0.3 V and V_{GS} of M_4 and M_5 is 1 V. M_4 and M_5 can be sized to have a long channel length in order to minimize the nonlinearity of its output resistance. However, for the $1\times V_{DD}$ design, an output swing of 0.8 V_{pp} implies a minimum V_{DS} of 0.2 V on M_1 and M_2, resulting in a deteriorated linearity because of strong channel-length modulation.

Table 2.
Simulated performances of 1-V and 2-V I/Q mixer drivers.

Parameters	1 V Mixer Driver	2 V Mixer Driver
Technology	90 nm CMOS	
Power consumption	2.54 mW	
Voltage gain	8 dB	
Source impedance	200 V	
Load	0.2 pF	
IIP3 (2-tone test at 500 & 505 MHz)	+2.7 dBm	+5.5 dBm
Reverse isolation (V_{in}/V_{outi})	31 dB	76.3 dB
I/Q isolation (V_{outq}/V_{outi})	39 dB	38.4 dB
Output -3-dB bandwidth	5.37 GHz	1.58 GHz
Output noise voltage (at 500 MHz)	5.29 nV/sqrtHz	6.25 nV/sqrtHz

The second advantage of the $2\times V_{DD}$ design is on the reverse isolation. Because of the presence of the cascode transistors M_4 and M_5, the $2\times V_{DD}$ design shows 45.3-dB better reverse isolation than the $1\times V_{DD}$ one.

The main drawback of the $2\times V_{DD}$ design is on the output bandwidth. It is 3.4× smaller than the $1\times V_{DD}$ design due to the need of a larger load resistor and one extra pole formed internally. Nevertheless, this speed penalty is acceptable for many applications.

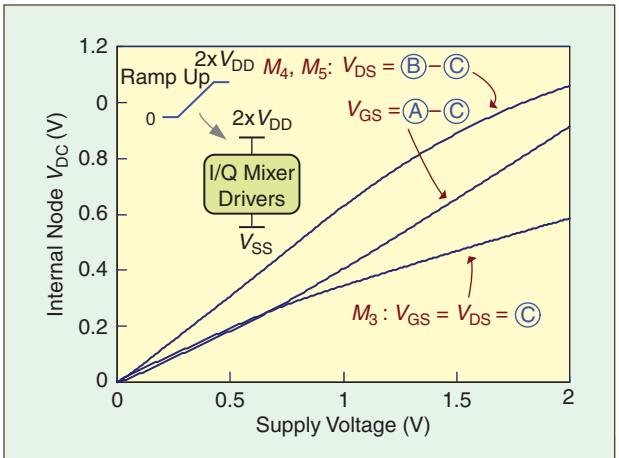

Figure 14. Simulated DC-node voltage variation of Fig. 13(b) with the $2\times V_{DD}$ ramps up from 0 to 2 V.

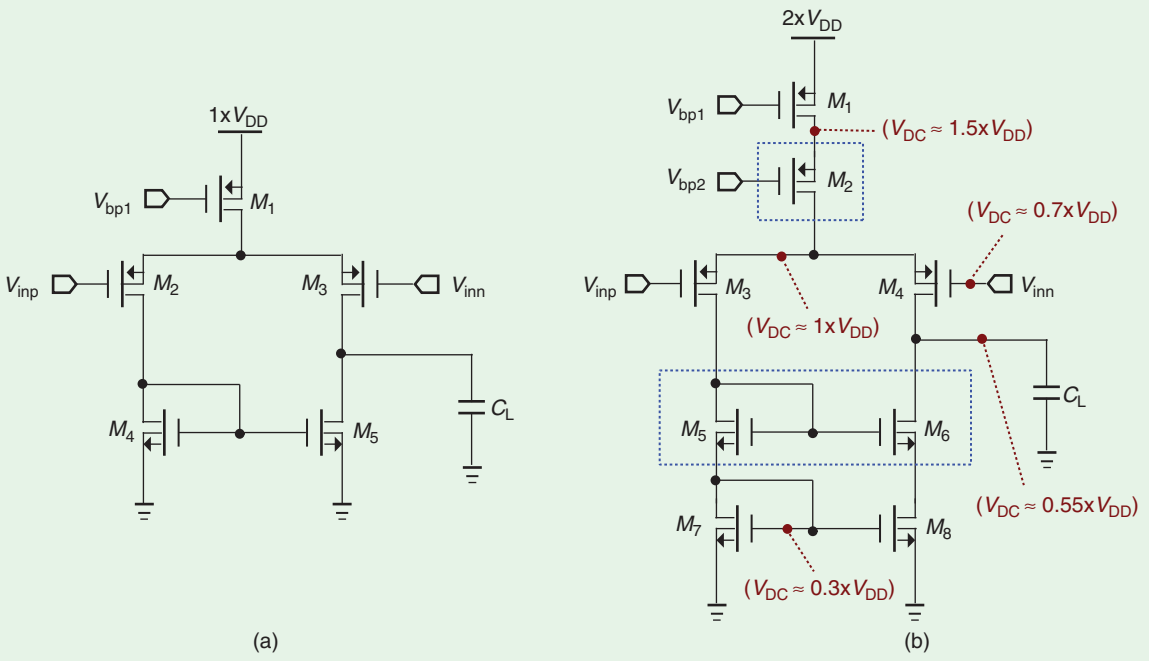

Figure 15. OpAmp's input stage with a current mirror load: (a) 1 V (typical) (b) 2 V-enabled.

E. Operational Amplifier (High-V_{DD} + Thin-Oxide Transistor)

A 3.3-V 0.18-μm CMOS two-stage operational amplifier (OpAmp) was demonstrated in [12]. The concept of extending the voltage is related with the addition of extra cascode transistors, boosting the voltage-withstand capability from 1.8 to 3.3 V. The input stage is of particular interest as it is based on a high-voltage-enabled differential pair using a current mirror load. In order to understand the performance difference in an advanced process, we re-design and compare only the input stage of the OpAmp (output stage is more customized) in 65-nm CMOS, as shown in Fig. 15(a) and (b). Table 3 summarizes the simulation results showing that the dc gain and linear output swing of the 2-V design are 8.4 dB and 2.6 times better than its 1-V counterpart, respectively. On the other hand, the unity-gain frequency is reduced by 40% due to the additional parasitic poles in the 2-V design. Thus, when the speed is not that demanding, a 2-V-enabled OpAmp is better since OpAmp-based circuits such as the active filter are normally for baseband operation.

Table 3.
Comparison between 65-nm 1-V and 2-V OpAmp's input stage with a current-mirror load.

Parameters	1 V OpAmp's Input Stage	2 V OpAmp's Input Stage
Technology	65 nm CMOS	
Transistor type	1V GP NMOS and PMOS	
Power consumption	0.4 mW	
Load C_L	1 pF	
DC gain	10 dB	18.4 dB
Unity-gain frequency	318.5 MHz	191 MHz
Phase margin	107°	95°
HD3 (at 1 MHz input)	45.6 dB at 125 mV_{pp} Output	44.3 dB at 330 mV_{pp} Output
Output noise voltage (at 100 MHz)	14.6 nV/sqrtHz	14.7 nV/sqrtHz

F. OpAmp-Based Analog-Baseband Circuits (High-V_{DD}+ Thin-Oxide Transistor)

A V_{DD}-elevated OpAmp can lead to a wide range of analog-baseband circuits which will take advantage of area and power savings. The general topology is shown in Fig. 16. Depending on the wanted impedances of Z_{fb} and Z_{ff} several types of continuous-time and discrete-time circuits can be synthesized. Its power and area advantages are particularly obvious for quadrature (I/Q) wireless systems that require many OpAmps for realizing high-order channel-selection filters and programmable-gain amplifiers.

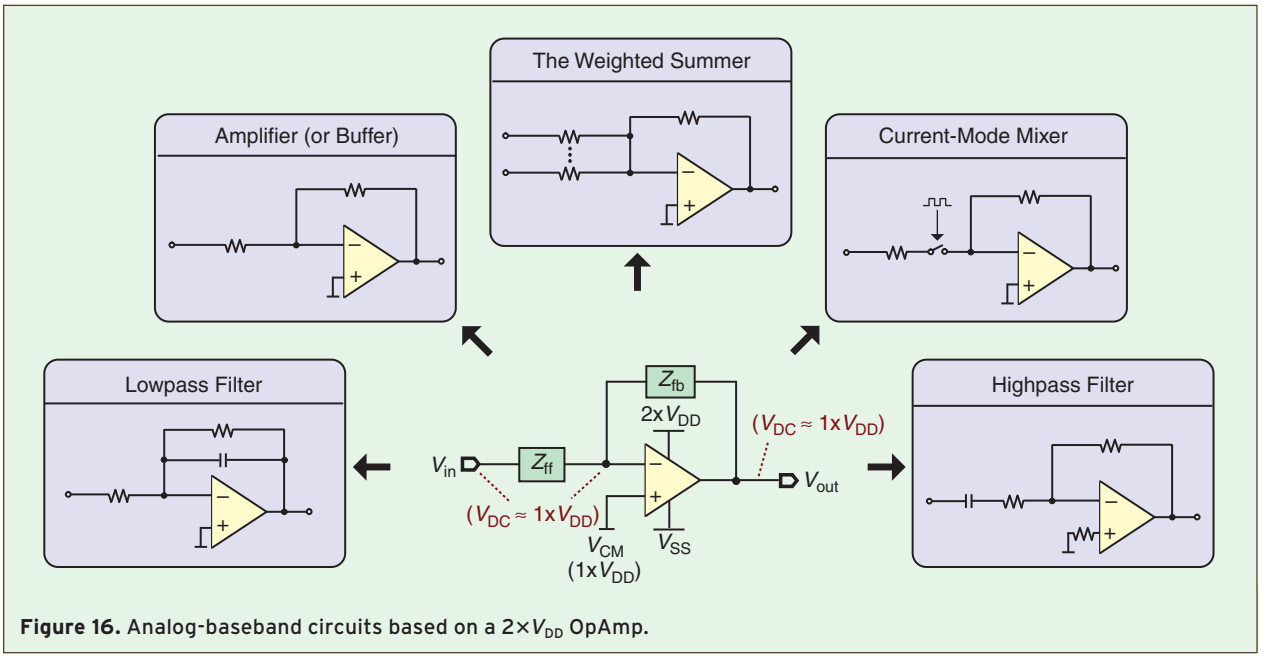

Figure 16. Analog-baseband circuits based on a $2\times V_{DD}$ OpAmp.

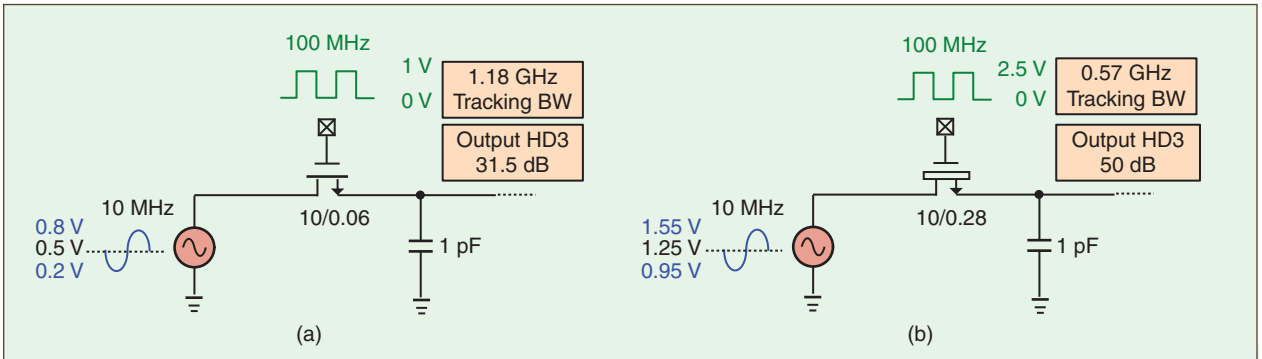

Figure 17. Sample-and-hold circuits: (a) 1-V design. (b) 2.5-V design.

G. Sample-and-Hold Amplifier (High-V_{DD}+ Mixed-Transistor)

Discrete-time analog-baseband circuits not only can benefit from the area and power savings of a V_{DD}-elevated OpAmp, but also the extra voltage headroom to improve the linearity of sampling. Shown in Fig. 17(a) and (b) are two sample-and-hold circuits with 1-V and 2.5-V supplies, respectively. At a 100-MHz sampling rate, to sample-and-hold a 10-MHz 0.6-V_{pp} sinusoidal input at a dc level that is midway to $V_{DD}/2$, the former based on thin-oxide MOS with a minimum channel length of 60 nm can achieve 1.18-GHz tracking bandwidth (BW) but the HD3 is limited to 31.5 dB. Alternatively, the latter based on thick-oxide MOS with a minimum channel length of 280 nm can achieve 50-dB HD3, but the tracking BW is almost halved. Then, this speed-linearity tradeoff is subject to applications and can be flexibly selected in advanced processes, as both thin- and thick-oxide devices are available. Since the clock is normally synthesized with the thin-oxide circuit for power and area reduction, a clock level shifter, as shown in Fig. 18, would be required for the 2.5-V design.

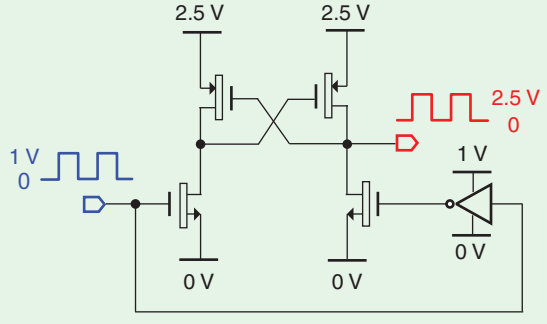

Figure 18. Clock level shifter for 1 to 2.5 V.

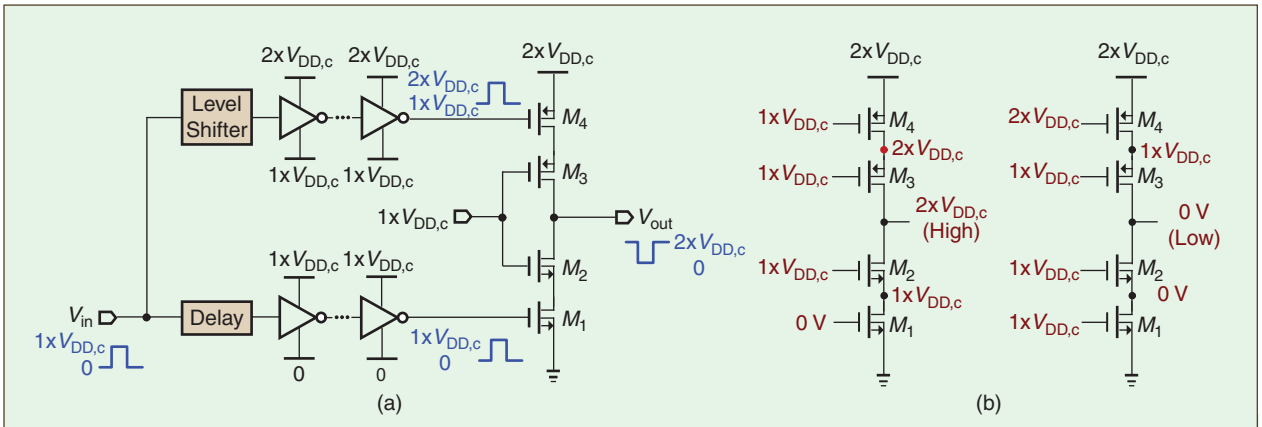

Figure 19. (a) CO line driver with a $2\times V_{DD,c}$. (b) The internal node voltages when the output stage is delivering high and low-state outputs showing all voltage differences are within $1\times V_{DD,c}$.

H. Line Driver (High-V_{DD} + Thin-Oxide Transistor)

Ref [13] has demonstrated that a 5.5-V line driver realized in a standard 1.2-V 0.13-μm process is capable to attain state-of-the-art performances with no reliability degradation. Figure 19(a) depicts the block schematic of such a line driver topology (the output stage), where a $2\times V_{DD,c}$ supply is adopted for simplicity. The input signal is delayed (to synchronize with the upper path) and buffered to drive the NMOS device M_1, besides being also level-shifted up to drive the PMOS device M_4. The cascode transistors M_2 and M_3 serve to increase the voltage-withstand capability. With a $2\times V_{DD,c}$ supply, the gate-bias voltages of M_2 and M_3 are very simple, i.e., $1\times V_{DD,c}$ to ensure no overstress in both high- and low-state outputs [Fig. 19(b)]. For a higher V_{DD} multiplying design (i.e., greater than 2), a dedicated bias circuit for each cascode transistor is necessary to guarantee no device is under overstress in both steady-state and transient operations. The circuit needs two supplies $1\times V_{DD,c}$ and $2\times V_{DD,c}$. The application-related performance metrics are available elsewhere [3], [13].

VI. Conclusions

High-/mixed-voltage RF and analog CMOS circuits feature high potential to boost up the performances of advanced nanometer-scale chips without degrading the reliability. Bringing the $V_{DD,IO}$ and thick-oxide transistors into the RF and analog circuit design portfolio does not by itself require any add-on resource or technology option, but effectively increase the design flexibility. Circuit techniques play a key role in this development, and are therefore long-term reusable when the technology continues to advance.

This article only serves as a glimpse of this research trend and guiding direction, while highlighting the necessary gate-drain-source engineering skills to take a broader advantage of available techniques. One of the critical points would be to guarantee the circuit reliability compliance with the foundry guidelines when considering device size and the potential adopted bias in transient and steady states. Advantages of high-/mixed-voltage RF and analog CMOS circuits have been demonstrated by several recent works, and are believed to be easily extendable to other circuits and systems in different applications.

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