A $2 \times V_{DD}$-Enabled Mobile-TV RF Front-End With TV-GSM Interoperability in 1-V 90-nm CMOS

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***Abstract*—A $2 \times V_{DD}$-enabled mobile-TV RF front-end with TV-GSM interoperability is described. It is an on/off-chip codesign employing externally three customized UHF/VHF preselect filters, an RF switch, and a balun. The integrated part includes: 1) a cascode–cascade inverter-based low-noise amplifier that features a high gain-to-power efficiency; 2) a linearized $C-2C$ attenuator using reliably-overdriven MOS switches; 3) an inductive-peaking feedforward path that evens out the passband variation; and 4) two cascode I/Q mixer drivers capable to drive passive mixers with small gain and bandwidth reduction. Gate-drain-source engineering and self-biased structures are the keys enabling performance optimization with low power and no reliability risk. Fabricated in a 90-nm CMOS process with 1-V thin-oxide devices, the RF front-end measures 68-dB rejection at GSM-900 uplink, 0.7-dB passband roll-off, 3.9-dB noise figure, and −5.5-dBm third-order intercept point at a maximum voltage gain of 26.2 dB. The core occupies 0.28 mm^2 and draws 15 mW. The achieved power-performance metrics compares favorably with the prior state of the art.**

***Index Terms*—Attenuator, CMOS, DVB-H, GSM-rejection filter, high-voltage circuits, inverter amplifier, ISDB-T, low-noise amplifier (LNA), MediaFLO, mixer, mobile TV, RF integrated circuit (RFIC), T-DMB, TV-GSM interoperation, TV tuner, ultrahigh frequency (UHF), very high frequency (VHF).**

I. Introduction

CONTINUED downscaling of transistor gate length and oxide thickness has led to the development of low-voltage-enabled high-performance analog and RF CMOS circuits [1], [2]. Inside the sub-1-V supply voltage (V_{DD}) regime, the design challenges are more severe than ever [3], [4]. Threshold voltage (V_T) cannot be scaled much because of transistor variability, matching and leakage issues. The tradeoff between signal swing and transistor overdrive sets the hurdle for power-performance optimization.

In this sense, high-voltage (HV)-enabled circuits emerge as a feasible alternative to cope with the sub-1-V technologies at low cost. Fig. 1 shows the nominal V_{DD} and V_T scaling roadmaps with process advancements. Arrived at the 90-nm CMOS node and beyond, an elevated V_{DD} outpacing the nominal value becomes an effective way for restoring back more voltage headroom. A high V_{DD}-to-V_T ratio directly opens up a great deal of flexibility in defining circuit topologies while ensuring a sufficient dynamic range for analog and RF signal processing. Evidently, design-for-reliability becomes a mandatory concern for preventing device overstress. The general advantages of HV-enabled circuits can be discussed by using the following two examples.

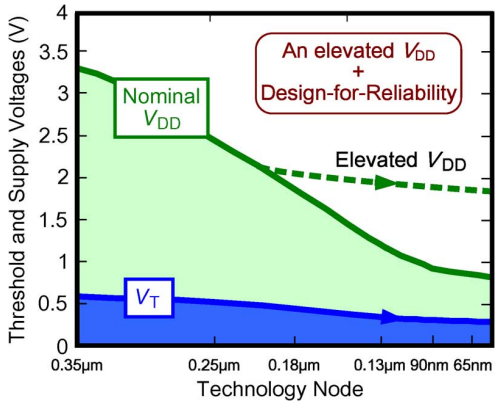

Fig. 1. Elevated V_{DD} ensures voltage headroom but requires design for reliability.

As shown in Fig. 2(a), a hybrid-transistor power amplifier (PA) [5] permits exploiting an elevated V_{DD} to enhance the power efficiency. The thin-oxide transistor featuring a high f_T can serve as the input device to maximize the speed. The thick-oxide transistor, serving as the cascode device, effectively multiplies up the voltage-withstand capability of the PA and improves its reverse isolation.

Alternatively, as shown in Fig. 2(b), a V_{DD}-elevated ultra-wideband (UWB) balun low-noise amplifier (LNA) [6] increases the output dynamic range while allowing a larger load resistance (RL_1), resulting in both high gain and high dynamic range. Obviously, a large RL_1 can notably limit the output bandwidth (BW). Subject to different applications, a gain-peaking inductor LL_2 can be employed to address the BW issue.

This paper describes novel HV-enabled RF circuits that are fully compliant with standard technologies. Only thin-oxide transistors are required, avoiding the need of thick-oxide devices and expensive specialized-HV devices (e.g., laterally diffused MOS). The proof-of-concept prototype is a $2 \times V_{DD}$ mobile-TV tuner RF front-end. The integrated part includes an LNA, a $C-2C$ attenuator, a gain roll-off compensation

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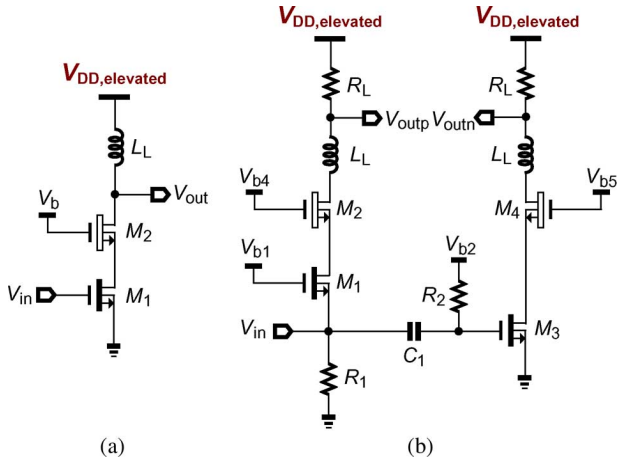

Fig. 2. RF circuits using an elevated V_{DD}. (a) PA. (b) Wideband balun LNA.

path, and two I/Q mixer drivers. Fabricated in a 1-V 90-nm CMOS process, the RF front-end achieves performance metrics that are competitive with the prior state-of-the-art technologies while consuming lower power. The experimental results were reported briefly in [7]. This paper extends significantly the presentation with more circuit insights and definitive materials. The reason for choosing just a *doubled* V_{DD} is due to the fact that nanoscale technologies have a nominal V_{DD} of around 1 V. A $2 \times V_{DD}$ implies typically a 2-V supply, which can be easily generated by a 3.6∼3.7-V Li-ion battery using a low-dropout regulator (LDO). In RF systems, LDO is widely employed to improve the power-supply rejection ratio of the driven circuit.

The second key contribution of this study is related to the fact that the proposed RF front-end supports both typical reception and TV-GSM interoperation through an on/off-chip co-design. TV-GSM interoperation has been the subject of intense research in recent years [8]. A nearby GSM-900 interferer complicates the tuner from receiving the VHF-III and UHF bands (170–860 MHz), where most of the mobile-TV standards such as DVB-H, ISDB-T, T-DMB, and MediaFLO are broadcast. A customized off-chip preselect filter in conjunction with an on-chip gain roll-off compensation technique realizes sufficient rejection at the GSM-900 band, while ensuring a flat passband.

Section II outlines the fundamental reason of adopting an elevated V_{DD}. Section III overviews the tuner architecture with emphasis on TV-GSM interoperation. Section IV describes the design and simulation of each building block. Section V reports the experimental results and benchmarks the work to the literature. Section VI concludes this paper.

II. Fundamentals for Adopting an Elevated V_{DD}

The basis for adopting an elevated V_{DD} are illustrated through analyzing the relationship between V_{DD} and the dynamic range of a common-source (CS) amplifier with a resistive load, as shown in Fig. 3. The channel-length modulation is neglected for simplicity. The input-referred squared noise voltages imputable to M_1 and R_L are given, respectively, by

$$\overline{V_{n,\mathrm{M1}}^2} = 4kT\frac{1}{g_m}\gamma \tag{1}$$

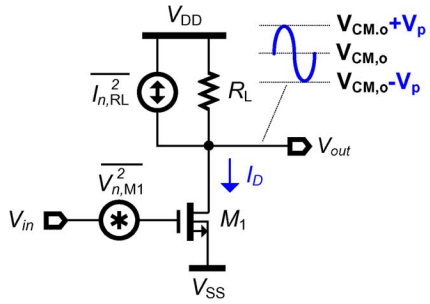

Fig. 3. Typical CS amplifier with a resistive load.

and

$$\overline{V_{n,\mathrm{RL}}^2} = \overline{I_{n,\mathrm{RL}}^2}\frac{1}{g_m^2} = \frac{4kT}{R_L}\frac{1}{g_m^2} \tag{2}$$

where γ is the noise factor and g_m is the transconductance of M_1, k is the Boltzmann's constant, and T is the temperature (in Kelvins). The generic $I-V$ equation of a MOSFET considering the mobility degeneration parameter θ is given by

$$I_D = \frac{1}{2}\frac{W}{L}\mu_o C_{ox}(V_{GS}-V_T)^2\frac{1}{1+\theta(V_{GS}-V_T)} \tag{3}$$

where W/L is the aspect ratio of the transistor and $\mu_o C_{ox}$ is the transconductance parameter. From (3), the input-referred third-order intercept point (IIP3) of a MOSFET can be calculated [9] as

$$V_{IIP3}^2 \approx \frac{8}{3}\frac{V_{GS}-V_T}{\theta} = \frac{16}{3}\frac{I_D}{g_m\theta}. \tag{4}$$

With (1), (2), and (4), the dynamic range $\mathrm{DR_{CS}}$ of the CS amplifier can be calculated as

$$\mathrm{DR_{CS}} \approx \frac{V_{IIP3}^2}{\overline{V_{n,\mathrm{M1}}^2}+\overline{V_{n,\mathrm{RL}}^2}} = \frac{4}{3}\frac{I_D}{kT\theta\left(\gamma+\frac{1}{|A_{V,DC}|}\right)} \tag{5}$$

where $A_{V,DC}$ is the dc voltage gain as given by

$$A_{V,DC} = -g_m R_L. \tag{6}$$

In practice, I_D cannot be arbitrarily increased to maximize the $\mathrm{DR_{CS}}$. Next, it will be observed how V_{DD} and the bias condition limit the achievable $\mathrm{DR_{CS}}$. Since the output common-mode voltage $V_{CM,o}$ must be within V_{DD}, we have

$$V_{CM,o} = xV_{DD} = V_{DD} - I_D R_L \tag{7}$$

where x denotes a ratio value <1 and can be conveniently set to 0.5 for $V_{CM,o} = V_{DD}/2$. Re-arranging (7) yields

$$I_D = \frac{V_{DD}(1-x)}{R_L}. \tag{8}$$

Substituting (8) back into (5), the $\mathrm{DR_{CS}}$ can be re-expressed as

$$\mathrm{DR_{CS}} = \frac{4}{3}\frac{V_{DD}}{R_L}\frac{1-x}{kT\theta\left(\gamma+\frac{1}{|A_{v,dc}|}\right)}. \tag{9}$$

From (9), it can be deducted that the most straightforward manner to increase the $\mathrm{DR_{CS}}$ is by elevating the V_{DD}. From gain-to-power-efficiency's viewpoint, it would be preferable to

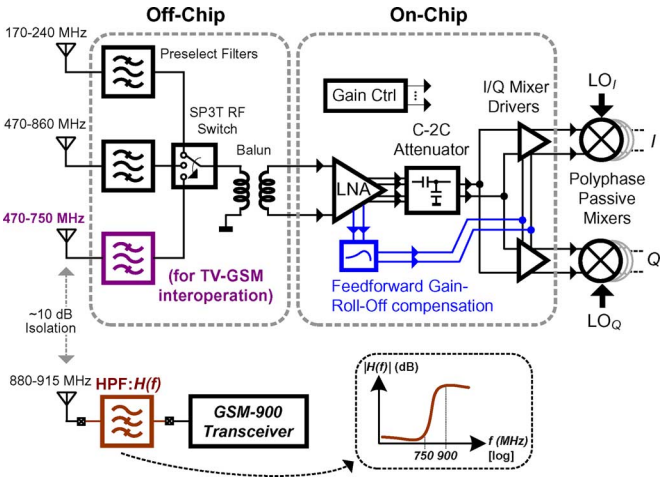

Fig. 4. Proposed on/off-chip codesigned mobile-TV tuner RF front-end supporting VHF-III (170–240 MHz) and UHF (470–860 MHz) bands in typical reception mode and narrower UHF (470–750 MHz) band in TV-GSM interoperation mode.

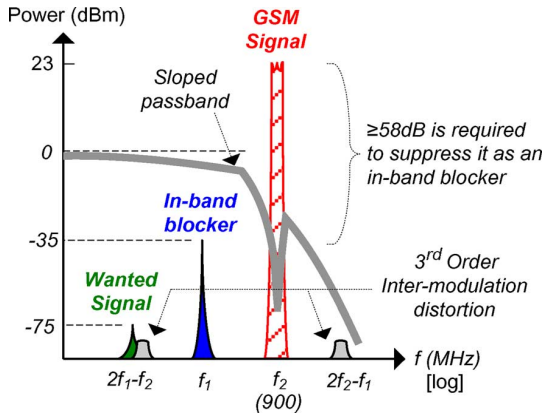

Fig. 5. 170–750-MHz preselect filter's profile for receiving the TV band in the presence of GSM-900 uplink.

boost the voltage gain by increasing $R_{\rm L}$ but not $g_{\rm m}$ ($g_{\rm m} \propto \sqrt{I_{\rm D}}$ for a given transistor size), as an equal increment of $V_{\rm DD}$ can help to maintain the $\rm DR_{CS}$ fairly unchanged under the condition that $\gamma \gg 1/|A_{\rm V,DC}|$. Assuming a conservative value of $\gamma = 5/3$ [10], $|A_{\rm V,DC}|$ should be equal to 6 (15.5 dB) for $\gamma = 10/|A_{\rm V,DC}|$, which is a reasonable value to be achieved.

An analogous observation exists for inductively-degenerated CS LNA and Gilbert-cell mixer as addressed in [9] and [11]. Obviously, $V_{\rm DD}$ cannot be arbitrarily increased to maximize the $\rm DR_{CS}$ due to reliability limitations. Boosting the device reliability by transistor stacking [12] has been one of the ways to push upward the drain–source voltage withstand capability of MOS devices. The major device reliability concerns of an ultrascaled CMOS process include the absolute maximum rating (AMR), hot carrier injection (HCI), negative bias temperature instability (NBTI), time-dependent dielectric breakdown (TDDB), and punchthrough effect [13]. Their implications to the circuit structures based on the employed 1-V 90-nm CMOS process will be justified in the text wherever appropriate.

III. Tuner Architecture for TV-GSM Interoperation

Fig. 4 shows the proposed $2 \times V_{\rm DD}$-enabled mobile-TV tuner RF front-end. It supports VHF-III (170–240 MHz) and UHF (470–860 MHz) bands in typical reception mode, and narrower UHF band (470–750 MHz) in TV-GSM interoperation mode. A direct-conversion architecture [14] facilitates the frequency plan and hardware reuse for multiband multistandard mobile-TV applications [15]. The external passives include an off-the-shelf balun, an off-the-shelf SP3T RF switch, and three customized preselect filters built with surface-mount devices (SMDs). A wideband LNA covering the VHF-III and UHF bands is employed as it can cover both VHF-III to UHF bands without demanding reconfigurability [16]. The LNA has to exhibit low noise, high gain, and gain control such that the noise contribution of the latter circuitry is minimized. However, due to the high gain of the LNA, the linearity of the front-end is limited by the $C-2C$ attenuator and I/Q mixer drivers. Since a $2 \times V_{\rm DD}$ helps improving linearity with low overhead as discussed in Section II, techniques for improving the linearity of the $C-2C$ attenuator and I/Q mixer driver are developed. All circuit blocks are differential to desensitize them from bondwire variation, while minimizing common-mode pickups and even-order nonlinearity. An inductive-peaking feedforward path is added to even out the passband variation. The reason for the LNA to have three sets of differential outputs will be addressed later in Section IV. The gain control is implemented digitally in three steps: 1) the LNA provides a one-step high-/low-gain control; 2) the $C-2C$ attenuator offers a coarse gain control with a 6-dB step size; and 3) the I/Q mixer driver renders a fine gain control with a 0.75-dB step size.

The rationale for employing three preselect filters is related to the fact that, in the frequency range of interest, the VHF-III band suffers from harmonic mixing if only one preselect filter is adopted, since the UHF band is located at the third harmonic of the local oscillator (LO) when downconverting the VHF-III band by hard-switching mixers. This drawback is overcome by separation of the VHF-III and the UHF prefilters with transference of the mixers to a polyphase harmonic-rejection mixer scheme [17], [18]. The VHF-III prefilter serves to reject the interferers located at the harmonics of the LO, whereas the mixer scheme interpolates a pseudo sinewave to suppress the third and fifth harmonics of the LO.

The preselect filter for the narrower-UHF band supports the TV-GSM co-integrated terminals. The presence of the GSM-900 service poses a strict challenge to the tuner operating in the UHF band [19]. Fig. 5 outlines the spectrum of TV-GSM interoperation, where the upper cutoff frequency is reduced from 860 to 750 MHz, as allowed by the DVB-H specifications [20]. Since the isolation between the tuner and GSM transceiver is limited to roughly 10 dB, external filtering is required for seamless TV-GSM interoperation. For the GSM transceiver, a forefront off-chip high-pass filter (HPF) minimizes its leakage power from increasing the tuner's input noise floor. For the tuner, a preselect filter having a notch at 900 MHz is required. An attenuation level of not less than 58 dB is necessary to guarantee the GSM-900 uplink signal, with a maximum power level of +33 dBm, still aligned with the maximum input power outlined by the DVB-H standard. Such a rejection requirement cannot be simply fulfilled by an off-the-shelf TV-tuner filter

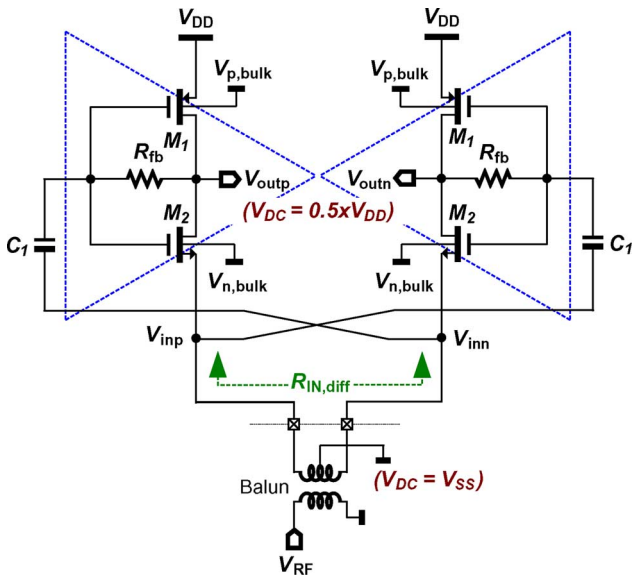

Fig. 6. $1 \times V_{DD}$ inverter LNA. Input dc level is assumed to be at V_{ss} (0 V).

[21]. Typically, with no intent of TV-GSM interoperation, only 30-dB attenuation at GSM-900 uplink is provided. Moreover, due to a limited Q factor, a sloped passband is induced.

Here, a customized preselect filter and a feedforward gain roll-off compensation path are applied concurrently in the TV-GSM interoperation mode to meet the GSM-rejection profile, while maintaining the flatness of the passband prior to down-conversion. Likewise, the input-referred noise around the transition frequency will not be significantly degraded.

Other design specifications are concisely summarized here as they have been extensively reported in the literature [15], [22]. The representative linearity specification is given by the $L1$ pattern test of DVB-H, i.e., the TV tuner has to demodulate a 16-QAM signal when there are two interferers, one digital (40-dB stronger) and one analog (45-dB stronger), two and four channels away from the desired, respectively. This test sets the IIP3 to -5 dBm together with a noise figure (NF) of 8 dB. The sensitivity specification is also given by the DVB-H standard. At the maximum gain a NF of 5 dB is required. This value includes the insertion loss (IL) of the external components.

IV. On/Off-Chip Circuit Design

All of the integrated circuits are of differential architecture, though several schematics are shown in their single-ended equivalents for simplicity.

A. Basic Cell of the LNA

Here, we describe the basic cell of the LNA that can be easily upscaled to $2 \times V_{DD}$ operation. As shown in Fig. 6, a $1 \times V_{DD}$ inverter-type amplifier with the NMOS's source terminal as the input enables a wideband input-impedance match. The capacitive cross-coupling technique [23] reuses the gate–source transconductance (g_m) of both nMOS and pMOS devices, resulting in an improved gain-to-power efficiency. In this subcircuit level, the input dc voltage is set at 0 V ($V_{DC} = V_{SS}$) through the off-chip balun. The gate voltage is self-biased by the feedback resistor R_{fb}, resulting in an ouput dc voltage halfway of the supply (i.e., $0.5 \times V_{DD}$) that can maximize the linear output swing. The differential voltage gain $A_{V,diff}$ is given by

$$\begin{aligned} A_{V,\text{diff}} &= \frac{V_{\text{outp}} - V_{\text{outn}}}{V_{\text{inp}} - V_{\text{inn}}} \\ &= \left(g_{m1} + 2g_{m2} + \frac{1}{r_{o2}} - \frac{1}{R_{fb}} \right) \\ &\quad \times (r_{o1} // r_{o2} // R_{fb}) \end{aligned} \tag{10}$$

where $g_{m1,2}$ and $r_{o1,2}$ are the transconductance and output resistance of $M_{1,2}$, respectively. The overall transconductance (G_m) corresponds to the term $g_{m1}+2g_{m2}+1/r_{o2}-1/R_{fb}$ which can be approximate to $g_{m1}+2g_{m2}$ for sufficiently large r_{o2} and R_{fb}, implying roughly a tripled increment of transconductance when comparing to that achieved by a single transistor. With $V_{DD} =$ 1 V, proper sizings lead to $|V_{GS}| = |V_{GD}| = |V_{DS}| =$ 0.5 V for both M_1 and M_2. Given that $|V_T|$ of the thin-oxide nMOS and pMOS transistors is roughly 0.3 V, each transistor is biased in strong inversion with $|V_{GS} - V_T| =$ 0.2 V. The G_m-to-I_b ratio is $\sim 30\ V^{-1}$ and the output dynamic range is 0.6 V_{pp}.

The use of M_2's source node as the input terminal realizes a wideband input impedance match. It can be shown that the differential input resistance $(R_{IN,diff})$ of the LNA is given by

$$R_{\text{IN,diff}} = \frac{2}{2g_{m2} + \frac{1}{R_{fb}} + \left(\frac{1}{R_{fb}} - \frac{1}{r_{o2}} \right) A_{V,\text{diff}}}. \tag{11}$$

which can be simplified to a handy and observable form as follows:

$$R'_{\text{IN,diff}} \approx \frac{2}{g_{m1} + 4g_{m2}} \tag{12}$$

when r_{o1} and r_{o2} are assumed to be infinite. However, in nanoscale technologies, (11) is essential for an accurate calculation of $R_{IN,diff}$. $R_{IN,diff}$ and the total input parasitic capacitance C_{IN} determine the value and BW of the input reflection coefficient magnitude $|\Gamma_{IN}|$, as given by

$$|\Gamma_{\text{IN}}| = \left| \frac{\frac{1}{j\omega C_{\text{IN}}} // R_{\text{IN,diff}} - R_S}{\frac{1}{j\omega C_{\text{IN}}} // R_{\text{IN,diff}} + R_S} \right| \tag{13}$$

where R_S denotes the output resistance of the test source. The finite output impedance of M_1 and M_2 complicates the optimization between voltage gain, BW and NF under an impedance-match condition. For the sizing of each component, a constraint-based semi-computed design flow [24] is applied to optimize those parameters concurrently. It is noteworthy that the capacitive cross-coupling technique and the use of an off-chip balun for signal injection allows effective noise and distortion cancellation of M_2.

Self-biased inverter-based circuits are sensitive to process, voltage, and temperature (PVT) variation. The back-gate control scheme highlighted in [25] is an effective solution for this problem. It keeps the supply current constant and reduces the sensitivity to supply ripple by returning the correcting signals to $V_{p,bulk}$ and $V_{n,bulk}$. A triple-well process is required to isolate the bulk of nMOS from substrate. Because this work is the very first proof-of-concept prototype, this back-gate control scheme has not been embedded.

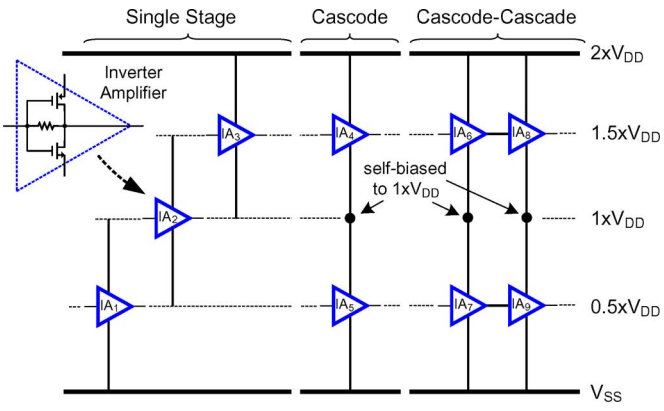

Fig. 7. Three $2 \times V_{\rm DD}$ partitioning schemes for the LNA.

Since the linearity of the receiver is mainly limited by the I/Q mixer drivers, the main design consideration of the LNA is to operate it reliably under a $2 \times V_{\rm DD}$ with guaranteed reliabilty. The associated biasing is simplified by introducing a $V_{\rm DD}$ *partitioning* concept. Based on it, a $2 \times V_{\rm DD}$ *cascode-inverter* LNA, and a $2 \times V_{\rm DD}$ *cascode-cascade-inverter LNA* that befits the proposed RF front-end, are developed.

1) $V_{\rm DD}$ Partitioning Concept: In order to reliably bias the thin-oxide transistors under an elevated supply, it is convenient to equally divide the supply into four regions, as shown in Fig. 7. From left to right, under $2 \times V_{\rm DD}$, a $1 \times V_{\rm DD}$ inverter-type amplifier ($\rm IA_1$ to $\rm IA_3$) can be connected in three different ways without affecting the performance and reliability. Such an amplifier is self-biased by a feedback resistor. It can be observed that the inter-rail voltage levels ($0.5 \times V_{\rm DD}$, $1 \times V_{\rm DD}$ and $1.5 \times V_{\rm DD}$) call for additional circuitry for generating the inter supply rails. This overhead, however, can be avoided by exploiting a *cascode* of two identical inverter amplifiers ($\rm IA_4$ and $\rm IA_5$). The intermediate point is still the RF input node, self-biased to a value close to $1 \times V_{\rm DD}$ because of voltage division. Due to a matched I/O dc level, the voltage gain can be enhanced further by cascading the cascoded inverter amplifiers ($\rm IA_6$ to $\rm IA_9$), without needing any ac coupling.

2) $2 \times V_{\rm DD}$ Cascode-Inverter LNA: Fig. 8 describes the transformation of a $1 \times V_{\rm DD}$ inverter LNA into a $2 \times V_{\rm DD}$ cascode-inverter LNA. It is noteworthy that the main objective is to keep the RF performance, power consumption and output resistance remain unchanged, but the voltage capability is doubled. The LNA is structured by, first, splitting the $1 \times V_{\rm DD}$ inverter LNA into two, relying on the principle of device parallelism. The second is stacking them together. The reliability of all devices is maintained at static and power-up/down transient as the dc-levels of all internal nodes follow linearly with the $2 \times V_{\rm DD}$ when it ramps up (see Fig. 8, right). Due to the separation of circuits from 1 to 2, the output impedance of each output ($V_{\rm out1}$ and $V_{\rm out2}$) is doubled from its original $1 \times V_{\rm DD}$ design. This issue can be solved by ac-shorting the dual outputs passively by a capacitor, or actively by another gain stage as shown in Fig. 9. The latter can further boosts the RF gain, at the expense of the BW (since $V_{\rm out}$ is of even higher output impedance). The reliability is guaranteed simply by adding two cascode devices $M_{\rm cp}$ and $M_{\rm cn}$ with resistor $R_{\rm b}$ for the drain–gate bias.

Here, the passive combination has been selected for its excellent linearity and the facts that the required summing capacitor can be merged into the subsequent programmable $C - 2C$ attenuator and the gain of the supply and ground noises to the single-ended output can be remarkably reduced. The gain enhancement is modified as a double capacitive cross-coupling technique. Thus, the bias point, and the net voltage stressed on each transistor, are unaltered when compared with a generic $1 \times V_{\rm DD}$ design. This feature contrasts with the outside-rail HV circuits [26] which operates with large signals, the trajectories of the device terminal voltages in transients must be controlled to be within the reliability limits such as HCI, TDDB, and punchthrough. The factor k is introduced as a correction constant since the roles of nMOS and pMOS in the lower inverter are switched compared with the upper one. It is possible to design without k, but it helps ensuring that the upper and lower inverters can achieve the same RF performances. The bulk of $M_2(M_3)$ should be tied to its source to avoid voltage overdrive between the bulk and source terminals. The bulks of M_1 and M_4 can be used to desensitize the circuit from PVT variation as mentioned before. The dc level of the input node is self-biased to a value close to $1 \times V_{\rm DD}$ (halfway of the elevated supply).

3) $2 \times V_{\rm DD}$ Cascode-Cascade-Inverter LNA: Its schematic is shown in Fig. 10. Adding one more gain stage boosts gain and permits gain switching without affecting the input impedance match. The second stage is realized by A_3 and A_4 that are inverter-like CS amplifiers offering a simple gain-bypass mode by using a switch (SW) in parallel with $R_{\rm fb2}$. Considering the upper path involving A_1 and A_3, the voltage gain $A_{\rm V,A3}$ of A_3 in the high-gain mode can be expressed by

$$A_{\rm V,A3} = \frac{V_{\rm out,2nd}}{V_{\rm in,2nd}} = \frac{g_{m5} + g_{m6} - \frac{1}{R_{\rm fb2}}}{\frac{1}{r_{o5}//r_{o6}} + \frac{1}{R_{\rm fb2}}} \tag{14}$$

where $g_{m5,6}$ and $r_{\rm o5,6}$ are the transconductance and output resistance of $M_{5,6}$, respectively. In the low-gain mode, $R_{\rm fb2}$ is reduced (in parallel with the ON-resistance of the SW). The input resistance of $A_3 R_{\rm IN,2nd}$ is given by

$$R_{\rm IN,2nd} = \frac{R_{\rm fb2} + r_{o5}//r_{o6}}{1 + (g_{m5} + g_{m6})(r_{o5}//r_{o6})}. \tag{15}$$

Since $R_{\rm IN,2nd}$ loads to A_1, the gains of A_1 and A_3 are simultaneously reduced in the low-gain mode when $R_{\rm fb2}$ is decreased, effectively increasing the linearity. Note that no reliability issue is induced as the gain control involves no change of bias point. The consideration applies for the lower path involving A_2 and A_4. One particular feature of this LNA is that, in addition to the two high-impedance output terminals ($V_{\rm out1p}$ and $V_{\rm out2p}$), a low-impedance output terminal ($V_{\rm out3p}$) is available, which will be reused for gain roll-off compensation (to be described in Section IV-F).

The simulated performances of the standalone LNA is shown in Fig. 11. At *no load* condition, the high-gain mode shows 31.4-dB voltage gain, 2.8-dB NF, and $S11 < -10$–dB BW of 0.1–1.5 GHz. At the low-gain mode, the performances are 21.1-dB voltage gain, 3.6-dB NF, and $S11 < -10$–dB BW of 0.1–1.56 GHz. An in-band two-tone test at 400 and 500 MHz shows an IIP3 of −3.3/5.4 dBm at high-/low-gain mode. The

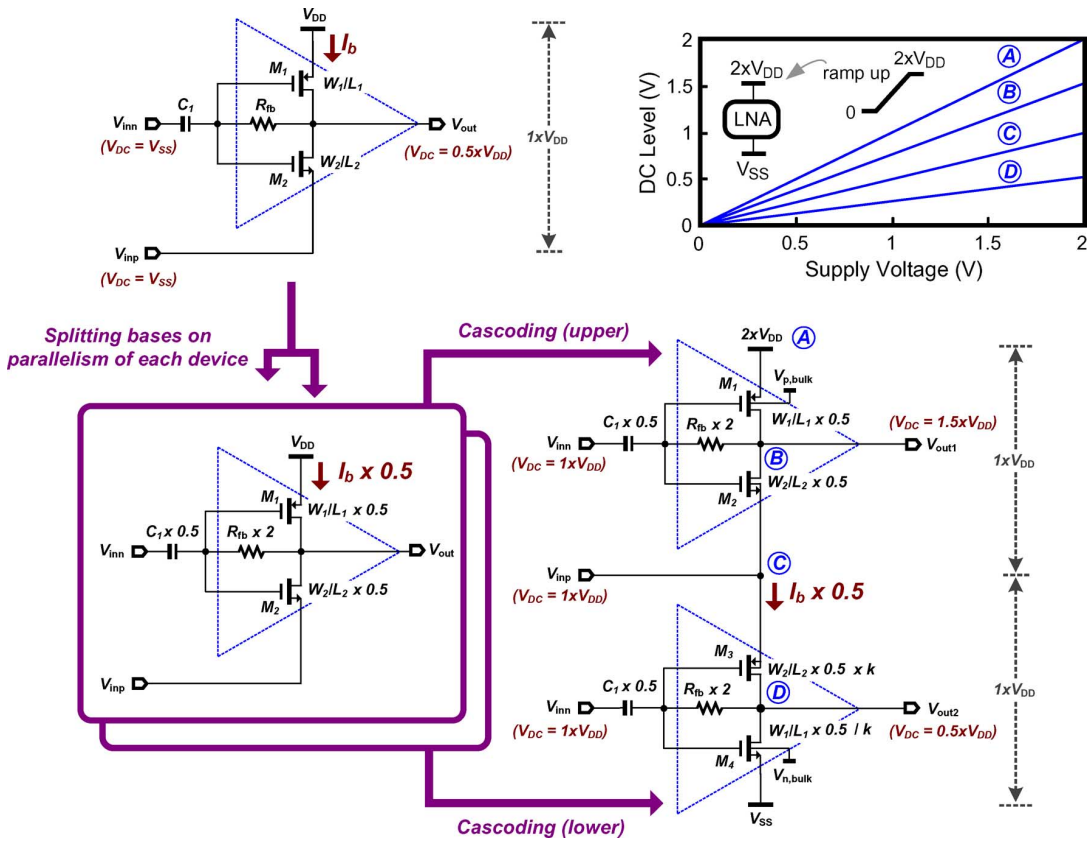

Fig. 8. Constant-power constant-performance transformation of a 1 × V_{DD} inverter LNA into a 2 × V_{DD} cascode-inverter LNA (simplified half circuit).

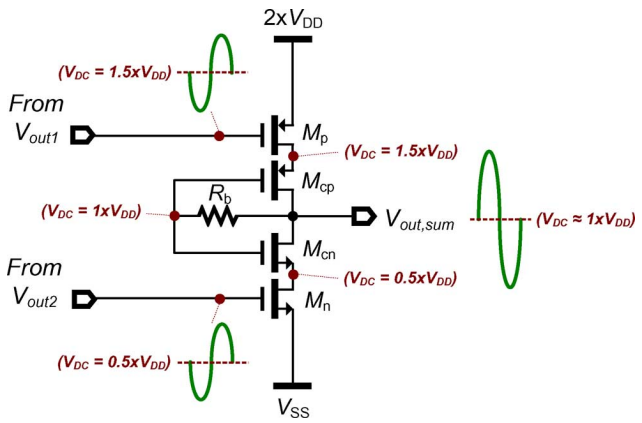

Fig. 9. 2 × V_{DD} cascode-inverter LNA with its dual outputs combined actively by a dual-input cascode amplifier.

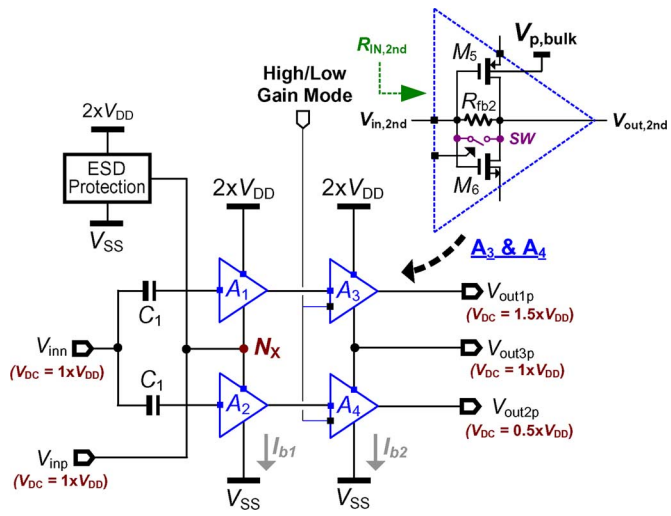

Fig. 10. 2 × V_{DD} cascode–cascade-inverter LNA with triple output terminals and high/low-gain mode (simplified half circuit).

LNA draws 9.8 mW at 2 V. It is noteworthy that those performance metrics exclude the loading effect of the $C - 2C$ attenuator and I/Q mixer drivers. Cosimulations between blocks are necessary to justify the overall RF performances.

B. ESD Protection Scheme

Since N_X (see Fig. 10) is self-biased internally by the LNA at a dc level halfway of the supply, it is convenient to apply forward-connected diode chains to boost the ESD protection level. As shown in Fig. 12, D_3's and D_4's are three substrate pnp diodes, which, together with the reverse-biased diodes (D_1 and D_2) and power clamp construct the ESD protection scheme. In the ESD-robustness simulation, a human body model (HBM) voltage pulse is applied to the LNA's input to induce a large $+/-$ zapping discharge current that has a rising/falling time of ∼8 ns [27]. As verified in all combinations, the RF input pins can withstand minimally ±4 kV of ESD zapping without causing internal or protection devices failure. This result fulfills the standard of "safe level" in the chip-level ESD specifications. The main concern is the induced nonlinear parasitic capacitance, which is roughly 0.2 pF in this design. With a rail-to-rail

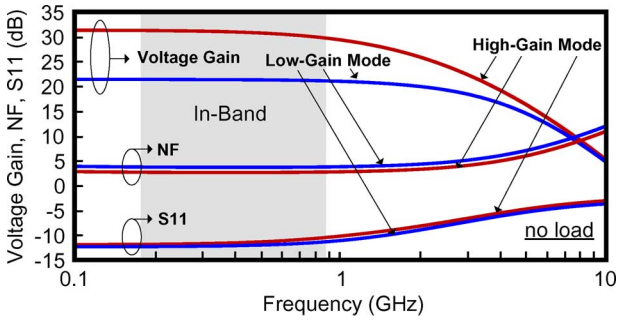

Fig. 11. Simulated performances of the standalone LNA with no load.

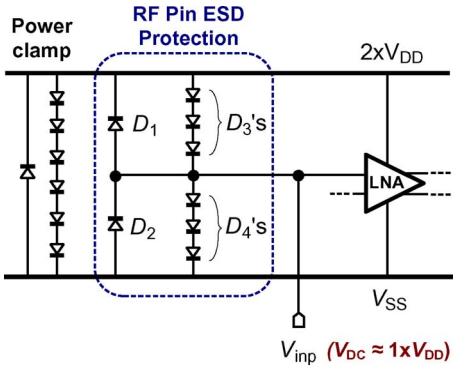

Fig. 12. ESD protection scheme of the RF input pin.

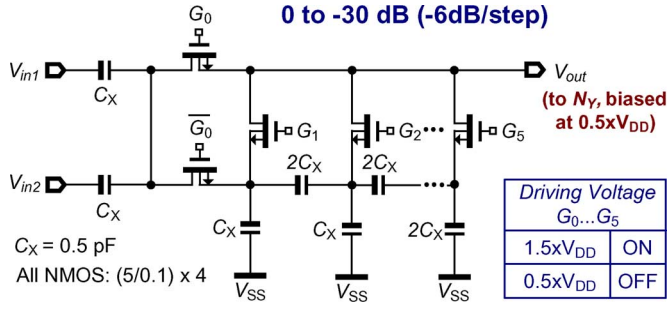

Fig. 13. Programmable $C-2C$ attenuator for coarse-gain control. The input capacitor $2C_{\rm x}$ is divided into $2C_{\rm x}$'s to interface with the LNA.

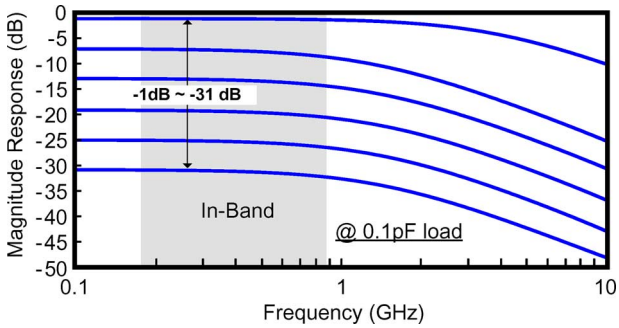

Fig. 14. Simulated magnitude response of the $C-2C$ attenuator.

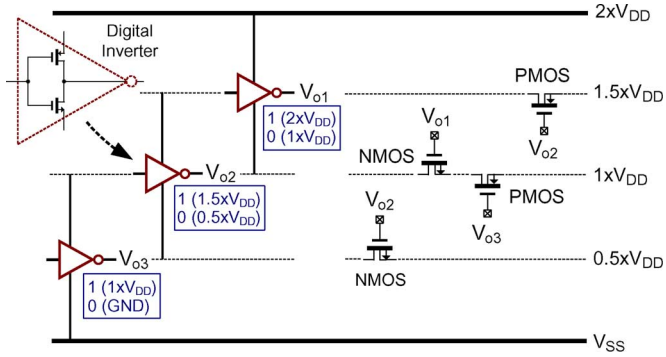

Fig. 15. Appropriate digital inverters for switches operating at different supply rails. They drive nMOS and pMOS switches correspondingly, such that $V_{\rm GS}$ of $1\times V_{\rm DD}$ in ON-state can be achieved in the four cases shown.

sinewave applied at the input, the total harmonic distortion is 0.1%.

C. Programmable $C-2C$ Attenuator

The linearity of the I/Q mixer driver limits that of the entire TV tuner because of the voltage gain of the LNA. Instead of utilizing the current-steering gain-control method [28] that can affect the operating points, a passive $C-2C$ attenuator (Fig. 13) is inserted between the LNA and the I/Q mixer drivers to control coarsely the dynamics of the RF signal. Conveniently, the input capacitor can be divided into two equally sized capacitors ($C_{\rm x}$'s) for passively combining the LNA's upper ($V_{\rm out1p}$) and lower ($V_{\rm out2p}$) outputs. The five-stage attenuator offers an attenuation range $A_{\rm v}=0$ to $-$30-dB with a $-$6-dB step size, i.e., $A_{\rm v}=G_{\rm n}(2)^{-n}$ for $n=0,1,\ldots 5$, where $G_{\rm n}=(0,1)$ is the gate control logic for switching the attenuation levels. Sizing $C_{\rm x}$ has a tradeoff between the accuracy and BW. An increase of $C_{\rm x}$ value can desensitize the gain step from parasitic capacitances, whereas a decrease of $C_{\rm x}$ value can maximize the BW. Here the optimized $C_{\rm x}$ is 0.5 pF for the targeted BW. The simulated magnitude response of the $C-2C$ attenuator is shown in Fig. 14. The ON-resistance of the switches and capacitor size determine the BW of the attenuator, which is well over 1 GHz among all attenuation levels. The output is not buffered before driving the mixer driver, inducing 0.1-dB passband gain loss under a 0.1-pF load, which models the input capacitance of the mixer driver.

An elevated $V_{\rm DD}$ helps minimizing the size and nonlinearity of MOS switches. In the proposed $V_{\rm DD}$ partitioning scheme there are four gain switching methods using digital inverters, as shown in Fig. 15. nMOS and pMOS switches using the corresponding inverter ensure $V_{\rm GS}=1$ V in the ON-state, $V_{\rm GS}=0$ V in the OFF-state. The main reliability concern of the $C-2C$ attenuator is the bias temperature instability (BTI), because all switches conduct no static current, and to overcome it, triple-well nMOS switches allowing bulk-source connection are employed as they are far less affected by BTI than the pMOS devices. The associated tradeoff is that nMOS requires a deep n-well to permit bulk-source connection, which is a cheap option that is widely available in advanced processes. The parasitic capacitances associated with the deep-n-well diodes have to be accounted to minimize gain-step error. The terminal voltage $N_{\rm Y}$ is purposely set to $0.5\times V_{\rm DD}$ (0.5 V) to interface with the I/Q mixer drivers. As such, the gain-control logics [G_0 to G_8] can be reliably up-shifted to $1.5\times V_{\rm DD}$ (1.5 V) in the ON-state. Considering AMR and TDDB, the RF input signals ($V_{\rm in1}$ and $V_{\rm in2}$) can be as large as 0.4 $V_{\rm pp}$. In the linear region, a 0.5-V increment of overdrive ($V_{\rm GS}-V_{\rm T}$) leads to a better linearity and a smaller

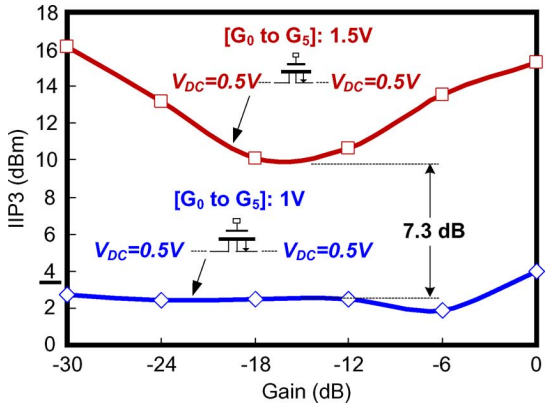

Fig. 16. IIP3's of the $C-2C$ attenuator with 1-V and 1.5-V gate voltages. The triple-well nMOS switches are biased at a DC level of 0.5 V.

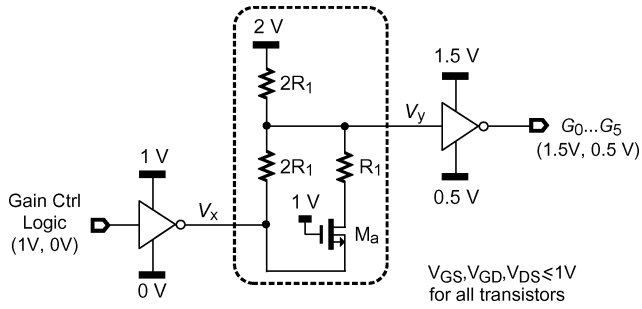

Fig. 17. $0.5 \times V_{DD}$-up level shifter.

transistor size for a given ON-resistance (R_{ON}). The R_{ON} of a CMOS transistor based on a first-order model is given by

$$R_{ON} = \frac{1}{\mu_o C_{ox} \frac{W}{L}(V_{GS} - V_T)}. \quad (16)$$

The simulated IIP3 of the $C-2C$ attenuator under a 50-Ω source impedance with 1.5-V and 1-V gate-control voltages are shown in Fig. 16. The former achieves +9.8–+16.1 dBm IIP3 among an attenuation range of 0–−30 dB, showing minimally 7.3-dB improvement of IIP3 when comparing it with the latter.

The involved $0.5 \times V_{DD}$-up level shifter is shown in Fig. 17. It features a simple structure to realize low-to-high transition from 0/1-V input to 0.5/1.5-V output. When the input is logic 1 (1 V), V_x is close to ground, the MOS switch M_a is turned ON (with a resistance much smaller than R_1), yielding $V_y \approx$ 0.5 V [i.e., $2\text{ V} \cdot (2R_1//R_1)/(2R_1//R_1 + 2R_1)$] and making [$G_0$ to G_5] equal to logic 1 (1.5 V). On the other hand, when the input is logic 0 (0 V), M_a is OFF, yielding $V_y \approx$ 1.5 V [i.e., $(2\text{ V} - 1\text{ V}) \cdot (2R_1)/(2R_1 + 2R_1) + 1\text{ V}$] and making [$G_0$ to G_5] equal to logic 0 (0.5 V). It can be verified that all terminal voltages of MOS devices satisfy the reliable limits. The required reference voltages are generated by an on-chip high-ohmic polysilicon resistor ladder.

D. I/Q Mixer Drivers

The proposed I/Q mixer drivers (Fig. 18) are based on a cascode structure with a resistive load to drive a passive mixer. It benefits the most from an elevated V_{DD} in terms of linear output swing and reverse isolation. The fine-gain control [G_6 to

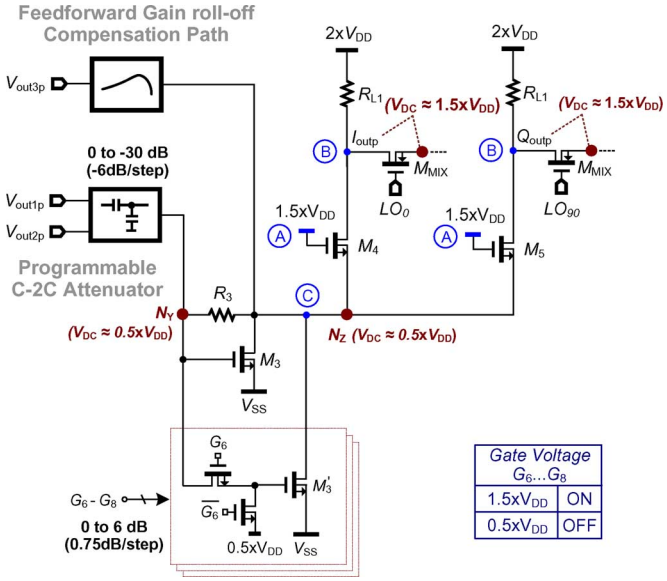

Fig. 18. Proposed cascode I/Q mixer driver. M_3 is partially switchable for fine-step gain control. The low-impedance node N_z interfaces the feedforward path to compensate the gain roll-off.

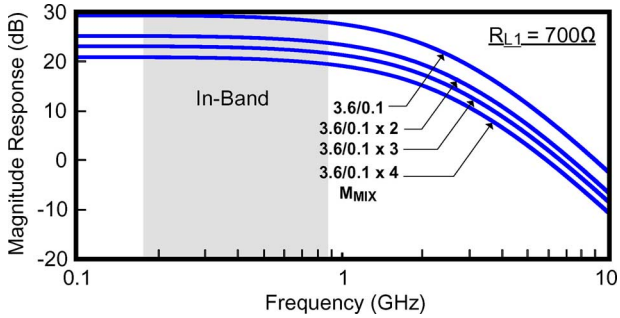

Fig. 19. Magnitude response of the RF front-end at different sizes of the M_{MIX}.

G_8] is set at the ac-switching part of M_3 (i.e., M_3'), covering a 0-to-6-dB gain range with a 0.75-dB step size. The gain-control logics [G_6 to G_8] are up-boosted to $0.5 \times V_{DD}$ in the OFF-state and $1.5 \times V_{DD}$ in the ON-state to improve the linearity, similar to the gain control in the $C-2C$ attenuator. The entire coarse-fine gain control involves no change of bias points, ensuring the reliability in all operating modes. M_4 and M_5 are nMOS transistors with $V_{GS} = V_{DS} = 1 \times V_{DD}$ and are of long channel length (i.e., 1.2 μm) to avoid BTI and punchthrough.

M_3 and M_3' are linearized and self-biased by R_3 at a V_{GS} of $0.5 \times V_{DD}$. They deliver the signal current to the two cascode devices M_4 and M_5 while maintaining adequate reverse and I/Q isolations of 76.3 and 38.4 dB in simulations, respectively. The linear output swing is boosted to 0.6 V_{pp} without jeopardizing the reliability limits in terms of RF stress [29], which is confirmed by checking the trajectories of the terminal voltages in power-up/-down transients.

The mixer driver is to deliver high swing output to a resistive load while ensuring a sufficient voltage gain. When driving a passive mixer realized with MOSFET, a small device size is preferred as the switching power of the LO path can be minimized. The mixer switch M_{MIX} shown in Fig. 19 is of pMOS

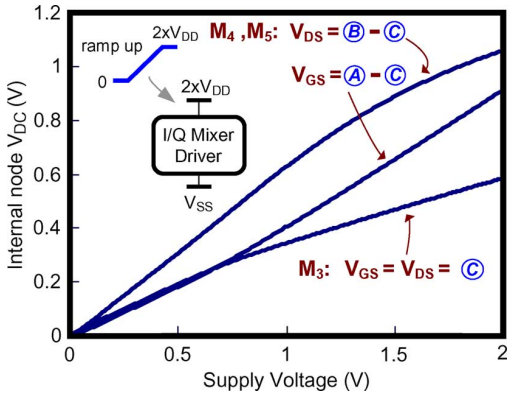

Fig. 20. Simulated dc-node voltage variation of Fig. 18 with the $2 \times V_{\rm DD}$ ramped up from 0 to 2 V.

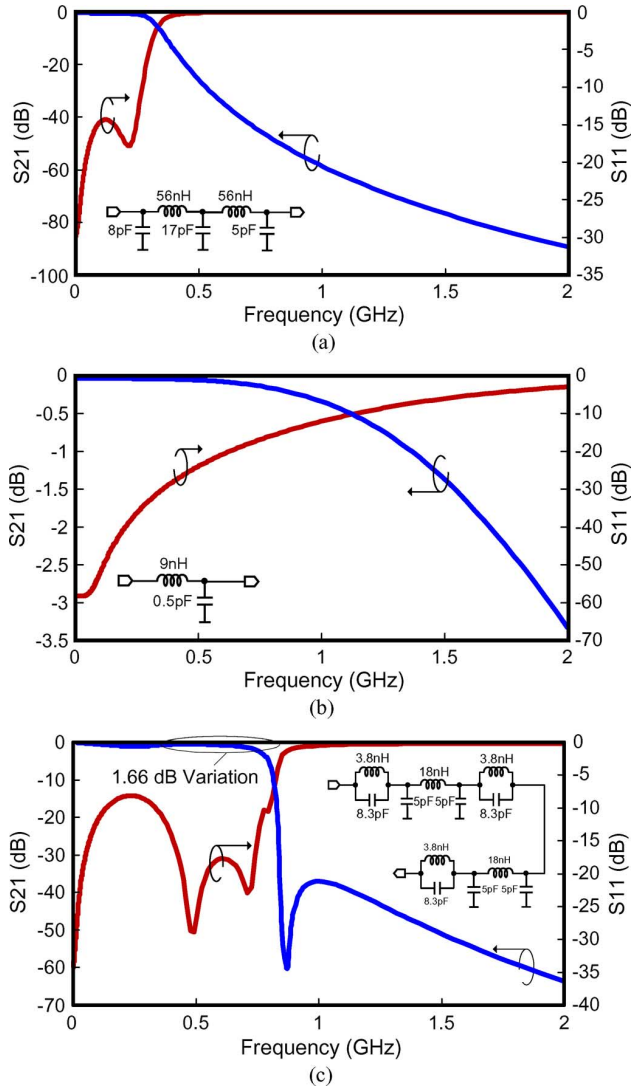

Fig. 21. Simulated S_{21} and S_{11} of the three preselect filters for: (a) 170–240-MHz band; (b) 470–860-MHz band; and (c) 470–750-MHz band.

type to take advantage of the $1.5 \times V_{\rm DD}$ output dc level, increasing the gate–source overdrive in the ON-state as $1 \times V_{\rm DD}$. Since the I/Q mixer driver has resistive input impedance, the loading effect between it and the LNA and the $C - 2C$ attenuator must be taken into account to check the overall gain and output BW under different loads. As shown in Fig. 20, with $R_{\rm L1} = 700\ \Omega$, the voltage gain can be maintained at >20 dB with around 1-GHz overall output BW with sizes of $M_{\rm MIX}$ ranging from $3.6/0.1 \times n$, where n =1, 2, 3, 4. With a 50-Ω RF test source and $M_{\rm MIX}$ sized as 3.6/0.1, the simulated differential voltage gain of the mixer driver is 5.4 dB and IIP3 is +8.6 dBm.

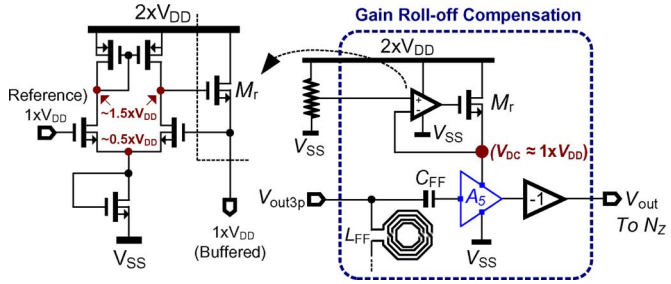

Fig. 22. Simplified schematic of the feedforward gain roll-off compensation path.

The I/Q mixer driver is extensively *voltage* biased to freeze the operating points necessary for reliable operation. Since the DVB-H employs time-slicing operation [20], a resistor ladder generating the reference and bias voltages avoids wrong voltage buildup (remove) sequences in internal nodes during power-up (down) transients. Fig. 20 shows the simulated internal node voltages of the I/Q mixer drivers (markers correspond to Fig. 18) when the $2 \times V_{\rm DD}$ ramps up from 0 to 2 V. It can be observed that the potential differences of all internal nodes are within the reliable guides of AMR and TDDB.

E. External Components

The schematics, S_{21} and S_{11} of the three preselect filters optimized for the 170–240, 470–860, and 470–750 MHz bands, are shown in Fig. 21(a)–(c), respectively. The source and input impedances of the RF front-end are matched with 75 Ω. The Q-factors of surface-mount-device (SMD) inductor and capacitor at 1 GHz are 60 $(Q_{\rm L})$ and 80 $(Q_{\rm C})$, respectively. A 1-pF input parasitic capacitance is assumed to be at the input of the RF front-end. The in-band $|S_{11}|$ is less than −10 dB in all cases. The 470–750-MHz preselect filter achieves 60-dB rejection at 900 MHz at the expense of 1.66-dB passband variation near the cutoff. This effect is addressed by a gain roll-off compensation technique to be described next. The 170–240-MHz preselect filter can achieve more than 30-dB rejection at 510 MHz to prevent the harmonic mixing. In order to measure the frequency response with minimum IL, the 470–860-MHz preselect filter for typical reception is a simplified LC structure.

The selected balun and RF SP3T switch are wideband components. Up to 1 GHz, the 1:2 balun has a 1.2-dB IL [30] and the single-pole triple throw (SP3T) RF switch has a 0.4-dB IL [31].

F. Feedforward Gain Roll-Off Compensation

The gain roll-off due to the 470–750-MHz preselect filter and the finite BW limitation of the LNA and $C - 2C$ attenuator

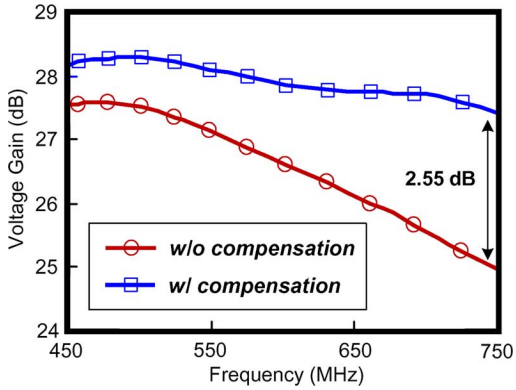

Fig. 23. Simulated magnitude responses of the RF front-end with and without gain roll-off compensation.

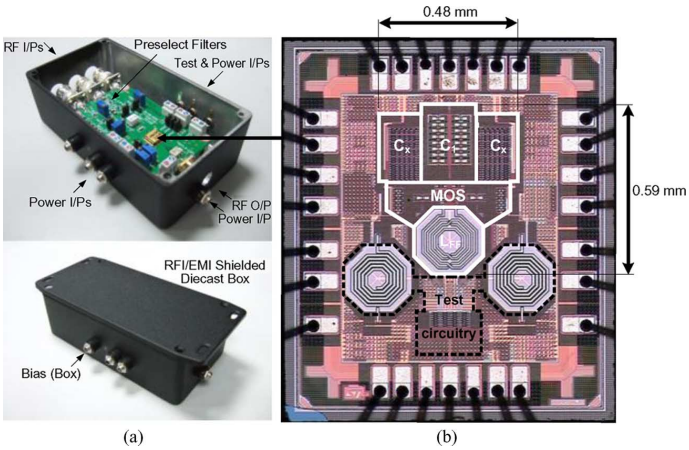

Fig. 24. (a) Test fixture for resisting the ambient GSM signals and (b) chip micrograph of the RF front-end.

in conjunction induce significant gain roll-off near the cutoff. V_{out3p} (see Fig. 10) is a low-impedance output node of the LNA reusable for gain roll-off compensation. Confirmed by on/off-chip cosimulation, a feedforward path (Fig. 22) from V_{out3p} with inductive peaking and amplification realizes a low-Q high-pass characteristic. The gain block of -1 implies cross connection of the differential terminals. It compensates the passband roll-off due to the external preselect filter, the LNA, and the $C - 2C$ attenuator. The inductor L_{FF} is differential for area savings and the amplification is based on another inverter amplifier A_5. Since it is a low-Q peaking, the technique is insensitive to the absolute value of L_{FF}. An error amplifier loop around M_{r} generates a regulated $1 \times V_{\text{DD}}$ supply for reliable operation of A_5. The error amplifier is based on a differential pair with a current mirror load. Its current tail nMOS is diode-connected to allow self-biasing, avoiding any overstress when the $2 \times V_{\text{DD}}$ ramps up. This current tail is sized to consume a voltage stress of $\sim 0.5 \times V_{\text{DD}}$ to reduce the voltage stress on the differential pair and current mirror. The simulated passband flatness with and without compensation is depicted in Fig. 23. The passband flatness is improved by 2.55 dB.

V. Experimental Results, Discussions and Benchmarks

Prototypes of the RF front-end have been fabricated in a 1-V 90-nm CMOS process. The die micrograph and test fixture

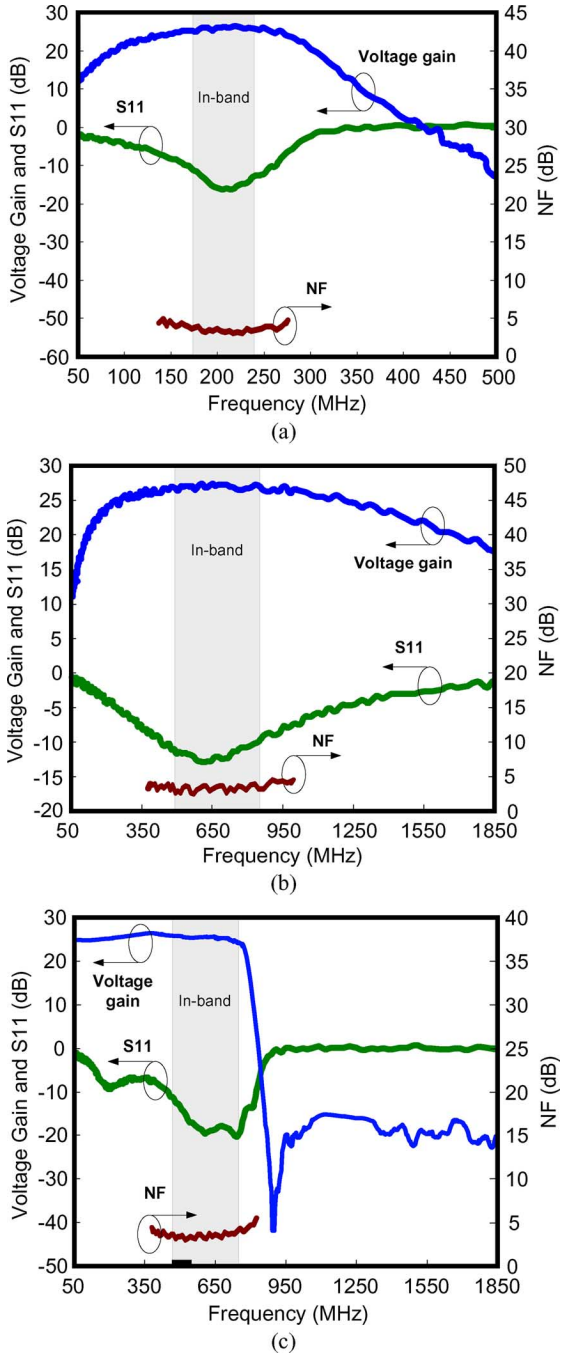

Fig. 25. Measured RF performances of the RF front-end with the corresponding preselect filters for: (a) 170–240-MHz band; (b) 470–860-MHz band; and (c) 470–750-MHz band.

for resisting the ambient GSM signals from affecting the test results are shown in Fig. 24(a) and (b), respectively. The RF front-end employs a single 2-V supply. It occupies 0.28-mm^2 active area and is filled symmetrically by obligatory dummy tiles to avoid mechanical strain differences. The metal lines are set to 1-μm width per 1-mA dc current to prevent electromigration. An inductive-peaking 50-Ω test buffer was designed to drive the equipments since the loading effect of the buffer cannot be simply de-embedded.

Fig. 25(a)–(c) shows the RF performances measured with different preselect filters. The measured peak voltage gain

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART CMOS VGLNAS

	This work			[25]	[34]	[35]	
Frequency (MHz)	170 – 240	470 – 750 [1]	470 – 862	470 – 862	470 – 870	174 – 245	450 – 862
NF (dB)	3.8	3.9	3.5	2.6	4.3	3.0	4.5
Max. Voltage Gain (dB)	24.9	26.2	26.5	23	16	28	25
Rejection at GSM-900 uplink (dB)	67 [2]	68 [2]	2 [2]	n/a	n/a	n/a	n/a
ESD Protection/level (V)	Yes / 4k [3]			no	no	Yes / n/a	
IIP3 (dBm) @ gain (dB)	–5.5 @ 26.2 –1.6 @ 16 (low-gain mode)			–5.4 @ 23 +0.6 @ 9	–1.5 @ 16	–5 to –4 @ 25	
Variable Gain Range (dB)	46			14	33	50	
Power (mW) @ V_{DD} (V)	10 @ 2 (LNA + C-2C Attenuator) 15 @ 2 (+ also I/Q Mixer Drivers)			40 @ 1.2	22 @ 1.8	16 @ 1.8	
Active Area (mm^2)	0.283			0.067	0.32	0.52	
Circuit Topology	Differential			Single-End in Differential Out	Single End	Differential	
Technology	90nm CMOS			90nm CMOS	0.18μm CMOS	0.18μm CMOS	

1: TV-GSM inter-operation mode.

2: With external filters.

3: The ESD protection level is based on HBM simulation.

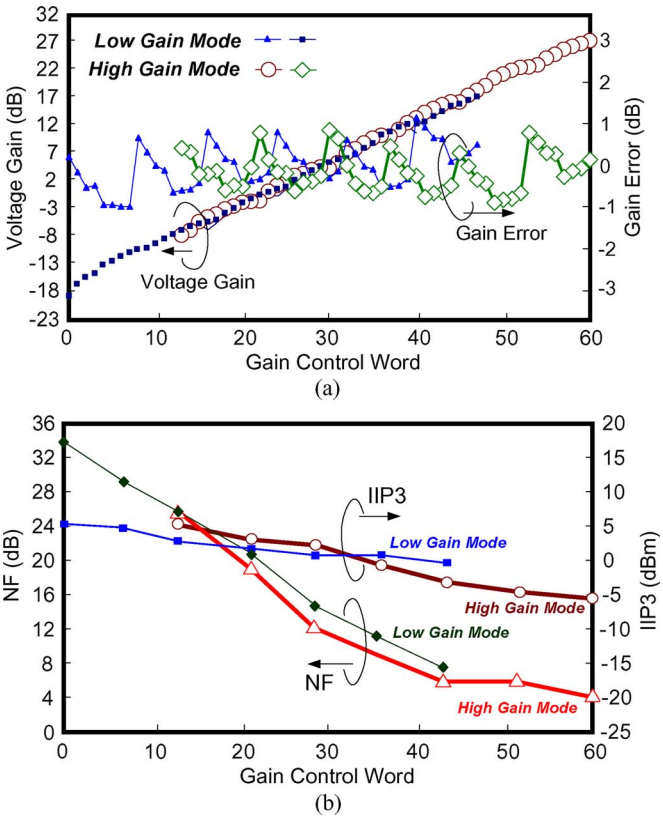

Fig. 26. Measured RF performances against the gain control word at 600 MHz. (a) Voltage gain and gain error. (b) NF and IIP3.

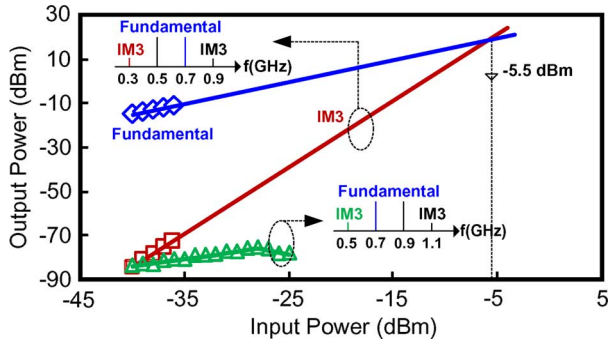

Fig. 27. Linearity measurements with two-tone tests at 0.5 and 0.7 GHz and 0.7 and 0.9 GHz.

ranges from 24.9 to 26.5 dB, and the minimum NF of the RF front-end ranges from 3.5 to 3.9 dB, after de-embedding the loss of the RF switch, balun, and preselect filters. The in-band S_{11} is below -10 dB in all modes. In TV-GSM interoperation mode, the rejection at GSM-900 uplink measures 68 dB and less than 0.7-dB gain roll-off within 470–750 MHz. Since the GSM-rejection filter is realized in a discrete form, post-tuning for alignment is necessary to ensure a stable and accurate notching at GSM-900 uplink against PVT. The manufacturable implementation of the filter prototypes should be with the low-temperature co-fired ceramic (LTCC) technology [32], [33] in the next phase, which can have an accurately controlled frequency response. Fig. 26(a) and (b) shows the voltage gain and gain error, NF and IIP3, measured against the gain-control words, respectively. The gain step error is within ± 1 dB throughout a gain control range of 46 dB. It is believed that this error can be mainly attributed to the $C - 2C$ attenuator, which should be reoptmized with the parasitic capacitance caused by the deep-n-well diodes and the density tilings.

Throughout a 46-dB gain-control range, the IIP3 ranges from -5.5 to $+4$ dBm under a two-tone test at 400 and 500 MHz. Nevertheless, when the RF front-end is switched to the low-gain mode (10-dB gain back-off), an IIP3 of -1.6 dBm together with a minimum NF of 6.4 dB is adequate to pass the DVB-H $L1$ pattern test with low-sensitivity degradation. The RF front-end excluding the test circuitry consumes 15 mW, out of which 10

mW is due to the LNA and the $C - 2C$ attenuator (plus its associated bias circuit).

The desensitization of the RF front-end to the GSM-900 interference is characterized by using two two-tone tests, as shown in Fig. 27. A two-tone test at 0.5 and 0.7 GHz measures an IIP3 of −5.5 dBm. With a preselect filter notching at the 0.9 GHz, the two-tone test at 0.7 and 0.9 GHz shows that the generated third-order intermodulation (IM3) distortion becomes insignificant.

With no access to industrial long-term reliability testers, the reliability of the chip was justified by operating it continuously at room temperature for three days (reference the method described in [13]). No detrimental effect on the performance was noted. Due to a similar reason, the ESD robustness could not be strictly characterized experimentally. The achieved ESD-protection level is based on simulations. Comprehensive system-level measurements including EVM degradation in a TV-GSM co-integrated scenario should be chased in the latter stages of the research, with the presence of the digital demodulator and other analog-baseband circuitry.

There is no similar on/off-chip co-design RF front-end reported in the literature for direct performance comparison. Nevertheless, it is relevant to compare the combined performance of the LNA and $C-2C$ attenuator with the state-of-the-art CMOS variable-gain low-noise amplifiers (VGLNAs) [25], [34], [35] in Table I. With similar NF and linearity performances, this work is advantageous for its lowest power consumption, multistandard conformity and TV-GSM interoperability. The chip area is much larger than [25] due to the reason that, here, a wider gain range is realized, and two I/Q mixer drivers and one gain-roll-off compensation path are implemented. The mixer drivers are capable of driving both resistive and capacitive loads with low gain and BW reduction.

VI. Conclusion

This study demonstrated that RF circuits reliably powered by an elevated V_{DD} are capable of achieving high performances with low power consumption and no reliability risk. The presented proof-of-concept prototype is a 2 × V_{DD}-enabled mobile-TV RF front-end with TV-GSM interoperability. Verified in a 1-V 90-nm CMOS process with standard 1-V thin-oxide devices, the circuit core draws 15 mW at a custom-elevated 2-V supply. In TV-GSM interoperation mode, an inductive-peaking feedforward path evens out the passband to 0.7-dB variation, while showing 68-dB rejection at the GSM-900 uplink. The presented stress-conscious circuit architectures and self-bias techniques are generally applicable for different designs. It is believed that HV-enabled circuits with design-for-reliability possess a high potential in boosting RF circuit performances in sub-1-V technologies at low cost. This research direction has been followed with the main objectives of increasing the circuit portfolio and the integration level.

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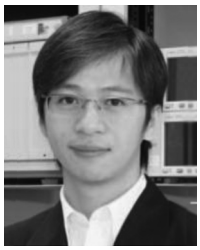

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