Hindawi Publishing Corporation
VLSI Design
Volume 2010, Article ID 706548, 8 pages
doi:10.1155/2010/706548

Research Article

Linearity Analysis on a Series-Split Capacitor Array for High-Speed SAR ADCs

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Received 31 May 2009; Accepted 8 December 2009

Academic Editor: Benjamin J. Blalock

A novel Capacitor array structure for Successive Approximation Register (SAR) ADC is proposed. This circuit efficiently utilizes charge recycling to achieve high-speed of operation and it can be applied to high-speed and low-to-medium-resolution SAR ADC. The parasitic effects and the static linearity performance, namely, the INL and DNL, of the proposed structure are theoretically analyzed and behavioral simulations are performed to demonstrate its effectiveness under those nonidealities. Simulation results show that to achieve the same conversion performance the proposed capacitor array structure can reduce the average power consumed from the reference ladder by 90% when compared to the binary-weighted splitting capacitor array structure.

1. Introduction

The SAR ADC is widely used in many communication systems, such as ultra-wideband (UWB) and wireless sensor networks which require low-to-medium-resolution converters with low power consumption. Traditional SAR ADCs are difficult to be applied in high-speed design; however the improvement of technologies and design methods have allowed the implementation of high-speed, low-power SAR ADCs that become consequently more attractive for a wide variety of applications [1, 2].

The power dissipation in an SAR converter is dominated by the reference ladder of the DAC capacitor array. Recently, a capacitor splitting technique has been presented, which was proven to use 31% less power from the reference voltage and achieve better DNL than the binary-weighted capacitor (BWC) array. The total power consumption of a 5 b binary-weighted split capacitor (BWSC) array is 6 mW which does not take into account the power from the reference ladder [3]. However, as the resolution increases, the total number of input capacitance in the binary-scaled capacitive DAC will cause an exponential increase in power dissipation as well as a limitation with reduction of speed due to a large charging time-constant. Therefore, small capacitance spread for DAC capacitor arrays is highly desirable in high-speed SAR ADCs [4].

This paper presents a novel structure of a split capacitor array for optimization of the power efficiency and the speed of SAR ADCs. Due to the series combination of the split capacitor array both small capacitor ratios and power-efficient charge recycling in the DAC capacitor array can be achieved, leading to fast DAC settling time and low power dissipation in the SAR ADC. The parasitic effects, the position of the attenuation capacitor, as well as the linearity performance (INL and DNL) of the proposed structure will be theoretically discussed and behavioral simulations will be performed. Different from the BWSC array, which only achieves better DNL (but not INL) than the BWC array, the proposed capacitor array structure can have both better INL and DNL than the series capacitor (SC) array. The design and simulations of an 8 b 180-MS/s SAR ADC in 1.2-V supply voltage are presented in 90 nm CMOS exhibiting a Signal-to-Noise-and-Distortion Ratio (SNDR) of 48 dB, with a total power consumption of 14 mW which demonstrates the feasibility of the proposed structure.

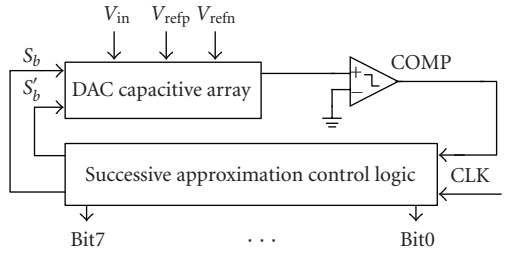

Figure 1: Simplified block diagram of an SAR ADC architecture.

2. The Overall SAR ADC Operation

The architecture of an SAR ADC is shown in Figure 1, consisting of a series structure of a capacitive DAC, a comparator, and successive approximation (SA) control logic. The SA control logic includes shift registers and switch drivers which control the DAC operation by performing the binary-scaled feedback during the successive approximation. The DAC capacitor array is the basic structure of the SAR ADC and it serves both to sample the input signal and as a DAC for creating and subtracting the reference voltage.

3. Capacitor Array Structure

3.1. Capacitor Structure Design. The major limitation on the speed of the SA converter is often related with the RC time constants of the capacitor array, reference ladder, and switches. For a BWC array the size of capacitors rises exponentially with the resolution in number of bits, which causes large power and RC settling time, thus limiting the speed of the overall SAR ADC. To solve this problem, Figure 2(a) shows an SC array [5], which utilizes attenuation capacitors C_{atten} to separate the capacitive DAC into b_M bits MSB and b_L bits LSB arrays. Thus, smaller capacitor ratios can be achieved when compared to the BWC array. However, charge-redistribution switching method for the SC array has been proven to be inefficient when discharging the MSB capacitor and charging the MSB/2 capacitor, which consumes 5 times more power than the charge-recycling switching method. Thus, a series-split capacitor (SSC) array is proposed, as shown in Figure 2(b), which can both alleviate the speed limitation and implement a charge-recycling switching approach.

The solution to perform charge-recycling for SC array is different from the BWC array, which just splits the MSB capacitor C_{MSB} into $n-1$ subarrays. As illustrated in Figure 2(b), the C_{MSB} of the SC array is split into $b_M - 1$ subarrays in the MSB array, where the total capacitance of the b_M-1 subarrays is $C_{MSB} - C_0$ and as a result the capacitors in LSB array and C_{atten} should be doubled; thus the C_{eq} can be calculated as

$$C_{eq} = 2C_{atten} // C_{totalLSB} = 2C_0,$$
$$C_{totalLSB} = 2^{b_L+1}C_0,$$
$$C_{totalMSB} = \sum_{n=1}^{b_M-1} 2^n C_0, \quad (1)$$

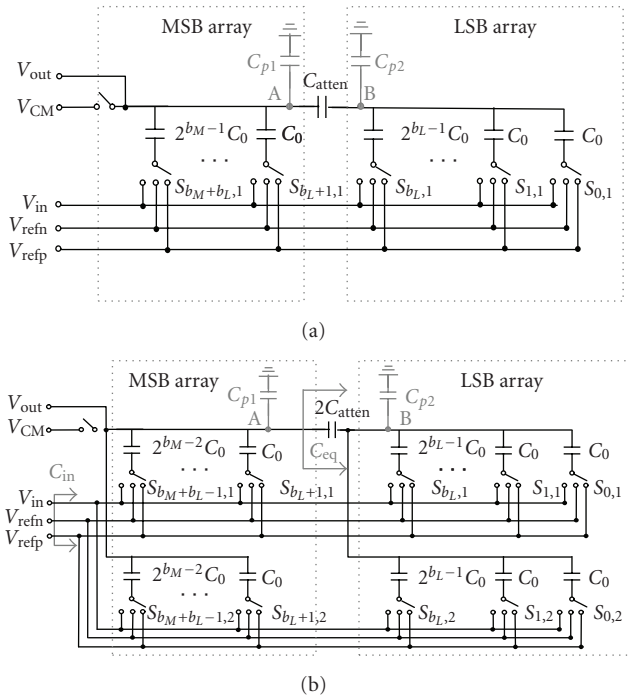

Figure 2: (a) $(b_M + b_L)$-bit SC array, (b) $(b_M + b_L)$-bit SSC array.

where $C_{totalLSB}$ and $C_{totalMSB}$ are the sum of LSB and MSB array capacitors, respectively. The C_{eq} can then be seen as two split unit capacitors C_0 attached to the right side of MSB array to maintain the capacitive ratio as $2^{bM-2} : \cdots : 2 : 1 : 1$. Therefore, the charge-recycling methodology in each section can perform binary-scaled feedback during the successive approximation.

3.2. Charge Recycling Implementation. In the proposed implementation the series-split capacitor array is designed to achieve charge recycling for the n $(n = b_M + b_L + 1)$ bit capacitive DAC, as shown in Figure 2(b). During the global sampling phase, the voltage V_{in} is stored in the entire capacitor array. Then, the algorithmic conversion begins by switching all upper capacitor arrays to V_{ref} and the lower to $-V_{ref}$, respectively, instead of switching only the MSB capacitor to V_{ref} and others to $-V_{ref}$. This implies that in the conversion phase 1 (corresponding to MSB capacitor conversion) V_{out} settles to (considering only differential node voltage)

$$V_{out}[1] = -V_{in} + \frac{V_{ref}}{2} - \frac{V_{ref}}{2} = -V_{in}, \quad (2)$$

and the comparator output will be

$$D_1 = \begin{cases} -1, & V_{in} > 0, \\ 1, & V_{in} < 0. \end{cases} \quad (3)$$

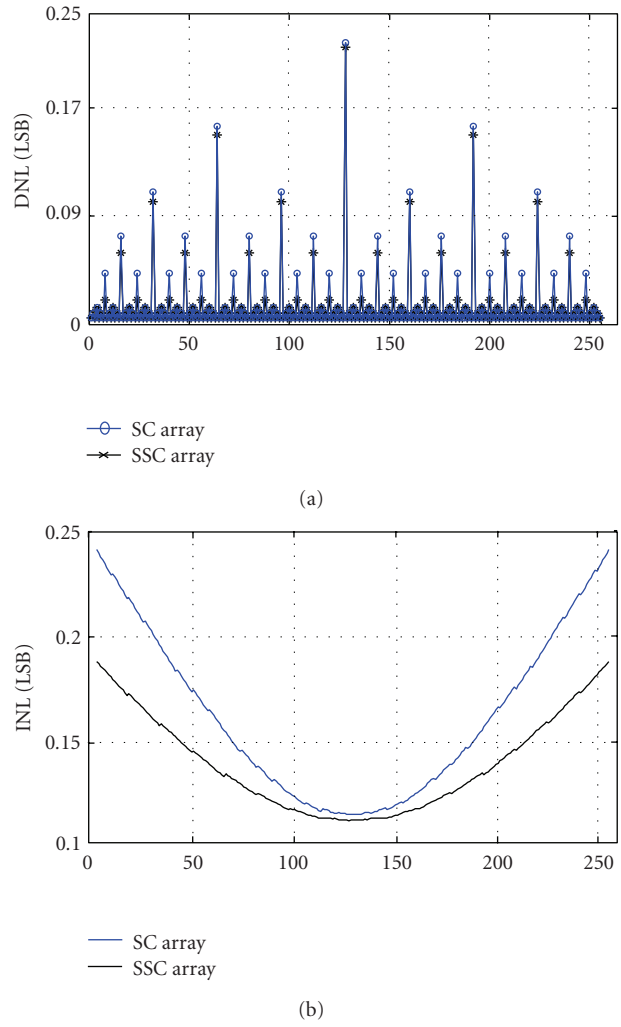

Figure 3: Behavioral simulations comparing the linearity of the SSC and the SC array.

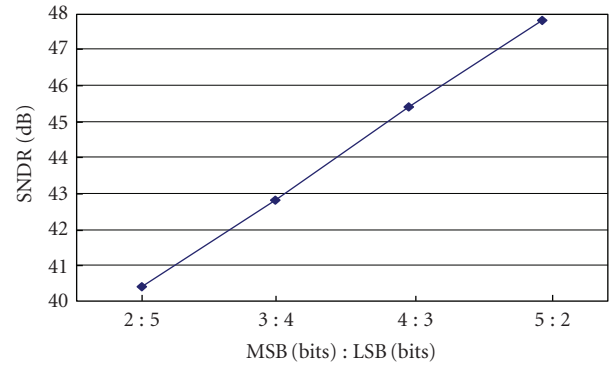

Figure 4: Behavioral simulation of 1000 Monte Carlo SNDR versus the different bits distribution of MSB and LSB arrays.

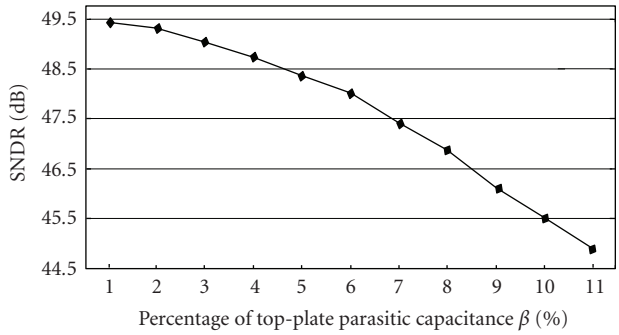

Figure 5: Behavioral simulation of 1000 Monte Carlo SNDR versus the percentage of the top-plate parasitic capacitance β for the SSC array at 8 bit level.

The comparator output will decide the switching logic of $S_{bM+bL-1,1}$ and $S_{bM+bL-1,2}$. If D_1 is low, $S_{bM+bL-1,1}$ is switched to $-V_{\text{ref}}$, dropping the voltage at $V_{\text{out}}[2]$ to $-V_{\text{in}} - V_{\text{ref}}/2$. If D_1 is high, $S_{bM+bL-1,2}$ is switched to V_{ref}, raising the voltage at $V_{\text{out}}[2]$ to $-V_{\text{in}} + V_{\text{ref}}/2$. The above process is repeated for $n-1$ cycles. As $S_{bM+bL-1,1}$ is switched from V_{ref} to $-V_{\text{ref}}$ (bit decision back from "1" to "0") the switches, from $S_{0,1}$ to $S_{bM+bL-2,1}$, are kept connected to V_{ref} and drive $V_{\text{out}}[1]$ to $V_{\text{out}}[2]$. The initial charge, supplied by V_{ref} in phase 1, is kept stored in the capacitors which will connect to V_{ref} at phase 1, instead of being redistributed; so the charge formed at phase 1 can be recycled in the next $n-1$ phases. However, the conventional switching method that discharges MSB capacitor and charges the MSB/2 capacitor will cause charge redistribution in the capacitor array and thus consuming more power.

3.3. Linearity Performance. To analyze the linearity of the SSC and SC arrays, each of the capacitors is modeled as the sum of the nominal capacitance value and the error term, as follows:

$$C_{n,1} = 2^{n-1}C_0 + \delta_{n,1},$$
$$C_{n,2} = 2^{n-1}C_0 + \delta_{n,2}. \tag{4}$$

Consider the case where all the errors are in the unit capacitors whose values are independent-identically-distributed Gaussian random variables with a variance of

$$E\left[\delta_{n,1}^2\right] = E\left[\delta_{n,2}^2\right] = 2^{n-1}\sigma_0^2, \tag{5}$$

and where σ_0 is the standard deviation of the unit capacitor.

The accuracy of an SAR ADC is dependent on the DAC outputs which are calculated here in the case of no initial charge on the array ($V_{\text{in}} = 0$). For a given DAC digital input X, with $D_{n,m}$ equals 1 or 0 representing the ADC decision

for bit n, the analog output $V_{\text{out}}(X)$ of the SSC array can be calculated as

$$\begin{aligned} &V_{\text{out}}(X) \\ &= \frac{2C_{\text{atten}}\left(\sum_{n=1}^{b_L}\sum_{m=1}^{2} D_{n,m}C_{n,m} + \sum_{n=1}^{b_M-1}\sum_{m=1}^{2} D_{n,m}C_{n,m}\right)}{2C_{\text{atten}}(C_{\text{totalLSB}} + C_{\text{totalMSB}}) + C_{\text{totalLSB}}C_{\text{totalMSB}} + \Delta C} V_{\text{ref}} \\ &\quad + \frac{\left(C_{\text{totalLSB}} + \sum_{n=1}^{b_L}\sum_{m=1}^{2} \delta_{n,m}\right)\sum_{n=1}^{b_M-1}\sum_{m=1}^{2} D_{n,m}C_{n,m}}{2C_{\text{atten}}(C_{\text{totalLSB}} + C_{\text{totalMSB}}) + C_{\text{totalLSB}}C_{\text{totalMSB}} + \Delta C} V_{\text{ref}} \end{aligned} \tag{6}$$

where

$$\begin{aligned} C_{n,m} &= 2^{n-1}C_0 + \delta_{n,m}, \\ \Delta C &= \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} \delta_{n,m}(2C_{\text{atten}} + C_{\text{totalLSB}}) \\ &\quad + \sum_{n=1}^{b_L}\sum_{m=1}^{2} \delta_{n,m}\left(2C_{\text{atten}} + C_{\text{totalMSB}} + \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} \delta_{n,m}\right). \end{aligned} \tag{7}$$

Subtracting the nominal value (i.e., $\delta_{n,m} = 0$ in (6)) from (6) the INL can be calculated as

$$\begin{aligned} &\text{INL}_{\text{ssc}} \\ &= \frac{2C_{\text{atten}}(\delta_X + \delta_Y) + \delta_Y\delta_X + C_{\text{totalLSB}}\delta_Y}{2C_{\text{atten}}(C_{\text{totalLSB}} + C_{\text{totalMSB}}) + C_{\text{totalLSB}}C_{\text{totalMSB}} + \Delta C} V_{\text{ref}} \\ &\quad + \frac{\sum_{n=1}^{b_M-1}\sum_{m=1}^{2} D_{n,m}C_{n,m}\delta_X}{2C_{\text{atten}}(C_{\text{totalLSB}} + C_{\text{totalMSB}}) + C_{\text{totalLSB}}C_{\text{totalMSB}} + \Delta C} V_{\text{ref}}, \\ &\delta_X = \sum_{n=1}^{b_L}\sum_{m=1}^{2} D_{n,m}\delta_{n,m}, \qquad \delta_Y = \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} D_{n,m}\delta_{n,m}, \end{aligned} \tag{8}$$

The first and second terms are quite small when compared with the third and fourth terms in the numerator, and the third term ΔC in the denominator does not depend on the bit decision $D_{n,m}$, which only causes a gain error; then they will be neglected. Thus, (8) can be simplified as

$$\text{INL}_{\text{ssc}} \approx \frac{C_{\text{totalLSB}}\delta_Y + \sum_{n=1}^{b_M-1}\sum_{m=1}^{2} D_{n,m}C_{n,m}\delta_X}{2C_{\text{atten}}(C_{\text{totalLSB}} + C_{\text{totalMSB}}) + C_{\text{totalLSB}}C_{\text{totalMSB}}} V_{\text{ref}}, \tag{9}$$

and the variance can be expressed as

$$\begin{aligned} &E\left[\text{INL}_{\text{ssc}}^2\right] \\ &= \frac{C_{\text{totalLSB}}^2(E_{b_{M-1},1} + E_{b_{M-1},2})}{\left[2C_{\text{atten}}(C_{\text{totalLSB}} + C_{\text{totalMSB}}) + C_{\text{totalLSB}}C_{\text{totalMSB}}\right]^2} V_{\text{ref}}^2 \\ &\quad + \frac{\left(\sum_{n=1}^{b_M-1}\sum_{m=1}^{2} D_{n,m}C_{n,m}\right)^2 (E_{b_L,1} + E_{b_L,2})}{\left[2C_{\text{atten}}(C_{\text{totalLSB}} + C_{\text{totalMSB}}) + C_{\text{totalLSB}}C_{\text{totalMSB}}\right]^2} V_{\text{ref}}^2, \end{aligned} \tag{10}$$

$$\begin{aligned} E_{b_{M-1},1} &= E\left[\left(\sum_{n=1}^{b_{M-1}} D_{n,1}\delta_{n,1}\right)^2\right], \\ E_{b_{M-1},2} &= E\left[\left(\sum_{n=1}^{b_{M-1}} D_{n,2}\delta_{n,2}\right)^2\right], \\ E_{b_L,1} &= E\left[\left(\sum_{n=0}^{b_L} D_{n,1}\delta_{n,1}\right)^2\right], \\ E_{b_L,2} &= E\left[\left(\sum_{n=0}^{b_L} D_{n,2}\delta_{n,2}\right)^2\right]. \end{aligned} \tag{11}$$

To simplify the analysis only the worse INL is considered that combines all the errors together (i.e., $D_{n,m} = 1$). For (5) it can be concluded that $E_{bM-1,1} = E_{bM-1,2}$ and $E_{bL,1} = E_{bL,2}$. Thus (10) can be simplified as

$$\begin{aligned} &E\left[\text{INL}_{\text{ssc}}^2\right] \\ &= \frac{\left(2^{b_L}C_0\right)^2\sum_{n=1}^{b_M-1} 2^n\sigma_0^2 + \left(\sum_{n=1}^{b_M-1} 2^{n-1}C_0\right)^2\sum_{n=1}^{b_L} 2^n\sigma_0^2}{\left[C_{\text{atten}}(2^{b_L+1}C_0 + \sum_{n=1}^{b_M-1} 2^nC_0) + 2^{b_L}C_0\sum_{n=1}^{b_M-1} 2^nC_0\right]^2} V_{\text{ref}}^2. \end{aligned} \tag{12}$$

While for the SC array, the $E[\text{INL}_{\text{sc}}^2]$ can be calculated similarly as

$$\begin{aligned} &E\left[\text{INL}_{\text{sc}}^2\right] \\ &= \frac{\left(2^{b_L}C_0\right)^2\sum_{n=1}^{b_M} 2^{n-1}\sigma_0^2}{\left[C_{\text{atten}}(2^{b_L}C_0 + \sum_{n=1}^{b_M} 2^{n-1}C_0) + 2^{b_L}C_0\sum_{n=1}^{b_M} 2^{n-1}C_0\right]^2} V_{\text{ref}}^2 \\ &\quad + \frac{\left(\sum_{n=1}^{b_M} 2^{n-1}C_0\right)^2\sum_{n=1}^{b_L} 2^{n-1}\sigma_0^2}{\left[C_{\text{atten}}(2^{b_L}C_0 + \sum_{n=1}^{b_M} 2^{n-1}C_0) + 2^{b_L}C_0\sum_{n=1}^{b_M} 2^{n-1}C_0\right]^2} V_{\text{ref}}^2. \end{aligned} \tag{13}$$

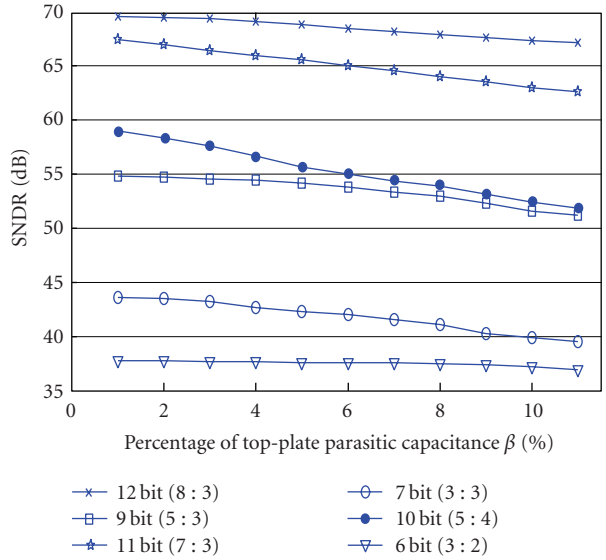

Figure 6: Behavioral simulation of 1000 Monte Carlo SNDR versus the percentage of the top-plate parasitic capacitance β of series-split capacitor array at 6- to 12-bit level.

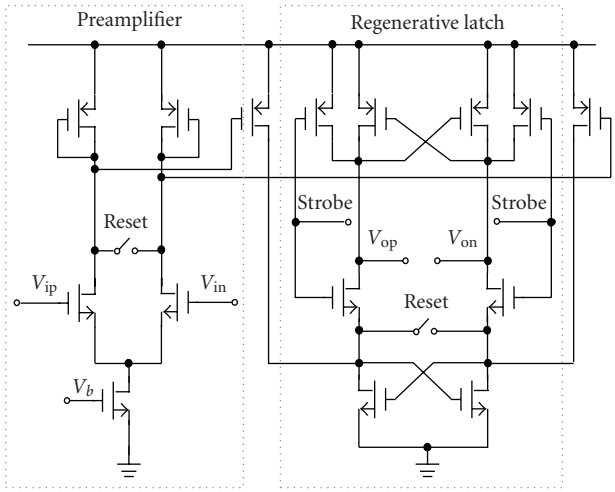

Figure 7: Circuit schematic of the dynamic comparator.

Then, subtracting (12) from (13), its value will become

$$E\left[\mathrm{INL}_{\mathrm{sc}}^2\right] - E\left[\mathrm{INL}_{\mathrm{ssc}}^2\right] \approx \frac{\left(2^{b_L}C_0\right)^2\sigma_0^2 + \left(\sum_{n=1}^{b_{M-1}} 2^n C_0\right)^2 \sum_{n=1}^{b_L} 2^{n-2}\sigma_0^2}{\left[C_{\mathrm{atten}}\left(2^{b_L}C_0 + \sum_{n=1}^{b_M} 2^{n-1}C_0\right) + 2^{b_L}C_0 \sum_{n=1}^{b_M} 2^{n-1}C_0\right]^2} > 0. \tag{14}$$

As a result of (14), the INL of the SSC array should be lower than the SC array which is different from the BWC and BWSC arrays that were already proven to have no difference between the INLs [1].

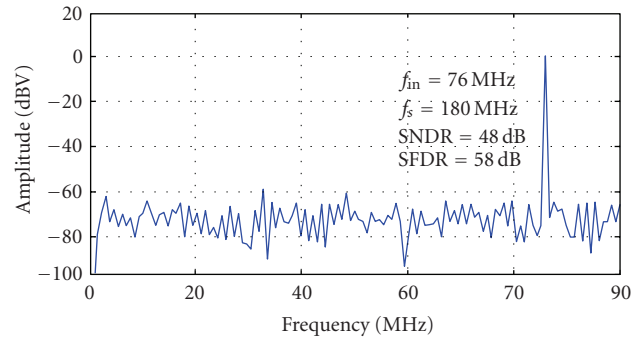

Figure 8: Simulated FFT spectrum of the ADC.

The maximum DNL for the SSC array is expected to occur at the step below the MSB transition [1], and the two output voltages can be calculated as

$$V_{\mathrm{err}}(X) \approx \frac{C_{\mathrm{totalLSB}} \sum_{n=1}^{b_{M-1}} \delta_n + \sum_{n=1}^{b_{M-1}} 2^{n-1}C_0 \sum_{n=1}^{b_L} \sum_{m=1}^{2} \delta_{n,m}}{2C_{\mathrm{atten}}\left(C_{\mathrm{totalLSB}} + C_{\mathrm{totalMSB}}\right) + C_{\mathrm{totalLSB}}C_{\mathrm{totalMSB}}} V_{\mathrm{ref}}, \tag{15}$$

$$V_{\mathrm{err}}(X-1) \approx \frac{C_{\mathrm{totalLSB}} \sum_{n=1}^{b_M-2} \sum_{m=1}^{2} \delta_{n,m}}{2C_{\mathrm{atten}}\left(C_{\mathrm{totalLSB}} + C_{\mathrm{totalMSB}}\right) + C_{\mathrm{totalLSB}}C_{\mathrm{totalMSB}}} V_{\mathrm{ref}} + \frac{\sum_{n=1}^{b_M-2} 2^n C_0 \sum_{n=1}^{b_L} \sum_{m=1}^{2} \delta_{n,m}}{2C_{\mathrm{atten}}\left(C_{\mathrm{totalLSB}} + C_{\mathrm{totalMSB}}\right) + C_{\mathrm{totalLSB}}C_{\mathrm{totalMSB}}} V_{\mathrm{ref}}, \tag{16}$$

subtracting (16) from (15), they will yield

$$\mathrm{DNL}_{\mathrm{ssc}} = \frac{2^{b_L+1}C_0\left(\delta_{b_{M-1}} - \sum_{n=1}^{b_M-2} \delta_{n,2}\right) + C_0 \sum_{n=1}^{b_L} \sum_{m=1}^{2} \delta_{n,m}}{2C_{\mathrm{atten}}\left(C_{\mathrm{totalLSB}} + C_{\mathrm{totalMSB}}\right) + C_{\mathrm{totalLSB}}C_{\mathrm{totalMSB}}} V_{\mathrm{ref}}^2 \tag{17}$$

with variance

$$E\left[\mathrm{DNL}_{\mathrm{ssc}}^2\right] = \frac{\left(2^{b_L}C_0\right)^2\left(2^{b_M-2}\sigma_0^2 - \sum_{n=1}^{b_M-2} 2^{n-1}\sigma_0^2\right)}{\left[C_{\mathrm{atten}}\left(2^{b_L+1}C_0 + \sum_{n=1}^{b_M-1} 2^n C_0\right) + 2^{b_L}C_0 \sum_{n=1}^{b_M-1} 2^n C_0\right]^2} V_{\mathrm{ref}}^2 + \frac{C_0 \sum_{n=1}^{b_L} 2^{n-1}\sigma_0^2}{\left[C_{\mathrm{atten}}\left(2^{b_L+1}C_0 + \sum_{n=1}^{b_M-1} 2^n C_0\right) + 2^{b_L}C_0 \sum_{n=1}^{b_M-1} 2^n C_0\right]^2} V_{\mathrm{ref}}^2 = \frac{\left[\left(2^{b_L}C_0\right)^2 + 2C_0 \sum_{n=1}^{b_L} 2^{n-1}\right]\sigma_0^2}{2\left[C_{\mathrm{atten}}\left(2^{b_L+1}C_0 + \sum_{n=1}^{b_M-1} 2^n C_0\right) + 2^{b_L}C_0 \sum_{n=1}^{b_M-1} 2^n C_0\right]^2} V_{\mathrm{ref}}^2. \tag{18}$$

For SC array the $E[\mathrm{DNL}_{\mathrm{sc}}^2]$ can be calculated similarly as

$$E\left[\mathrm{DNL}_{\mathrm{sc}}^2\right] = \frac{\left[\left(2^{b_L}C_0\right)^2 + C_0\sum_{n=1}^{b_L}2^{n-1}\right]\sigma_0^2}{\left[C_{\mathrm{atten}}\left(2^{b_L}C_0+\sum_{n=1}^{b_M}2^{n-1}C_0\right)+2^{b_L}C_0\sum_{n=1}^{b_M}2^{n-1}C_0\right]^2}V_{\mathrm{ref}}^2; \tag{19}$$

thus, $E[\mathrm{DNL}_{\mathrm{sc}}^2]/\ E[\mathrm{DNL}_{\mathrm{ssc}}^2]$ can be expressed as

$$\frac{E\left[\mathrm{DNL}_{\mathrm{ssc}}^2\right]}{E\left[\mathrm{DNL}_{\mathrm{sc}}^2\right]} \approx \frac{\left(2^{b_L}C_0\right)^2 + 2C_0\sum_{n=1}^{b_L}2^{n-1}}{2\left[\left(2^{b_L}C_0\right)^2 + C_0\sum_{n=1}^{b_L}2^{n-1}\right]} < 1. \tag{20}$$

Thus, from (20) it can be concluded that the maximum DNL of the SSC is also lower than that of the SC array.

3.4. Parasitic Nonlinearity Effect. One potential issue with these two series capacitor array structures (SSC and SC) is the parasitic capacitances C_{p1} and C_{p2} on the nodes A and B, which will deteriorate the desired voltage division ratio and result in poor linearity. The parasitic effect is caused by the bottom- and top-plate parasitic capacitance of C_{atten} as well as the top-plate parasitic capacitance of MSB and LSB array capacitors which can be calculated as

$$\begin{aligned} C_{p1} &= \alpha\cdot C_{\mathrm{atten}} + \beta\cdot C_{\mathrm{sumMSB}},\\ C_{p2} &= \beta\cdot C_{\mathrm{atten}} + \beta\cdot C_{\mathrm{sumLSB}}, \end{aligned} \tag{21}$$

where α and β represent the percentage of bottom- and top-plate parasitic capacitances of each capacitor, respectively (with metal-isolator-metal (MIM) capacitor option, α = 10%, β = 5%). For the SSC array, the analog output $V_{\mathrm{out}}(X)$ with C_{p1} and C_{p2} taken in to account can be calculated as

$$\begin{aligned} V_{\mathrm{out}}(X) &= \frac{C_{\mathrm{atten}}\left(\sum_{n=1}^{b_L}\sum_{n'=1}^{2}D_{n,n'}2^{n-1}C_0+\sum_{n=1}^{b_M}\sum_{b'=1}^{2}D_{n,n'}2^{n-1}C_0\right)}{C_{\mathrm{atten}}\left(C_{\mathrm{sumLSB}}+C_{\mathrm{sumMSB}}+C_{p1}+C_{p2}\right)+\mathfrak{D}}V_{\mathrm{ref}}\\ &\quad+\frac{\left(C_{\mathrm{sumLSB}}+C_{p2}\right)\sum_{n=1}^{b_M}\sum_{n'=1}^{2}D_{n,n'}2^{n-1}C_0}{C_{\mathrm{atten}}\left(C_{\mathrm{sumLSB}}+C_{\mathrm{sumMSB}}+C_{p1}+C_{p2}\right)+\mathfrak{D}}V_{\mathrm{ref}}, \end{aligned} \tag{22}$$

where $\mathfrak{D}$ denotes $(C_{\mathrm{sumLSB}} + C_{p2})(C_{\mathrm{sumMSB}} + C_{p1})$. This equation shows that the parasitic capacitances C_{p1} and C_{p2} in the denominator are completely uncorrelated in the bit decisions, which can cause only a gain error and have no effect into the linearity performance. However, the parasitic capacitance C_{p2} in the numerator contributes with a code-dependent error, which degrades the linearity of the SAR ADC. Subtracting the nominal value the error term will become

$$\begin{aligned} V_{\mathrm{error}}(X) &= \frac{C_{p2}\sum_{n=1}^{b_M}\sum_{n'=1}^{2}D_{n,n'}2^{n-1}C_0}{C_{\mathrm{atten}}\left(C_{\mathrm{sumLSB}}+C_{\mathrm{sumMSB}}+C_{p1}+C_{p2}\right)+\mathfrak{D}}V_{\mathrm{ref}}. \end{aligned} \tag{23}$$

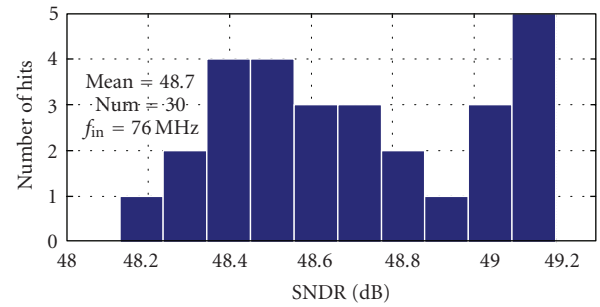

Figure 9: 30-times Monte Carlo simulation of SNDR from the 8 b SAR.

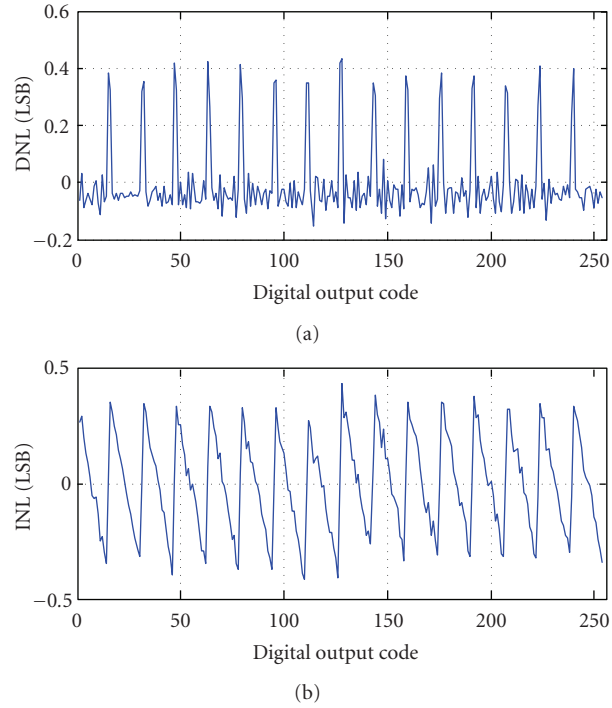

Figure 10: Simulated linearity: (a) DNL and (b) INL.

The parasitic capacitance C_{p2} is composed of the parasitic capacitance of C_{atten} and C_{sumLSB}. By reducing the number of bits in the LSB array, the size of C_{sumLSB} can be minimized; thus the nonlinearity effect can be alleviated. But, this will enlarge the capacitor spread in the MSB array; thus the distribution of bits in both MSB and LSB arrays should consider the trade-off between linearity, tolerance, and capacitance spread limitations.

3.5. Behavioral Simulations. Four behavioral simulations of the SSC and the SC array DAC were performed to verify the previous analysis. The values of the unit and attenuation capacitors used are Gaussian random variables with standard deviation of 1% (σ_0/C_0 = 0.01), and the ADC is otherwise ideal. Figure 3 shows the result of 10000-time Monte Carlo runs, where the standard deviation of DNL and INL is plotted versus output code at the 8-bit level. As expected,

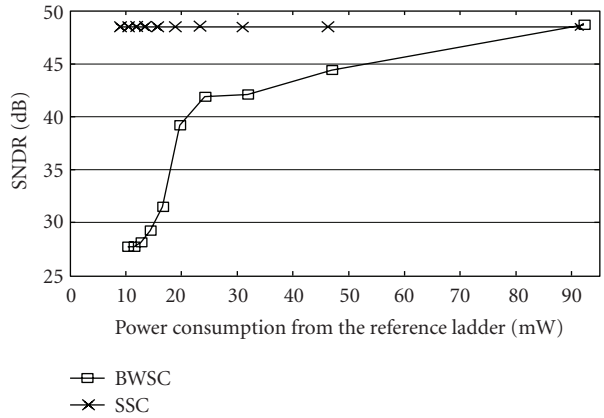

Figure 11: Simulated SNDR versus power consumption from the reference ladder for series-split (SSC) and binary-weighted split-capacitor array (BWSC).

the SSC array has better INL and DNL than its SC array counterpart. Figure 4 shows the result of 1000 Monte Carlo runs with 5% top-plate and 10% bottom-plate parasitic capacitances, where the SNDRs are plotted versus different distribution of bits in the MSB and LSB array at the 8-bit level. Comparing the SNDR shown in Figure 4, and as expected, a larger number of bits in the LSB array will cause poor linearity. Although MSB : LSB = 5 : 2 can achieve the best SNDR, since larger capacitor ratios will both reduce the conversion speed and increase the power dissipation, MSB : LSB = 4 : 3 will be adopted for circuit implementation due to both good linearity performance and smaller capacitor ratios. Figure 5 illustrates the result of 1000-time Monte Carlo runs, where the SNDRs are plotted versus the percentage of the top-plate parasitic capacitance β for the SSC array structure for an 8-bit ADC. With C_{p2} increasing, the parasitic capacitance will decrease the SNDR of the conversion performance. But with approximate ±5% variance of β a good linearity performance of an SAR ADC can still be achieved. Figure 6 illustrates the result of 1000 Monte Carlo runs, where the SNDRs are plotted versus the percentage of the top-plate parasitic capacitance β at the 6- to 12-bit level with proper bits distribution of the LSB and MSB arrays. From it we can find that the parasitic nonlinearity effect is insignificant; thus the series split structure can also be utilized in high-resolution applications.

3.6. Power Consumption Analysis. The power consumption of the SAR converter is dominated by the DAC capacitor array, the comparator, and the switches' drivers. The array's power is proportional to the sum of the array total capacitance C_{total} of which the bottom-plate is connected to the reference voltage supply and can be calculated as

$$P_{\text{array}} = C_{\text{total}} V_{\text{ref}} V_{\text{FS}} \tag{24}$$

where V_{FS} is the full-scale input voltage, assuming that V_{FS} has been fully sampled on to the capacitor array and the charge is all supplied by the reference voltage V_{ref} [1]. In a 8-bit case, the C_{total} of the proposed structure is $46C_0$ (with MSB : LSB = 4 : 3), but for a binary-weighted capacitor array the C_{total} is $256C_0$, which can consume 5 times more power than the proposed structure. The series combination allows a significant reduction of the largest capacitor ratio; in an 8-bit case, the largest capacitor C_{max} of the series split and binary-weighted split capacitor array structure is $8C_0$ and $64C_0$, respectively, which decreases the DAC settling time and speeds up the conversion. The total input capacitance of the proposed structure is not completely dependent on the number of bits of the ADC and can be calculated as

$$C_{\text{in}} = C_{\text{sumMSB}} + 2C_0. \tag{25}$$

The power consumptions of the comparator and switch drivers are also proportional to the equivalent input capacitance C_{in}. Therefore, the smaller C_{total}, C_{max}, and C_{in} it will imply an increase in efficiency of the overall conversion performance.

Table 1: Performance Summary of the SAR ADC.

Technology	90-nm CMOS with MIM
Resolution	8 bit
Sampling Rate	180 MS/s
Supply Voltage	1.2 V
Full Scale Analog Input	1.2 Vpp differential
SNDR ($@f_{\text{in}} = 76$ MHz)	48 dB
SFDR ($@f_{\text{in}} = 76$ MHz)	58 dB
ENOB ($@f_{\text{in}} = 76$ MHz)	7.7 bit
FOM	0.37 pJ/conversion step
DNL	±0.5 LSB
INL	±0.5 LSB
Power Consumption	
Analog	9.4 mW
Digital	2.3 mW
Reference ladder	2.3 mW
Total	14 mW

4. Circuit Implementation Details

A high-speed SAR converter imposes a stringent requirement in the clock generation; for example, an 8 b 180 MS/s SAR ADC requires an internal master clock of over 1.62 GHz. To generate such a high-frequency clock pulse the generator will consume even more power than the ADC itself. Due to the power limitations of the clock generator in a synchronous SA design an asynchronous SAR processing technique [4] will be adopted here, where only a master clock of 180 MHz is required.

The dynamic comparator [6] used in this ADC is shown in Figure 7 and it is composed of a preamplifier and a regenerative latch. The preamplifier can provide sufficient gain to suppress the relatively high input referred offset voltage of the latch. Also, the kickback noise of the latch can be isolated by the current mirror between the two stages. The dynamic operation of this circuit is divided into a reset phase and a regeneration phase. During the reset phase the

two outputs (V_{op} and V_{on}) are pulled up to V_{DD}. After the input stage has settled, the voltage difference is then amplified to a full swing during the regeneration phase. The differential output can generate a data ready signal to indicate the completion of the comparison, which will be used to trigger a sequence of shift registers and the switch drivers to perform asynchronous conversion [4]. Dynamic logic circuits are also utilized instead of traditional static logic to release the limitation of digital feedback propagation delay in the SA loop.

5. Simulation of an 8-Bit 180 MS/s SAR ADC

To verify the proposed capacitor structure of the capacitive DAC, a 1.2 V, 8 b, 180-MS/s SAR ADC was designed using a 90 nm CMOS process with metal-isolator-metal (MIM) capacitor option. The SAR ADC was implemented in a fully differential architecture, with a full scale differential input range of 1.2 V_{PP}. Considering the parasitic capacitance of the attenuation capacitors that will reduce the linearity of the ADC, 5% top-plate and 10% bottom-plate, they were included in the simulations according to the data from the foundry datasheet.

Figure 8 shows a spectrum plot of the SAR ADC after a Monte Carlo simulation with an input signal of 76 MHz leading to an SNDR of 48 dB, which clearly demonstrates the tolerance to the parasitic effect caused by the C_{p2}. Figure 9 also shows the corresponding 30-times Monte Carlo mismatch simulations where the ADC achieves a mean SNDR of 49 dB with an input signal of 76 MHz. The DNL and INL are both within ±0.5 LSB as shown in Figure 10. Figure 11 shows the SNDR versus power consumption from the reference ladder in the proposed architecture, as well as in the BWSC array structure, clearly demonstrating that the BWSC results are poor in terms of SNDR mainly due to the large RC settling time. To reach the same conversion performance the BWSC array consumes 10 times more power than the proposed structure. Table 1 summarizes the overall performance of the SAR ADC with the total power consumption of 14 mW only and an FoM of 0.37 pJ/conversion-step, distinctly proving the low power dissipation feature of the proposed technique.

6. Conclusions

A novel series-split capacitive DAC technique has been proposed which can both implement an efficient charge recycling SAR operation and achieve a small input capacitance. The reduction of the maximum ratio and sum of the total capacitance can lead to area savings and power efficiency, which allow the SAR converter to work at high speed while meeting a low power consumption requirement. Theoretical analysis and behavioral simulations of the linearity performance demonstrate that the proposed SSC structure can have a better INL and DNL than the traditional SC array structure. Simulation results of a 1.2 V, 8 b, 180-MS/s SAR ADC were presented exhibiting an SNDR of 48 dB at a 76 MHz input with the total power consumption of 14 mW that certifies the power efficiency of the novel circuit structure.

Acknowledgments

This work was financially supported by research grants from the University of Macau and FDCT with Ref nos. RG-UL/07-08S/Y1/MR01/FST and FDCT/009/2007/A1.

References

[1] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 739–747, 2007.

[2] D. Draxelmayr, "A 6b 600 MHz 10 mW ADC array in digital 90 nm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference (ISSCC '04)*, vol. 1, pp. 264–265, February 2004.

[3] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISSCAS '05)*, pp. 184–187, 2005.

[4] M. S. W. Chen and R. W. Brodersen, "A 6b 600 MS/s 5.3 mW asynchronous ADC in 0.13 μm CMOS," in *Proceedings of IEEE International Solid-State Circuits Conference (ISSCC '06)*, pp. 574–575, February 2006.

[5] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, John Wiley & Sons, New York, NY, USA, 2nd edition, 2004.

[6] G. M. Yin, F. Eynde, and W. Sansen, "A high-speed CMOS comparator with 8-b resolution," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 208–211, 1992.