A Rapid Power-Switchable Track-and-Hold Amplifier in 90-nm CMOS

He-Gong Wei, U-Fat Chio, Yan Zhu, *Student Member, IEEE*, Sai-Weng Sin, *Member, IEEE*, Seng-Pan U, *Senior Member, IEEE*, and R. P. Martins, *Fellow, IEEE*

***Abstract*—This brief presents the design and implementation of a high-speed and high-accuracy power-switchable track-and-hold (T/H) in 90-nm CMOS that achieves a total harmonic distortion of −60 dB at 100 MS/s. With the proposed power-switching (P-S) technique, the T/H amplifier obtains not only further power optimization but also enhanced sampling speed and accuracy. The P-S technique requires no extra voltage headroom in the source-follower amplifier, thus allowing a relatively large input voltage swing of 0.8-V_{PP} in differential mode. A spurious-free dynamic range of 70 dB at 100 MS/s was measured with an input of 40.6 MHz and 0.8 V_{PP}. While driving a 2.5-pF capacitive load, the T/H consumes 2.97 mW from the 1.2-V supply.**

***Index Terms*—High-accuracy, high-speed, power switchable, track-and-hold (T/H).**

I. Introduction

SINCE all naturally produced signals received or sent by humans are analog, the data conversion interface, which is composed of sampling circuits and analog-to-digital converters (ADCs) or digital-to-analog converters, is irreplaceable and highly demanded by different types of advanced applications in medical imaging, instrumentation, communication, and consumer electronics, because it provides the appropriate link between the analog world and the fast-evolving realm of comprehensive digital systems.

Prior to the ADC, the analog input signal must be sampled and kept constant while the conversion takes place [1], and with state-of-the-art requirements of high speed and high resolution, these impose very stringent characteristics in the sample-and-hold front-end circuit, which is the key element of the whole system dominating the overall ADC's precision. A source-follower (SF)-based track-and-hold (T/H) circuit, which is often required in most front ends, plays a significant role in the ADC designs, particularly high-frequency applications. The T/H circuit greatly improves the dynamic performance at high frequency by reducing the pedestal error without sacrificing the system's speed and linearity. During the hold phase, the analog input must be kept unchanged, and various types of dynamic errors can be suppressed, such as aperture jitter, skews in clock delivery, limited input bandwidth prior to latch generation, and signal-dependent dynamic nonlinearity [2]. Distortion introduced by timing uncertainties at high frequency can be avoided in this way, and only a single switch in the sample-and-hold circuit determines the timing accuracy. In addition, the performance of the T/H could further be improved by clock bootstrapping techniques [3], [4].

With CMOS technology, downscaling of the conversion speed of the ADC has rapidly been developing, implying that the T/H has to process input signals at increasingly higher speed. Thus, in order to guarantee the accuracy of the T/H at such high speed of operation, a larger bandwidth becomes necessary, leading, on the other hand, to significant power dissipation, which might become the dominant factor in the whole ADC power consumption. In this brief, a power-switchable high-speed high-accuracy T/H amplifier will be presented. The proposed power-switching (P-S) technique provides a rapid switching operation in order to avoid the static power dissipation of the T/H without degrading the output voltage swing. Meanwhile, by using the technique, the tracking speed and accuracy of the T/H are enhanced as well [5].

II. Power-Switchable T/H Amplifier

Although the open-loop T/H can provide a reliable solution to sample the input signal at high speed with high accuracy, it exhibits a main drawback related with its large static power consumption in the SF. On the other hand, a power-switchable T/H is expected to avoid drawing static power when the T/H is at rest, which can imply large power savings for applications where the T/H's working time frame is much smaller than the whole period, e.g., in the cases of two-step or power-scalable ADCs.

A. Traditional Power-Switchable T/H

In a traditional power-switchable T/H, as presented in Fig. 1(a), the sampling phase and P-S phase have fixed power-on phase but variable period [6]. When the period is extended, the ratio between the power-on phase and the whole conversion period T is reduced, and power saving can be achieved. This solution introduces a switched SF (with a series switch) in the T/H, where Φ_{PD} is the P-S phase and Φ_S is the sampling phase. When the switch S_{PD} is open, the dc current in the SF will be cut off, and the static power consumption is avoided. Moreover, the parasitic capacitance around S_{PD} is relatively small, so the T/H can switch very fast.

Manuscript received April 30, 2009; revised July 29, 2009. First published January 8, 2010; current version published January 15, 2010. This work was supported by research grants from the University of Macau and FDCT under Reference UL013A/08-Y2/EEE/MR01/FST and Reference FDCT/009/2007/A1. This paper was recommended by Associate Editor J. Li.

H.-G. Wei, U.-F. Chio, Y. Zhu, S.-W. Sin, and S.-P. U are with the Analog and Mixed-Signal VLSI Laboratory, Faculty of Science and Technology, University of Macau, Macao, China (e-mail: weihegong@ieee.org).

R. P. Martins is with the Analog and Mixed-Signal VLSI Laboratory, Faculty of Science and Technology, University of Macau, Macao, China, and also with the Instituto Superior Técnico, Technical University of Lisbon, 1049-001 Lisbon, Portugal (e-mail: rmartins@umac.mo).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2009.2037260

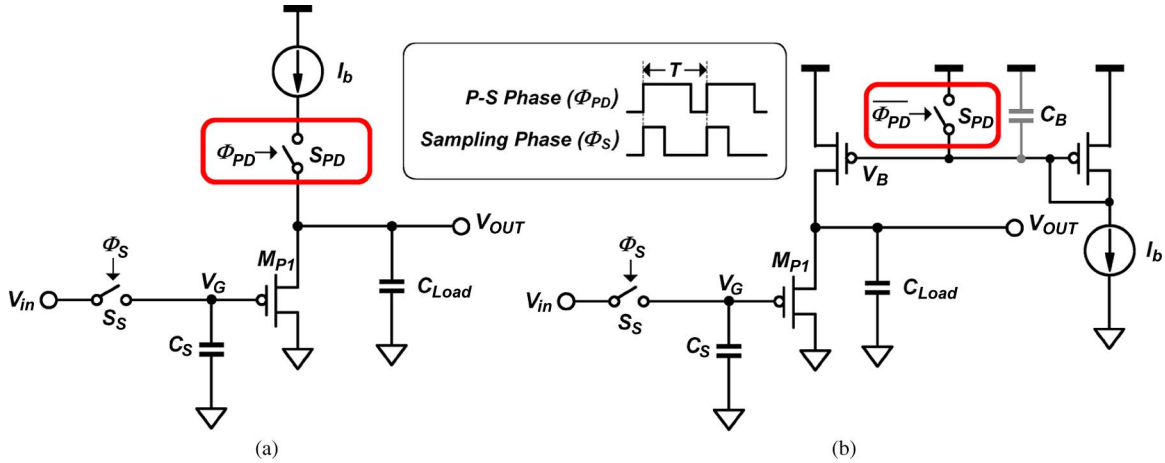

Fig. 1. (a) Traditional power-switchable T/H overall principle with basic circuit structure and (b) alternative circuit.

However, the P-S technique presented in Fig. 1(a) exhibits a major drawback since the voltage drop at $S_{\rm PD}$ can become large, leading to a limited output voltage swing when the dc current is large in very high speed applications. For a large input swing, a significant amount of distortion will be induced by M_{P1}, and the linearity of the T/H will seriously be degraded. This disadvantage becomes even more prominent with nano-CMOS technology, in the presence of lower supply voltage.

Another alternative P-S solution is shown in Fig. 1(b), where the power control switch $S_{\rm PD}$ is added between the biasing point of the SF's current source and the power supply. Then, the switch will not consume any voltage swing or induce any distortion into the SF. However, this P-S method can only be applied in low-speed applications, because, to secure the biasing point of the current source, a large parasitic capacitance is usually necessary (or a large decoupling capacitance C_B) to stabilize the bias voltage. Then, the switching operation limited by the charging/discharging speed of C_B will be quite slow.

B. Proposed Power-Switchable T/H

In order to simultaneously have a rapid P-S operation and a large output swing, a new circuit structure is proposed in Fig. 2(a). The highlighted P-S control switch is added between the gate of M_{P1} and the power supply. When $S_{\rm PD1}$ closes, the gate of M_{P1} will be pulled up to the supply. Then, M_{P1} falls into the cutoff region, and the dc current in the SF stops flowing. When $S_{\rm PD1}$ is open, the gate of M_{P1} is connected to the input. Since there is no series-connected switch in the SF, this implies that the voltage swing will not be reduced. On the other hand, the parasitic capacitance at the gate of M_{P1} is not as high as C_B [from Fig. 1(b)]; thus, a high switching speed can be achieved.

During powerdown, $S_{\rm PD1}$ will also pull up the top plate of the sampling capacitor C_S, thus degrading the speed. To alleviate this problem, a further improved solution can be adopted, as shown in Fig. 2(a), with one more power control switch $S_{\rm PD2}$, which is added between C_S and the ground. When $\Phi_{\rm PD}$ is reset, C_S will then float, and the speed of the powerdown transient can be improved since C_S does not need to be discharged.

The design of the proposed T/H also includes linearity-improving elements, such as the bootstrapping network. In addition, a unity-gain buffer is inserted between the input and the bulk of the SF to enhance the output's accuracy and speed.

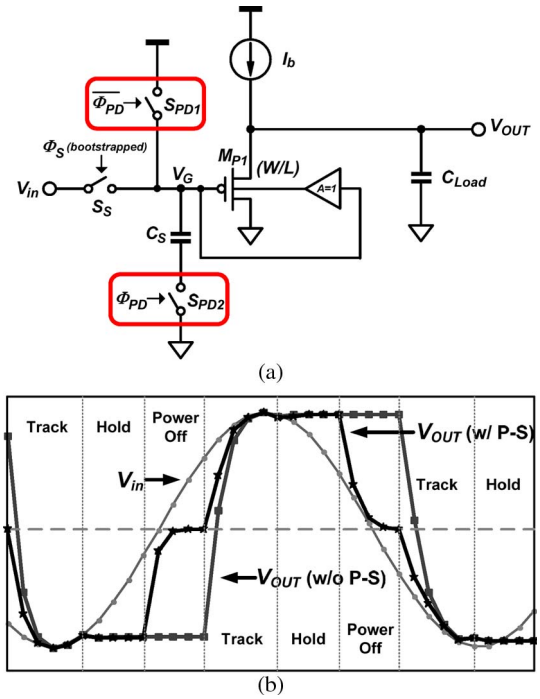

Fig. 2. Proposed P-S T/H amplifier. (a) Circuit implementation and (b) output transient with or without the P-S circuit.

The unity-gain buffer can be implemented by a replica branch [7], which is a scaled-down version of the main SF.

With the P-S operation, the output of the T/H is reset every duty cycle. Originally, as shown in Fig. 2(b), tracking the input implies a significant time if the two sampled values of $V_{\rm IN}$ have a large voltage difference, which can be, in the worst case, equal to a full-scale input swing. However, when the proposed P-S method is applied, the differential voltages of V_G and $V_{\rm OUT}$ are reset to zero in each clock cycle. Thus, the output voltage varies from zero to $V_{\rm IN}$ after every period, implying that the maximum change in the output voltage will be half of the full input swing, and therefore, the tracking time can be reduced.

III. Mathematical Analysis and Simulated Transient Response

As previously presented, the settling time of the T/H's output is reduced when the T/H is designed to be reset every cycle,

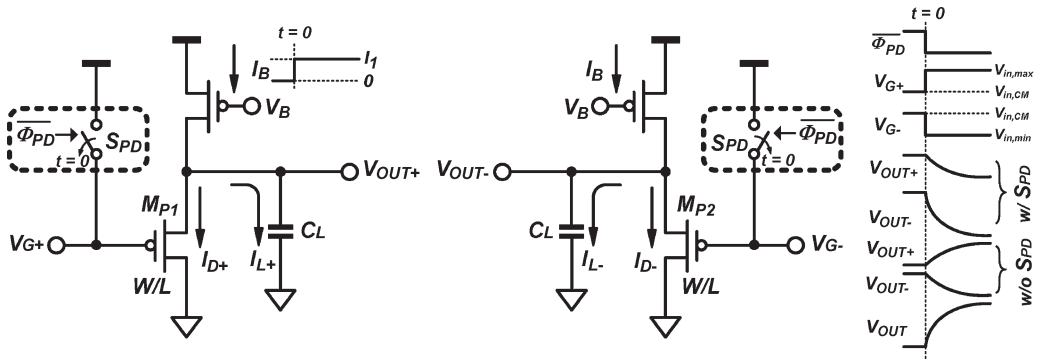

Fig. 3. Simplified T/H circuit diagram used in the mathematical analysis.

which is inherited by the P-S operation. It is also interesting to notice that, by applying the proposed P-S technique, the SF buffer is able to provide a large charging/discharging current (differentially) through the load capacitor, leading to an even faster settling speed of the output, when compared to the traditional nonpower-switched designs. In this section, a mathematical model of the output voltage will be derived, together with the performance comparison between a normal T/H and the proposed power-switchable T/H circuit. Since the speed limitation of the T/H is mainly derived from the driving ability of the SF (buffer), whereas the input switched-capacitor sampler could achieve a very small *RC* time constant, the following speed analysis of the T/H will only focus on the SF, and the input switched capacitor will not be considered for simplicity. Subsequently, the simplified circuit diagram used in the mathematical analysis is shown in Fig. 3, where the gate of the T/H V_{G+} (or V_{G-}) is supplied by a step input ranging from the input common-mode voltage to the maximum (or minimum, respectively) of the input swing. Before the analysis, some assumptions are necessary and listed here.

1) Although the current source is pulled up to V_{DD} in the power-off phase providing negligible current, it will rapidly settle to its normal value when the T/H is powered on. Since the biasing current will settle to its normal value I_1 much faster than the settling of the SF composed by M_{P1} and M_{P2} (which will be proven next), the current I_B is modeled as a step from zero to I_1, triggering at $t = 0$, as shown in Fig. 3.
2) Although the parasitic capacitance slows down the speed of the T/H, the speed limitation usually originates from the settling of C_L. In the following analysis, the parasitic capacitances, such as C_{gs} and C_{gd}, are not included, because their charging speed is much faster than that associated with the load capacitor C_L (which is equal to 2.5 pF in the implementation shown next). This is especially valid in nano-CMOS with dramatically reduced SF parasitics.

Based on the preceding assumptions, the drain current of the SF in the positive side of the T/H can be derived as

$$I_{D+} = k(V_{\mathrm{OUT}+} - V_{G+} - V_{\mathrm{TH}})^2 \tag{1}$$

where $k = \mu_p C_{\mathrm{ox}}(W/L)/2$, and V_{G+} is the gate voltage that remains the same after $t = 0$ and can be treated as a constant. As shown in Fig. 3, S_{PD} opens at $t = 0$, and the T/H enters into the track phase. The load current flowing through C_L can be expressed as

$$I_{L+} = I_1 - k(V_{\mathrm{OUT}+} - V_{G+} - V_{\mathrm{TH}})^2 = C_L \frac{dV_{\mathrm{OUT}+}}{dt}. \tag{2}$$

With the initial condition at $V_{\mathrm{OUT}+}(t = 0)$, the differential equation (2) can be solved as

$$V_{\mathrm{OUT}+}(t) = V_{G+} + V_{\mathrm{TH}} + \sqrt{\frac{I_1}{k}} \times \tanh\left[\frac{t}{C_L}\sqrt{kI_1} + \frac{1}{2}\ln\left(-1 + \frac{2\sqrt{I_1/k}}{V_{G+} + V_{\mathrm{TH}} + \sqrt{I_1/k} - V_{\mathrm{OUT}+}(0)}\right)\right]. \tag{3-a}$$

Similarly, the output at the negative side can be derived as

$$V_{\mathrm{OUT}-}(t) = V_{G-} + V_{\mathrm{TH}} + \sqrt{\frac{I_1}{k}} \times \tanh\left[\frac{t}{C_L}\sqrt{kI_1} + \frac{1}{2}\ln\left(-1 + \frac{2\sqrt{I_1/k}}{V_{G-} + V_{\mathrm{TH}} + \sqrt{I_1/k} - V_{\mathrm{OUT}-}(0)}\right)\right]. \tag{3-b}$$

Then, the differential output of the T/H can be found from

$$V_{\mathrm{OUT}} = V_{\mathrm{OUT}+} - V_{\mathrm{OUT}-}. \tag{4}$$

In addition, because the initial conditions $V_{\mathrm{OUT}+}(0)$ and $V_{\mathrm{OUT}-}(0)$ are equal to the voltage supply if the proposed P-S technique is applied (the output will be pulled up to supply during the power-off phase), the transistor M_{P1} and M_{P2} will be in the saturation region at $t = 0$ due to the large value of source–drain voltage in the presence of sufficient source–gate voltage drop.

In order to compare settling speeds, the traditional design with non-P-S T/H can also be analyzed, which is described by (4) but with different values of $V_{\mathrm{OUT}+}(0)$ and $V_{\mathrm{OUT}-}(0)$. However, one exception needs to be considered at the positive side of the T/H output voltage, which imposes that (1) cannot hold under the circumstances of non-P-S. The initial condition $V_{\mathrm{OUT}+}(0)$ and $V_{\mathrm{OUT}-}(0)$ will be equal to the output common-mode voltage that is close to half the voltage supply. When V_{G+} receives a positive step at $t = 0$, the source–gate voltage suddenly becomes very small or even negative, and the transistor

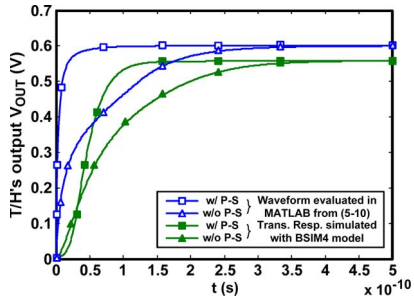

Fig. 4. T/H's output voltage comparison with and without the proposed P-S.

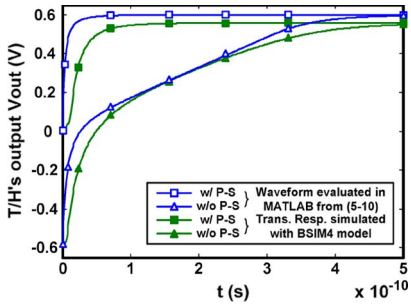

Fig. 5. T/H's output comparison with and without the proposed P-S with a maximum step input.

M_{P1} will not be saturated as in (1) but, on the contrary, will be cut off. Then, the load C_L will be charged by the current source only, and (1), as well as (3-a), will no longer hold. In this case, the load current I_{L+} is given by

$$I_{L+} = C_L \frac{dV_{\mathrm{OUT}+}}{dt} = I_1. \tag{5}$$

Since, I_1 is constant, $V_{\mathrm{OUT}+}$ can be calculated as

$$V_{\mathrm{OUT}+} = \frac{I_1}{C_L} t + V_{\mathrm{OUT}+}(0). \tag{6}$$

Then, C_L will linearly be charged, and $V_{\mathrm{OUT}+}$ increases, as described in (6), until $V_{\mathrm{OUT}+} - V_{G+} > V_{\mathrm{TH}}$ at $t = t_1$. After t_1, M_{P1} will enter the saturation region, and $V_{\mathrm{OUT}+}$ can be expressed as (2). With the initial condition $V_{\mathrm{OUT}+}(t_1)$ at $t = t_1$, $V_{\mathrm{OUT}+}$ can be obtained as

$$V_{\mathrm{OUT}+}(t) = V_{G+} + V_{\mathrm{TH}} + \sqrt{\frac{I_1}{k}} \times \tanh\left[\frac{t}{C_L}\sqrt{kI_1} - \frac{t_1}{C_L}\sqrt{kI_1} - \tanh^{-1}\left(\frac{V_G + V_{\mathrm{TH}} - V_{\mathrm{OUT}+}(t_1)}{\sqrt{I_1/k}}\right)\right]. \tag{7}$$

Moreover, at the negative side of the T/H, $V_{\mathrm{OUT}-}$ can still be expressed by (3-b) since V_{G-} receives a negative step that provides a large source–gate voltage and M_{P2} is always saturated.

In order to obtain the final quantitative solution of the T/H's output voltage and plot its waveform, based on the formulas, certain values of the parameters need to be established. For a good approximation with the transistor-level simulation, the values are chosen as $k = 0.625$ A/V^2, $I_1 = 4$ mA, $V_{\mathrm{TH}} = 0.2$ V, and $C_L = 2.5$ pF, and the input common-mode voltage injected to the T/H is 0.3 V, with an input voltage amplitude of 0.3 V. Then, in the step responses, V_{G+} varies from 0.3 to 0.6 V, and V_{G-} varies from 0.3 to 0 V. Substituting the values into (3-a)–(7), the waveform of V_{OUT} can be calculated (in MATLAB) and plotted in Fig. 4. Obviously, using the proposed P-S technique, the T/H's output voltage settles faster than that with the traditional nonswitching arrangement. Moreover, the transient response of V_{OUT}, which was obtained by the transistor-level simulation with the BSIM4 model in CADENCE, is also plotted in Fig. 4 and includes all the nonidealities, such as the body effect, channel length modulation, parasitic capacitances such as C_{gs} and C_{gd}, and the real circuit of the current source that provides the transient current (instead of only using the step current I_B modeled in Fig. 3). From Fig. 4, it can be detected that the simulated transient response of V_{OUT} settles slower, because the waveforms obtained from (3-a)–(7) do not consider the parasitic capacitances that slow down the response, but it is still obvious that the curves with P-S settle much faster. The final output voltages of the waveforms evaluated by MATLAB are larger than the simulated ones, because channel length modulation has not been considered when deriving (3-a)–(7).

To strengthen the preceding analysis, another example is illustrated in Fig. 5. In this case, different T/H's input settings are utilized, where the input steps from its minimum to maximum at $t = 0$. Therefore, V_{G+} varies from 0.0 to 0.6 V, V_{G-} varies from 0.6 to 0 V, and other circuit parameters remain the same. The transient response from the transistor simulation has also been provided in Fig. 5 with the same input signal. In this case, the proposed P-S scheme has an even smaller settling time since the output of the T/H is reset before the track phase, as discussed before.

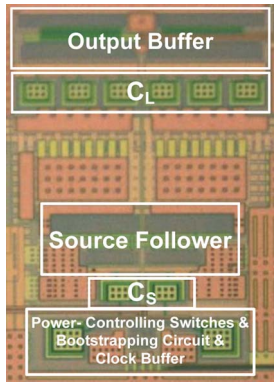

Fig. 6. Chip micrograph of the proposed power-switchable T/H.

IV. Measurement Results

The proposed power-switchable T/H circuit was fabricated in 90-nm CMOS technology, and the test chip includes the complete differential architecture, as presented in Fig. 2(a), as well as a 2.5-V output buffer that was added to drive the pad-ring and off-chip printed circuit board (PCB) loads. In the integrated prototype, a capacitance of 2.5 pF is added in order to test the driving ability of the T/H, and a 500-fF sampling capacitance is implemented in order to achieve 10-b accuracy. The micrograph of the proposed power-switchable T/H is shown in Fig. 6 with an active area of 0.023 mm^2. Several experimental measurements were obtained, leading to the following evaluation: 1) Fig. 7 shows the transient response

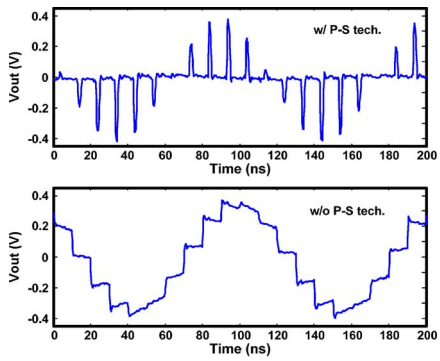

Fig. 7. Measured output waveform at $f_S = 100$ MHz with $f_{\rm in} = 9$ MHz ($V_{\rm in} = 800\ {\rm mV_{pp}}$).

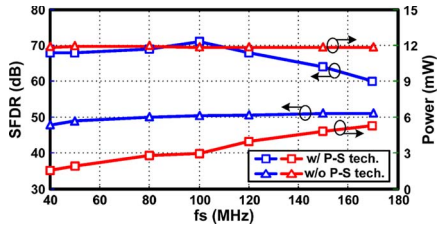

Fig. 8. Measured SFDR and power of the T/H with or without the proposed P-S at different sampling frequencies f_S with $f_{\rm in} = 1.9$ MHz ($V_{\rm in} = 800\ {\rm mV_{pp}}$).

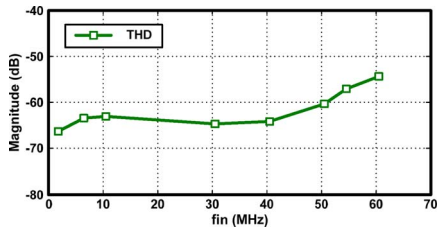

Fig. 9. Measured THD of the proposed power-switchable T/H with different input frequencies at $f_S = 100$ MHz. ($V_{\rm in} = 800\ {\rm mV_{pp}}$).

of the T/H with or without the proposed P-S technique at $f_S = 100$ MHz and with $f_{\rm in} = 9$ MHz. Since the P-S process resets the output of the T/H, its output voltage goes down to zero in every duty cycle, instead of remaining constant. In addition, the output voltage has been normalized to match the input scale (0.8 $V_{\rm pp}$) to compensate the attenuation of the output buffer and PCB testing platform. 2) Fig. 8 plots the measured spurious-free dynamic range (SFDR) and power consumption of the T/H versus the sampling frequency f_S, where the SFDR is more than 68 dB (60 dB) up to $f_S = 120$ MHz (170 MHz), with the track- and power-on phases fixed to 1.5 and 3 ns, respectively.Thus, the power dissipation of the T/H is scaled down for lower values of the sampling frequency. The proposed P-S T/H simultaneously exhibits better linearity and lower power consumption, confirming prior deductions. 3) Fig. 9 illustrates the measured total harmonic distortion (THD) of the T/H versus the input frequency, where the THD is shown to be lower than -60 dB in the Nyquist band (0–50.6 MHz). 4) Finally, the output spectrum of the proposed power-switchable T/H amplifier is shown in Fig. 10, with a 40.6-MHz sinusoidal input wave sampled at 100 MHz, and the T/H exhibits SFDR $= 70$ dB, SNDR $= 61$ dB, and THD $= 68$ dB. The overall performance is summarized in Table I.

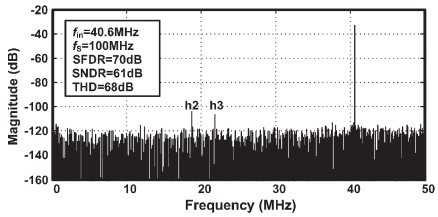

Fig. 10. Measured output signal spectrum of the power-switchable T/H sampling a 40.6-MHz input at 100 MHz. ($V_{\rm in} = 800\ {\rm mV_{pp}}$).

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED POWER-SWITCHABLE T/H AMPLIFIER

Technology	90nm CMOS
Maximum Sampling Frequency	100MHz
Differential Input Range	0.8V_{pp}
Maximum Input Frequency	50MHz
THD (f_{in}=40.6MHz)	68dB
THD (f_{in}=50.6MHz)	60dB
SFDR (f_{in}=40.6MHz, f_S=100MHz)	70dB
SFDR (f_{in}=50.6MHz, f_S=100MHz)	63dB
Supply Voltage	1.2V
Power (f_S=40MHz, V_{dd}=1.2V)	1.57mW
Power (f_S=100MHz, V_{dd}=1.2V)	2.97mW
Power (f_S=100MHz, V_{dd}=0.8V)	0.69mW
Active Area	0.18x0.13mm^2

V. CONCLUSION

This brief has presented a power-switchable T/H implemented in 90-nm CMOS operating at 1.2 V, with more-than-63-dB SFDR and 60-dB THD. The measured performance has demonstrated a prototype's operation up to 100 MS/s, with a 50.6-MHz 0.8-$V_{\rm pp}$ input. The proposed P-S technique has enhanced the linearity of the T/H while also reducing the power consumption.

ACKNOWLEDGMENT

The authors would like to thank the unknown reviewers for the advices and contributions.

REFERENCES

[1] K. R. Stafford, R. A. Blanchard, and P. R. Gray, "A complete monolithic sample/hold amplifier," *IEEE J. Solid-State Circuits*, vol. SSC-9, no. 6, pp. 381–387, Jul. 1974.

[2] M. Choi and A. A. Abidi, "A 6-b 1.3-Gsample/s A/D converter in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1847–1858, Dec. 2001.

[3] S. Limotyrakis, S. D. Kulchychi, D. K. Su, and B. A. Wooley, "A 150-MS/s 8-b 71-mW CMOS time-interleaved ADC," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1057–1067, Dec. 2005.

[4] A. M. Abo and P. R. Gray, "A 1.5-V, 10-b, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[5] H.-G. Wei, U.-F. Chio, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A power scalable 6-Bit 1.2 GS/S flash ADC with power on/off track-and-hold and preamplifier," in *Proc. IEEE ISCAS*, Seattle, WA, May 2008, pp. 5–8.

[6] A. Boni, A. Pierazzi, and C. Morandi, "A 10-b 185-MS/s track-and-hold in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 195–203, Feb. 2001.

[7] X. Jiang and M. C. Chang, "A 1-GHz signal bandwidth 6-bit CMOS ADC with power-efficient averaging," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 532–536, Feb. 2005.