phase velocity v_{ph} mismatching. W, S and S_c are tuned separately in each step of the minimisation process in connection with the error function for Z, C and v_{ph}, respectively. This scheme reduces the number of optimisation steps in comparison with a conventional Newton–Raphson optimisation procedure.

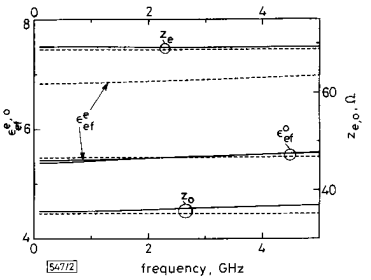

Fig. 2 *Modal effective dielectric constants and characteristic impedances for 50 Ω, 10 dB coupler design based on CCS and MCS*

---- CCS: $W = 0{\cdot}41$, $S = 0{\cdot}14$, $h_1 = 0$, $h_2 = 0{\cdot}49$, $h_3 = 8{\cdot}1$, $a = 12$

——— MCS: $W = 0{\cdot}69$, $S = 0{\cdot}30$, $S_c = 1{\cdot}46$, $h_1 = 11{\cdot}7$, $h_2 = 0{\cdot}49$, $h_3 = 8{\cdot}1$, $a = 12$

MCS and CCS dimensions in millimetres

Substrate: $\varepsilon_r = 9{\cdot}6$

Experimental results: A 10 dB, 2 GHz coupler has been designed with the method of this Letter. Identical mode phase velocities cannot be achieved with the available substrate, while keeping reasonable dimensions, but the difference between the modal phase velocities has been reduced by the presence of the slot in the ground plane. The S parameters were measured with the HP-8510 ANA and are shown in Fig. 3. Theoretical data for the coupling have been also included for comparison and they agree very well with experimental results (coupling measured at 2 GHz is 10·01 dB). More than 33 dB return loss and almost 40 dB isolation are measured at 2 GHz, in accordance with theoretical predictions (notice that measurements were carried out without any adjustment after the fabrication process and without de-embedding of coax-microstrip transitions). A similar design was made by using a CCS for comparison purposes. In this case, S should be significantly smaller ($S = 0{\cdot}06$ mm), which results in fabrication difficulties. Moreover, theoretical isolation is limited to about 26 dB (at 2 GHz). This is significantly worse than isolation experimentally obtained with the MCS. Consequently, the structure analysed in this Letter is useful in increasing the isolation and coupling of edge coupled strips configuration.

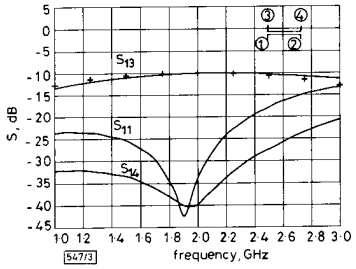

Fig. 3 *Experimental S parameters and theoretical S_{13} for 50 Ω, 10 dB MCS design*

Substrate: $\varepsilon_r = 2{\cdot}43$

Dimensions (mm): $W = 2{\cdot}09$, $S = 0{\cdot}17$, $S_c = 3$, coupling length $l_c = 27{\cdot}9$

Box dimensions and substrate thickness are same as in Fig. 2

——— experimental S parameters

× theoretical S_{13} parameters

Conclusions: The full-wave analysis of a modified pair of coupled microstrip lines has been developed. The analysis has been used as the basis of an optimisation scheme to accurately design a directional coupler. Appropriate analytical preprocessing has been used to accelerate the computations. Measured data confirm the predictions of the theory. The structure is thus useful for improving isolation and coupling of MIC couplers.

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NOVEL SECOND-ORDER SWITCHED-CAPACITOR INTERPOLATOR

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Indexing terms: Switched-capacitor networks, Signal processing, Digital filters, Circuit design

A novel switched-capacitor interpolator circuit is proposed for the realisation of arbitrary second-order interpolating functions employing a reduced number of switching waveforms and yielding low capacitance spread and total capacitor area.

Introduction: Switched-capacitor (SC) interpolators are specialised networks that increase the sampling rate from a low value F_s to a higher value LF_s, and possess an appropriate filtering function to shape the baseband signals and reject the corresponding unwanted imaging components. Infinite impulse response (IIR) SC interpolators have been traditionally implemented based on the nonoptimum and suboptimum classes of circuits defined according to the resulting speed requirements of the operational amplifiers (OAs). Nonoptimum IIR SC interpolator circuits are usually implemented using classical biphase SC filters where the resulting speed of the OAs and capacitance spread are both determined by the higher output sampling frequency LF_s. The suboptimum type of IIR SC interpolator circuits consist of the cascading of a nonrecursive polyphase structure with an interpolating factor L and an SC filter operating at LF_s [1]. Although the polyphase structure can employ OAs operating at the low

sampling rate F_s, faster OAs are still needed in the SC filter operating at LF_s.

The purpose of this Letter is to introduce a novel SC interpolator circuit, with optimum implementation, where both OAs can operate at the lower sampling rate F_s and the realisation of arbitrary second-order interpolating functions can be achieved employing a reduced number of switching waveforms and requiring low capacitance spread and total capacitor area.

Modified z-transfer function: For simplicity, the type of SC interpolator circuit proposed in this Letter will be described considering an example where the sampling rate increases by a factor of $L = 3$ and the interpolating function is of second order. Specifically, we consider an SC lowpass interpolator with sampling rate increase from 384 kHz to 1·152 MHz and bilinear second order Chebyshev lowpass response with cutoff frequency of $f_c = 4{\cdot}8$ kHz, 0·01 dB passband ripple, and minimum stopband attenuation of 25 dB at 76·8 kHz. Based on a computer-aided filter synthesis procedure we obtain first the original bilinear z-transfer function

$$H(z) = k\frac{[1 - 2r_z\cos(\theta_z)z^{-1} + z^{-2}](1 + z^{-1})}{1 - 2r_p\cos(\theta_p)z^{-1} + r_p^2z^{-2}}$$

$$= 0{\cdot}0062\frac{(1 - 0{\cdot}9074z^{-1} + z^{-2})(1 + z^{-1})}{1 - 1{\cdot}8835z^{-1} + 0{\cdot}8902z^{-2}} \quad (1)$$

where $r_{z(p)}$ and $\theta_{z(p)}$ are the polar co-ordinates of both the zeros and poles, and the unit delay period is equivalent to $1/3F_s$. After modification for optimum implementation [2, 3] this leads to

$$H'(z) = \frac{\sum_{i=0}^{2L+1} a_i' z^{-i}}{1 - 2r_p^L\cos(L\theta_p)z^{-L} + r_p^{2L}z^{-2L}}$$

$$= 10^{-3}\frac{6{\cdot}165 + 12{\cdot}183z^{-1} + 18{\cdot}028z^{-2} + 19{\cdot}094z^{-3} + 18{\cdot}971z^{-4} + 17{\cdot}792z^{-5} + 10{\cdot}789z^{-6} + 4{\cdot}886z^{-7}}{1 - 0{\cdot}7055z^{-3} + 1{\cdot}6515z^{-6}} \quad (2)$$

where the unit delay period still refers to the higher sampling rate $3F_s$.

Circuit architecture and switching timing: The above z-transfer function can be implemented using the proposed SC interpolator shown in Fig. 1. The circuit architecture of Fig. 1*a* consists of a two-integrator loop (TIL) network whose amplifiers operate both at the low input sampling frequency F_s, together with two output polyphase networks [4] whose characteristics depend both on the interpolation factor L and on the complexity of the numerator polynomial function. The interpolated signal is obtained at the output of an SC accumulator which linearly combines the packets of charge transferred through the branches of the polyphase networks. Such an accumulator employs a unity gain buffer for reduced power and silicon consumption and high frequency of operation [2, 5]. The operation of the interpolator presented in Fig. 1*a* is referred to the switch timing indicated in Fig. 1*b*, which is divided into three sets of time slots corresponding to time frames S, T and R. Time slots E and O of time frame S define the input sampling instants and control the operation of the recursive part of the circuit in a similar way as in a conventional biquad. These time slots are also used to define the input sampling of the polyphase networks, and whose operation additionally requires the time slots of time frames T and R. Whereas each one of the time slots 0, 1, and 2 of time frame T, define an interpolated output sample, time slots R_0, R_1 and R_2, of time frame R, are used to reset the previous output sample of the accumulator.

Design equations: The z-transfer function of the circuit of Fig. 1*a* can be expressed by [2]

$$T(z) = \frac{V_0}{V_i}(z)$$

$$= T_{32_1}(z)\cdot T_{21_1}(z) + T_{32_2}(z)\cdot T_{21_2}(z) \quad (3)$$

where $T_{21_1}(z) = V_{2_1}/V_i$, $T_{21_2}(z) = V_{2_2}/V_i$ and $T_{32_1}(z) = V_{3_1}/V_{2_1}$, $T_{32_2}(z) = V_{3_2}/V_{2_2}$. By applying well known SC analysis tech-

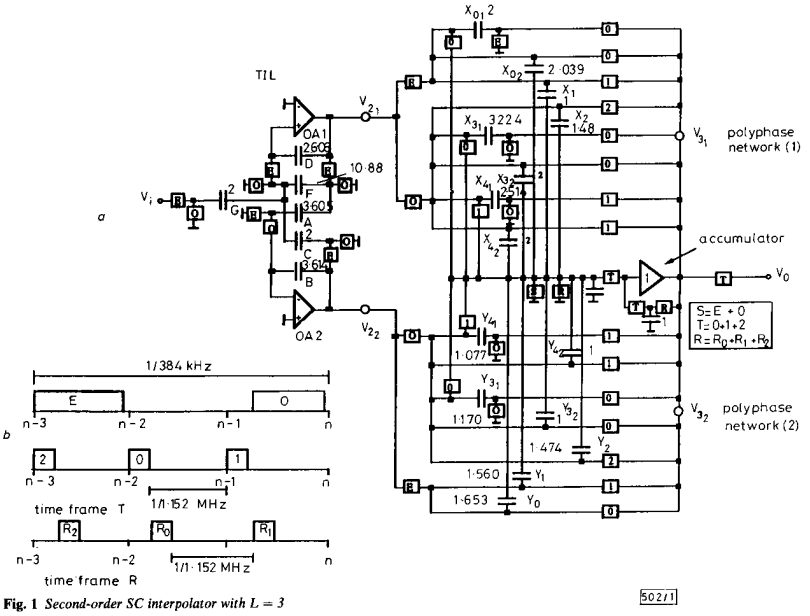


Fig. 1 *Second-order SC interpolator with $L = 3$*
a Circuit architecture
b Switching waveforms

niques [3], it can be shown that the overall z-transfer function resulting from eqn. 3 is given by

$$T(z) = -\frac{G \cdot z^{-x}}{D \cdot (B+F)} \times \frac{\left[(1-z^{-3}) \cdot \sum_{i=0}^{4}(X_i \cdot z^{-i}) + A \cdot z^{-3} \cdot \sum_{i=0}^{4}(Y_i \cdot z^{-i})\right]}{\left\{1 + \left[\frac{(A \cdot C - D \cdot F - 2B \cdot D)}{D \cdot (B+F)}\right] \cdot z^{-L} + \left[\frac{B \cdot D}{D \cdot (B+F)}\right] \cdot z^{-2L}\right\}} \quad (4)$$

where the unit delay period refers to the output sampling rate. The factor z^{-x} represents an unimportant flat delay between the end of time slot E and the end of time slot 0. The complete set of design equations are obtained by equating eqn. 2 to eqn. 4, leading to

$$\boldsymbol{B} = \boldsymbol{D} = 1$$

$$\boldsymbol{F} = \frac{1}{r_p^{2L}} - 1$$

$$\boldsymbol{A} = \boldsymbol{C} = \sqrt{\{2 + F - [2r_p^L \cos(L\theta_p)](1+F)\}}$$

$$\boldsymbol{X}_i = \frac{-(1+F)\boldsymbol{a}_i'}{G} \quad \text{if } i = 0, 1, 2$$

and

$$\boldsymbol{X}_i = \frac{-(1+F)\boldsymbol{a}_{i+3}'}{G} \quad \text{if } i = 3, 4 \quad (5)$$

$$\boldsymbol{Y}_i = -\frac{1}{A}\left[\frac{-(1+F)\boldsymbol{a}_{i+3}'}{G} + \boldsymbol{X}_{i+3} - \boldsymbol{X}_i\right] \text{ if } i = 0, 1$$

$$\boldsymbol{Y}_i = -\frac{1}{A}\left[\frac{-(1+F)\boldsymbol{a}_{i+3}'}{G} - \boldsymbol{X}_i\right] \quad \text{if } i = 2$$

and

$$\boldsymbol{Y}_i = \boldsymbol{X}_i \quad \text{if } i = 3, 4$$

Designing for reduced capacitance spread is achieved by making, in some equations, $\boldsymbol{X}_i = \boldsymbol{X}_{i_1} - \boldsymbol{X}_{i_2}$ or $\boldsymbol{Y}_i = \boldsymbol{Y}_{i_1} - \boldsymbol{Y}_{i_2}$. The final normalised capacitance values obtained after scaling for maximum signal handling capability are also indicated in Fig. 1*a* yielding a total capacitor value of only 88·57 units.

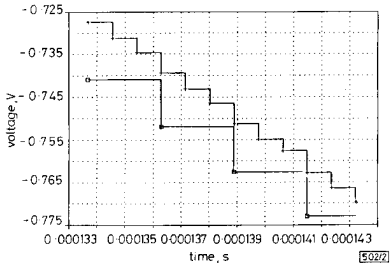
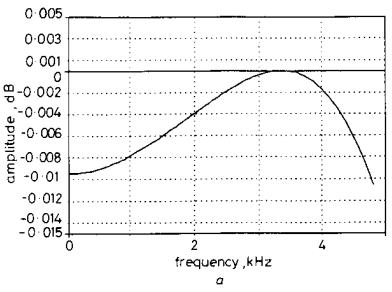


Fig. 2 *Transient analysis of SC interpolator of Fig. 1 showing input samples at F_s and interpolated output samples at $3F_s$*

The time domain operation of the proposed SC interpolator can be observed in Fig. 2, where we can see a portion of a 1 kHz input sinewave sampled at F_s and its interpolated output signal at $3F_s$. Fig. 3 shows the nominal computer simulated amplitude responses in the passband (Fig. 3*a*), and from DC to $3F_s = 1{\cdot}152$ MHz (Fig. 3*b*), where the notches at F_s and its integer multiples are due to the sample-hand-hold effect.



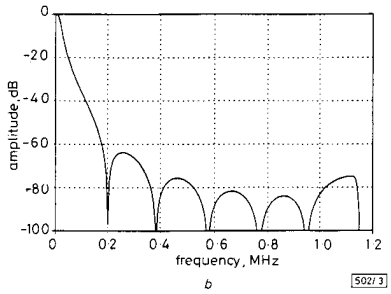


Fig. 3 *Amplitude response of SC interpolator of Fig. 1*
a Passband (DC–4·8 kHz)
b From DC to 1·152 MHz

Conclusions: This Letter presented a novel SC interpolator circuit where not only the speed requirements of the amplifiers are determined by the lower input sampling rate F_s but which also possesses attractive features concerning the low values of both the capacitance spread and total capacitor area. This was illustrated considering a simple design example for a bilinear second-order interpolating function and interpolating factor of $L = 3$.

4th December 1991

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