Design of an ESD-Protected Ultra-Wideband LNA in Nanoscale CMOS for Full-Band Mobile TV Tuners

Pui-In Mak, *Member, IEEE*, and Rui Martins, *Fellow, IEEE*

***Abstract*—This paper presents an electrostatic discharge (ESD)-protected ultra-wideband (UWB) low-noise amplifier (LNA) for full-band (170-to-1700 MHz) mobile TV tuners. It features a PMOS-based open-source input structure to optimize the I/O swings under a mixed-voltage ESD protection while offering an inductorless broadband input impedance match. The amplification core exploiting *double current reuse* and *single-stage thermal-noise cancellation* enhances the gain and noise performances with high power efficiency. Optimized in a 90-nm 1.2/2.5-V CMOS process with practical issues taken into account, the LNA using a constant-g_m bias circuit achieves competitive and robust performances over process, voltage and temperature variation. The simulated voltage gain is 20.6 dB, noise figure is 2.4 to 2.7 dB, and IIP3 is $+10.8$ dBm. The power consumption is 9.6 mW at 1.2 V. $|S_{11}| < -10$ dB is achieved up to 1.9 GHz without needing any external resonant network. Human Body Model ESD zapping tests of ± 4 kV at the input pins cause no failure of any device.**

***Index Terms*—CMOS, electrostatic discharge (ESD), low-noise amplifier (LNA), mobile TV tuner, radio frequency (RF), thermal-noise cancellation, ultra-wideband (UWB).**

I. Introduction

A LARGE number of independently developed mobile TV standards worldwide has led to the demand of multiband silicon tuners for cost minimization of the embedded handheld devices that are intended for global market sale. Presently, the most dominant mobile TV standards are: terrestrial—digital multimedia broadcasting (T-DMB), integrated services digital broadcasting—terrestrial (ISDB-T), MediaFLO, digital video broadcasting—handheld (DVB-H) and digital multimedia broadcasting—terrestrial (DMB-T). Their brief profiles are listed in Table I.

From the implementation viewpoint, the digital back-end can be efficiently shared since those standards favor similar kinds of modulation and data coding. For the radio frequency (RF) front-end, however, state-of-the-art solutions still require dedicated RF circuits optimized for each band, e.g., [1]. Yet, with the advance of fabrication technologies, multistandard-compliant system-on-chip (SoC) solutions using wideband techniques to cover multiple applications would have the highest potential to yield the optimum cost [2].

TABLE I
BRIEF PROFILES OF THE MOST DOMINANT MOBILE TV STANDARDS

Mobile TV Standard	Frequency	Data Coding	Air Interface
T-DMB (Korea, China, Europe)	174 – 245 MHz 1452 – 1492MHz	Video: H.264 30 fps/QVGA Audio: BSAC/AAC+	OFDM (QPSK)
ISDB-T (Japan, Brazil)	470 – 770 MHz	Video: H.264 15 fps/QVGA Audio: AAC+	OFDM (QPSK/16QAM)
DVB-H (Europe, US)	470 – 860 MHz 1670 – 1675 MHz	Video: H.264 30 fps/QVGA Audio: AAC+	OFDM (QPSK/16QAM/64QAM)
DMB-T (China)	470 – 860 MHz 1670 – 1675 MHz	Video: H.264 30 fps/QVGA Audio: AAC+	OFDM (QPSK/16QAM/64QAM)
MediaFLO™ (US)	712-722 MHz	MPEG4 (Video)	OFDM

This paper presents the circuit techniques enforced in the design of an electrostatic discharge (ESD)-protected ultra-wideband (UWB) low-noise amplifier (LNA) for mobile-TV applications. It covers the full band of mobile-TV services from 170 to 1700 MHz such that only one LNA is necessary to support multiple standards. Unlike the design of narrowband LNAs, concurrent reception over a wide range of spectrum necessitates the LNA to feature high linearity, preventing desensitization by the high-power blockers. This requirement, in conjunction with the design goals of high ESD protection level, low noise figure (NF), low power, impedance match, and high gain, constitute hard tradeoffs to obtain a sensible balance in between. Being realized in a 90-nm CMOS process, the proposed LNA is optimized by introducing novel circuit techniques, together with careful sizing and biasing strategies, to achieve competitive and robust RF performances over process, supply voltage, and temperature (PVT) variations.

The organization of this paper is as follows. Section II describes the circuit structure and design issues of the proposed LNA. The practical issues governing the robustness of the LNA over PVT variation are summarized in Section III. The simulation results and benchmarks of this work to prior arts are given in Section IV. Section V concludes the paper.

II. Circuit Description

A. Full-Band Mobile-TV Tuner Architecture

Fig. 1 shows the block diagram of the full-band mobile-TV tuner to which the proposed LNA is referred. The architecture is based on a direct-conversion receiver that is differential to avoid common-mode pickups and even-order distortion. As addressed

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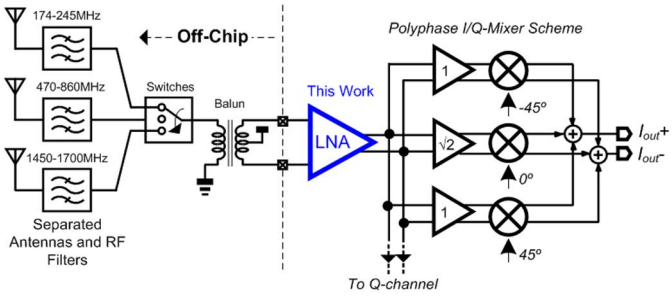

Fig. 1. Full-band mobile-TV tuner using a single wideband balun and LNA.

in many existing TV tuners (e.g., [1], [3]–[5]), the baluns required for generating the differential inputs in this frequency range are bulky in size, and should be placed off chip. Wideband baluns having a center-tapped secondary can be employed. The typical insertion losses of a 4.5–2000-MHz 1:1 SMD balun are 0.32 and 2 dB in 4.5–1000 MHz and 1–2 GHz, respectively [6].

Wideband reception suffers from the problem of harmonic mixings, i.e., inband blockers located at the harmonics of the local oscillator will become the co-channel interferers. Basically, a 60-dB harmonic rejection ratio is necessary. To achieve this, separated RF filters in conjunction with a polyphase I/Q-mixer scheme are employed to doubly reject the harmonic-mixing products. The polyphase I/Q-mixer scheme includes three transconductance amplifiers having a gain ratio of $1 : \sqrt{2} : 1$ to drive the passive current-mode mixers [7]. A *voltage-to-voltage* LNA is therefore chosen to drive those transconductance amplifiers that feature purely capacitive input impedance.

B. PMOS-Based Open-Source Input Structure and Mixed-Voltage ESD Protection

Fig. 2 depicts the schematic of the proposed LNA. In order to save voltage headroom and reduce the number of active devices, the cascode structure was not applied. The main consequence of not using a cascode structure is a limited reverse isolation. The results, however, show that with proper sizings the reverse isolation is acceptable in the targeted frequency range. No matching network is required as the source node of a nanoscale transistor offers a simple broadband input impedance match.

The 1:1 balun equally splits the RF signal $V_{\rm rf}$ to M_1 and M_2 with opposite phases, where reverse-biased $\rm P^+$-diffusion diode $D_{\rm P}$, and $\rm N^+$-diffusion diode $D_{\rm N}$, are adopted for pin-to-rail ESD clamp. ESD-protection rail-clamp circuits incorporated with $\rm D_P$ and $D_{\rm N}$ offer low-ohmic discharge paths among the I/O supply voltage $V_{\rm DD,I/O}$, the core supply voltage $V_{\rm DD}$, and the common ground *GND*. The aim of choosing a pMOS-based input structure instead of nMOS is illustrated by comparing the different bias conditions of the LNA and its pin-to-rail ESD clamp, as follows.

In the case of nMOS [Fig. 3(a)], the input swing can be optimized by setting the common-mode voltage $V_{\rm CM,IN}$ to 0.6 V. Regrettably, $V_{\rm CM,IN} = 0.6$ V will offset the output common-mode level by the same amount, resulting in a limited output swing. Though $V_{\rm CM,IN} = 0$ V can resolve such an output swing

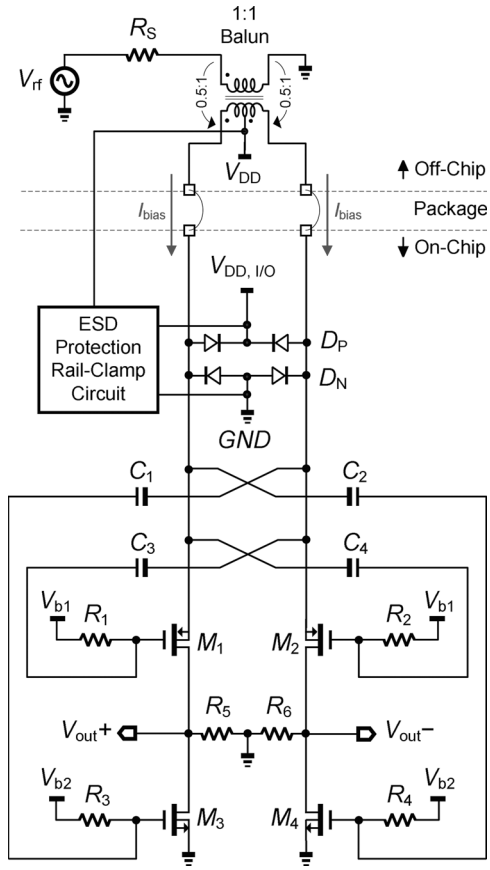

Fig. 2. Schematic of the proposed LNA.

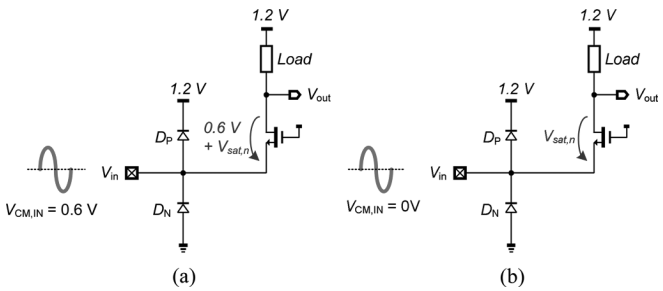

Fig. 3. Diode clamps with an nMOS-input structure. (a) $V_{\rm CM,IN} = 0.6$ V. (b) $V_{\rm CM,IN} = 0$ V.

limitation [Fig. 3(b)], $D_{\rm N}$ at such a $V_{\rm CM,IN}$ is at a higher risk of forward bias, unavoidably sacrificing part of the input swing.

Conventionally, the above tradeoff cannot be resolved by using pMOS devices as shown in Fig. 4(a). In this study, we propose to use $V_{\rm DD,I/O}$ as the driving voltage for the pin-to-rail ESD clamp. $V_{\rm DD,I/O}$ is commonly available in modern dual-oxide CMOS processes necessary for input–output (I/O) interfaces. Given that $V_{\rm DD,I/O} = 2.5$ V in the employed technology, the I/O swings can be concurrently maximized, as shown in Fig. 4(b). Besides that, considering the ESD robustness, $V_{\rm CM,IN} = V_{\rm DD}$ balances the discharge capability of $\pm$ zapping events.

The improvement of the proposed input structure in the employed 90-nm CMOS technology is illustrated by plotting the

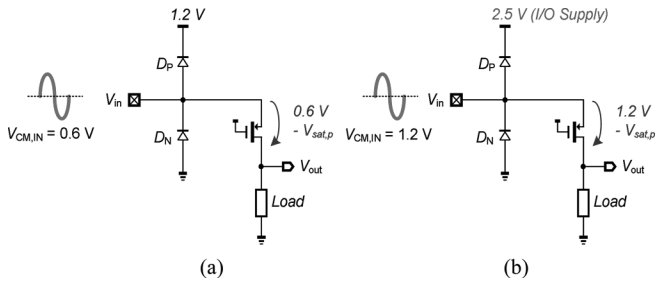

Fig. 4. Diode clamps with a pMOS-input structure. (a) $V_{\mathrm{CM,IN}} = 0.6$ V. (b) $V_{\mathrm{CM,IN}} = 1.2$ V, but the clamping voltage is the $V_{\mathrm{DD,I/O}} = 2.5$ V.

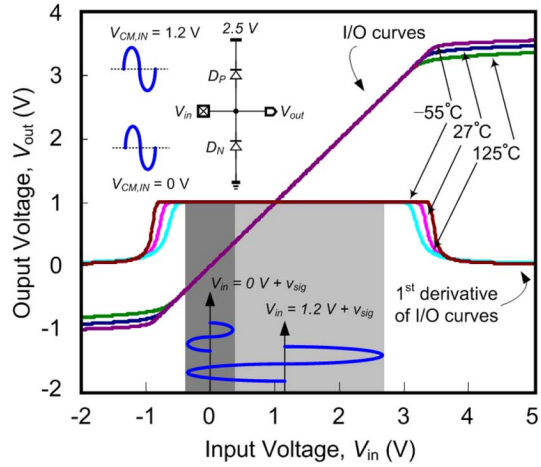

Fig. 5. Diode-clamp I/O transfer curves and their first derivatives at different temperatures, showing the linear input swing versus the selected $V_{\mathrm{CM,IN}}$.

diode-clamp I/O transfer curves and their first derivatives at typical and extreme temperatures (Fig. 5). With $V_{\mathrm{CM,IN}} = V_{\mathrm{DD}} = 1.2$ V, the linear input $[v_{\mathrm{sig}}(t)]$, even at the highest temperature, has a swing of roughly 3 $\mathrm{V_{pp}}$ in the pMOS case, while it is just roughly 0.8 $\mathrm{V_{pp}}$ in nMOS case with $V_{\mathrm{CM,IN}} = GND$ (0 V).

C. Double Current Reuse for g_m-Enhancement

Current reuse is power-efficient in gain enhancement. In this study, current is doubly reused to boost the transconductance (g_m). A simplified small-signal half-circuit equivalent of Fig. 2 is shown in Fig. 6. First, M_1 gate–source terminals are coupled with a gain of -1 (i.e., capacitive cross-coupling [8]) such that the transconductance of M_1, g_{m1}, is enhanced to g'_{m1}, as given by

$$g'_{m1} = (1 + A_x)g_{m1} \tag{1}$$

where A_x stands for the voltage transfer of the high-pass network: C_3 and R_1. The capacitance division between M_1's C_{GS} and C_3 gives $A_x < 1$.

The capacitive cross-coupling reuses in the nMOS device M_3 to further enhance the overall transconductance G_m as given by

$$G_m = g'_{m1} + A_y g_{m3} \tag{2}$$

where A_y is the voltage transfer of the high-pass network: C_1 and R_3. R_5 is a grounded resistor. R_5 and C_{OUT} in parallel with the output resistance of M_3 (i.e., r_{o3}), and the resistance

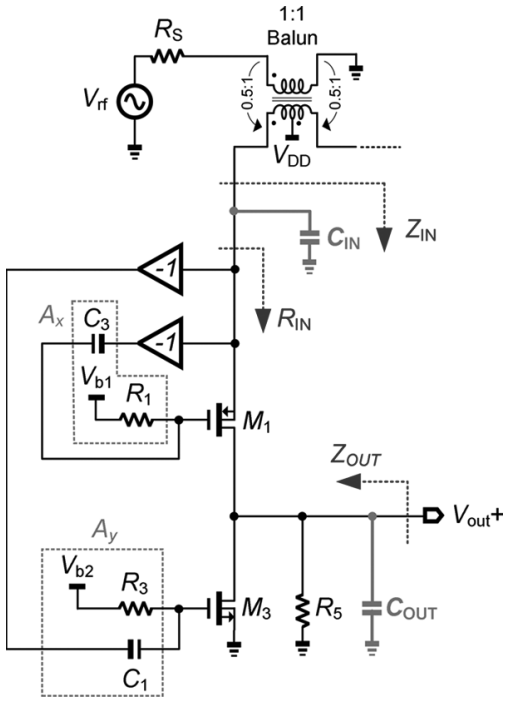

Fig. 6. Single-ended small-signal equivalent circuit of the proposed LNA.

looking into the drain node of M_1 [i.e., $R_{\mathrm{out,M1}} = r_{o1} + R_S + g_{m1}r_{o1}(A_x+1)R_S$], gives the total output impedance Z_{OUT} as

$$Z_{\mathrm{OUT}} = R_5 \| [r_{o1} + R_S + g_{m1}r_{o1}(A_x+1)R_S] \| r_{o3} \| \frac{1}{j\omega C_{\mathrm{OUT}}}. \tag{3}$$

Grounded R_5 implemented with a high-resistive polysilicon is to linearize Z_{OUT} and optimize the output common-mode voltage. Since nanoscale transistors suffer from strong channel-length modulation, the conventional $1/g_m$ approximation of the LNA's source-node input impedance leads to poor matching between the calculated and simulated results. An accuracy expression of the resistive input impedance R_{IN} has to count all finite output impedances into account, i.e., r_{o1} of M_1 and r_{o3} of M_3, yielding

$$R_{\mathrm{IN}} = \frac{R_5 \| r_{o3} \| \frac{1}{j\omega C_{\mathrm{OUT}}} + r_{o1}}{1 + g'_{m1}r_{o1}}. \tag{4}$$

R_{IN} in parallel with the input parasitic capacitance C_{IN} gives the input impedance Z_{IN} of the LNA as given by

$$Z_{\mathrm{IN}} = R_{\mathrm{IN}} \| \frac{1}{j\omega C_{\mathrm{IN}}}. \tag{5}$$

After all, the differential voltage gain of the LNA, $A_{v,diff}$, can be obtained as

$$A_{v,\mathrm{diff}} = \frac{V_{\mathrm{out+}} - V_{\mathrm{out-}}}{V_{rf}} = \frac{2Z_{\mathrm{IN}}}{R_S + 2Z_{\mathrm{IN}}} G_m Z_{\mathrm{OUT}}. \tag{6}$$

D. Single-Stage Thermal-Noise Cancellation

Noise-cancelling LNAs using a cascading configuration have been reported, e.g., [9], [10]. However, additional amplification stages lead to higher NF and poor linearity. In this study,

thermal-noise cancellation can be achieved in a single stage by taking advantages from the bi-directional coupling behavior of the balun and the structure of the LNA after double-current reuse. Reexamining Fig. 2, we can observe that the thermal noise of M_1 (which can be modeled as a noise current source connecting its drain and source) is partly injected to $V_{\rm out}+$ and partly negatively couples to the source of M_2 through the balun and to the gate of $M_2(M_4)$ through the cross-coupling network $R_2 - C_4(R_4 - C_2)$. An identical noise coupling operation occurs around M_2. Differentially, certain noise transfer paths will be out phased from the others, yielding a way to cancel out the noise of M_1 with virtually no cost. Based on $R_{\rm IN}$ (but not $Z_{\rm IN}$ to simplify the noise analysis), it can be shown that the noise factor F of the LNA is given by

$$F = 1 + \frac{\left[\frac{R_S R_{IN}}{R_S+2R_{IN}} G_m - 1\right]^2 g_{m1}\frac{\gamma_1}{\alpha_1} + g_{m3}\frac{\gamma_3}{\alpha_3} + \frac{1}{R_5}}{\left(\frac{2R_{IN}}{R_S+2R_{IN}}\right)^2 \left(\frac{4R_{IN}}{R_S+2R_{IN}}\right)^2 G_m^2 \frac{R_S}{2}} \quad (7)$$

where $\alpha_1(\alpha_3)$ and $\gamma_1(\gamma_3)$ are the process- and bias-dependent parameters of $M_1(M_3)$, respectively. A detailed deduction of (7) is given in the Appendix. Principally, the noise generated by $M_1(M_2)$ can be minimized by designing

$$\frac{R_S R_{\rm IN}}{R_S + 2R_{\rm IN}} G_m = \frac{R_S R_{\rm IN}}{R_S + 2R_{\rm IN}} \left(g'_{m1} + A_y g_{m3}\right) \to 1. \quad (8)$$

Regrettably, since (6) and (7) are inter-dependent by most parameters, there is no straight way to minimize the overall *system NF* ($\mathrm{NF} = 10 \cdot \log F$) since $A_{v,\rm diff}$ also affects the input-referred noise contribution of the succeeding circuits.

In order to cooptimize the key performance metrics, a constraint-based semi-computed design flow is applied. Given a power budget of 10 mW and a -3-dB output bandwidth of > 1.7 GHz when driving a 0.3-pF load (the input capacitance of the polyphase I/Q-mixer scheme), the size of M_1 and R_5 are picked to fulfill the required R_{IN}, which must be close to $R_S/2$ for an acceptable S_{11} (< -10 dB). R_5 is relatively low ($250\,\Omega$) to desensitize r_{o3} in (5) such that, without affecting the input match, tuning the size of M_3 can trade the $A_{v,\rm diff}$, NF and linearity. Simulation results are plotted in Fig. 7(a) and (b), where the size multiplier (N) of M_3 is swept from 1 to 9. Selecting $N = 5$ yields the highest input-referred third-order intercept point (IIP3) since the third-order derivative of the dc characteristic is close to zero at this N. The corresponding $A_{v,\rm diff}$ is over 20 dB and NF is 2.5 dB. The -3-dB output bandwidth (1.84 GHz), $|\mathrm{S}_{11}|$ (-16.3 dB) and power budget (9.6 mW) are satisfied.

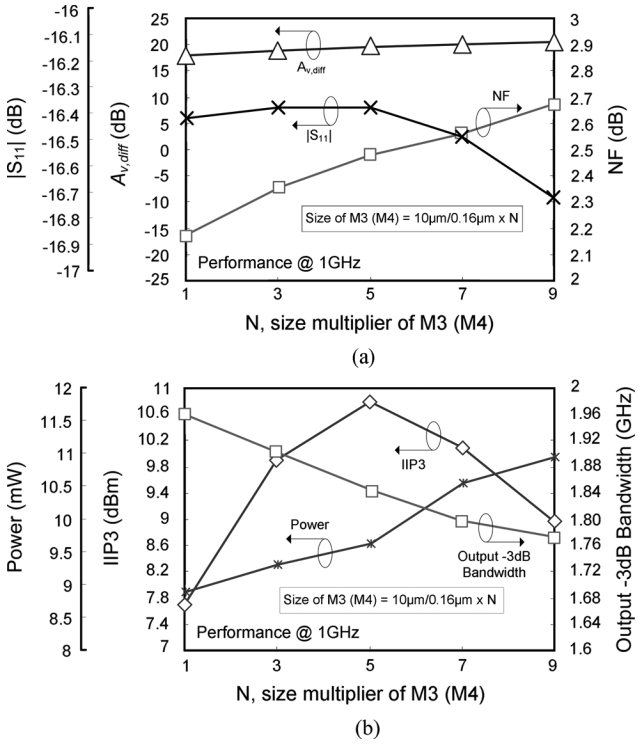

Fig. 7. Size of $M_3(M_4)$ versus RF performances. (a) $|\mathrm{S}_{11}|$, $A_{v,\rm diff}$ and NF. (b) Power consumption, IIP3, and output -3-dB bandwidth.

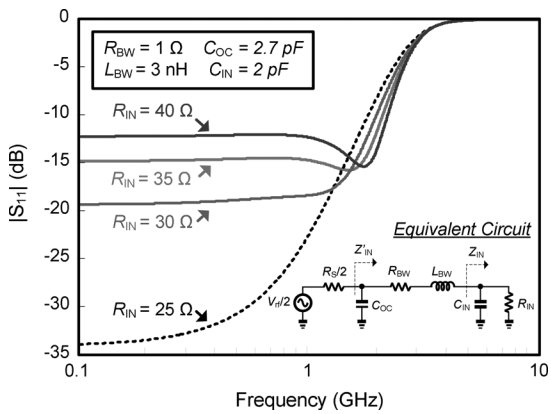

Fig. 8. Input-matching design including package effects.

III. Key Practical Design Issues

A. Package Effect on Input Impedance Match

With the package effect (Fig. 8) taken into account, the single-ended (left-half) input impedance $Z'_{\rm IN}$ of the LNA is given by

$$Z'_{\rm IN} = \frac{1}{j\omega C_{\rm OC}} \left\| \left[j\omega L_{\rm BW} + R_{\rm BW} + \left(R_{\rm IN} \left\| \frac{1}{j\omega C_{\rm IN}} \right. \right) \right] \right. \quad (9)$$

where $C_{\rm OC}$ denotes the parasitic capacitance of the leadframe and soldering pad on the testing board. $L_{\rm BW}$ and $R_{\rm BW}$ stand for the inductance and resistance of the bondwire, respectively, C_{IN} is the total input capacitance resulting from M_1, $D_{\rm N}$, and $D_{\rm P}$, the parasitic capacitance of C_1 and C_3, and the bondpad $(C_{\rm PAD})$.

Similar to the analysis addressed in [11], targeting an in-band $|\mathrm{S}_{11}| < -10$ dB requires an input reflection coefficient magnitude $|\Gamma_{\rm IN}|$ to satisfy

$$|\Gamma_{\rm IN}| = \left| \frac{Z'_{\rm IN} - \frac{R_{\rm S}}{2}}{Z'_{\rm IN} + \frac{R_{\rm S}}{2}} \right| \le 0.32. \quad (10)$$

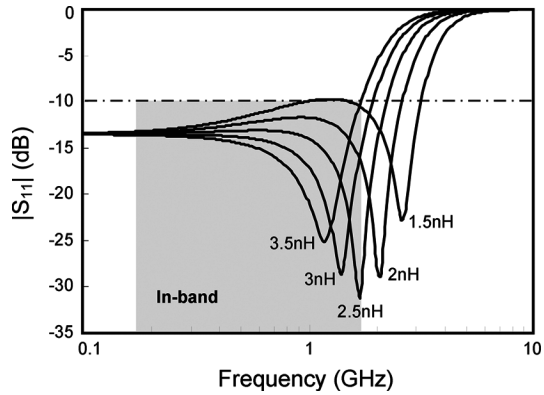

Fig. 9. Input matching versus the inductance ($L_{\rm BW}$) variation of the bondwire.

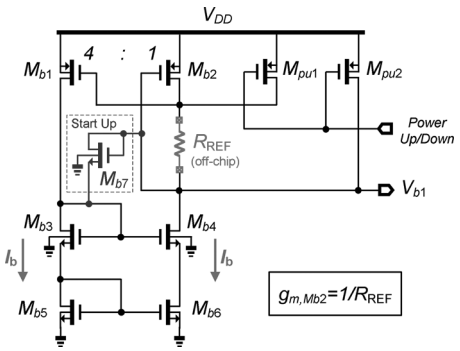

Fig. 10. Self-startup constant-g_m bias circuit (with power up/down control).

With $R_{\rm S} = 50\ \Omega$ and a balun ratio of 1:1, $R_{\rm IN} = 25\ \Omega$ achieves a superior $|{\rm S}_{11}|$. However, the matched bandwidth is insufficient since $C_{\rm IN}$ will lower $Z_{\rm IN}$ when frequency is increasing. Thus, as shown in Fig. 8 as well, the optimal $R_{\rm IN}$ that can result in a broadened bandwidth should be a higher value in practice. Here, $R_{\rm IN}$ between 35–40 Ω gives an adequate $|{\rm S}_{11}|$ over the desired bandwidth, avoiding any external resonant network.

Since the exact value of $L_{\rm BW}$ is uncertain in practice, the picked $R_{\rm IN}$ must guarantee a $|{\rm S}_{11}| < -10$ dB over an acceptable range of inductance variation [12]. As shown in Fig. 9, the tolerable $L_{\rm BW}$ variation is from 1.5 to 3.5 nH for $R_{\rm IN} = 40\ \Omega$.

B. Self-Startup Constant-g_m Bias Circuit

To tackle the PVT variation, a self-startup constant-g_m bias circuit is adopted. As depicted in Fig. 10, an off-chip resistor $R_{\rm REF}$ serves as the reference, such that $g_{m,Mb2}$ can be fixed to the inverse of $R_{\rm REF}$ by equalizing the dc bias current of M_{b1} and M_{b2} (they exhibit a ratio of 4:1 and are both long-channel devices) [13]. The generated V_{b1} is the bias voltage of the LNAs M_1 and M_2. $R_{\rm REF}$ is scaled up by 10× to reduce the power consumption. Thus, the size ratio of M_{b2} to M_1 is set to 1:10 for a correct transconductance ratio.

The self-bias structure requires a start-up circuit. Diode-connected M_{b7} guarantees that the bias circuit can be started up at power-on by satisfying

$$V_{{\rm T},Mb5} + V_{{\rm T},Mb3} + V_{{\rm T},Mb7} + |V_{{\rm T},Mb2}| < V_{\rm DD} \qquad (11)$$

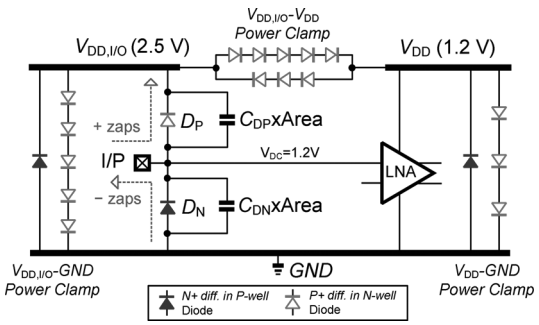

Fig. 11. Mixed-voltage ESD-protection scheme.

and shut down afterwards by satisfying

$$V_{{\rm GS},Mb5} + V_{{\rm GS},Mb3} + V_{{\rm T},Mb7} + |V_{{\rm GS},Mb2}| > V_{\rm DD} \qquad (12)$$

where $V_{\rm T}$ is the threshold voltage of the transistor.

TABLE II
DEVICE DIMENSION

Device	Size	Device	Size
M_1, M_2	(10μm/0.08μm) x 10	$R_{\rm REF}$	400Ω
M_3, M_4	(10μm/0.08μm) x 5	M_{b1}	(10μm/0.08μm) x 4
R_1-R_4	1μm x 40μm = 40kΩ	M_{b2}	(10μm/0.08μm) x 1
C_1-C_4	1μm x 40μm = 2.7pF	M_{b3}-M_{b7}	(1μm/0.32μm) x 8
R_5, R_6	10μm x 3μm = 250Ω	$D_{\rm P}$, $D_{\rm N}$	(1μm/50μm) x 10

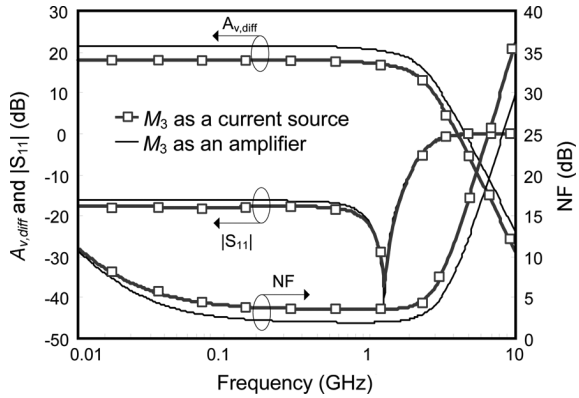

Fig. 12. RF performance comparison of using M_3 as a current source (i.e., only capacitive cross coupling of M_1) or as an amplifier (double-current reuse).

C. Power-Up/Down Control With Reliability Concern

Nanoscale circuits for mobile TV require particular attention of reliability in power-down condition since DVB-H uses time-slicing operation. In the employed 90-nm CMOS process, the proposed LNA operating at 1.2 V is free from hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), and absolute maximum rating (AMR). The primary concern is the negative bias temperature instability (NBTI) of all pMOS devices. To prevent large $V_{\rm GS}$ or $V_{\rm GD}$ in power-down mode, M_{b1} and M_{b2} in the self-startup constant-g_m bias circuit (Fig. 9) are pulled up to $V_{\rm DD}$. In this way, the NBTI stress is transferred to the pull-up switches, $M_{\rm pu1}$ and $M_{\rm pu2}$, which show no impact

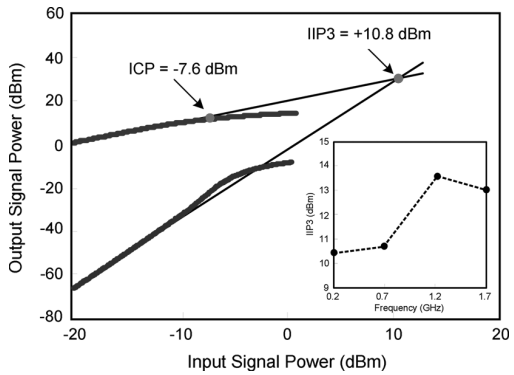

Fig. 13. Two-tone tests at 695 and 700 MHz.

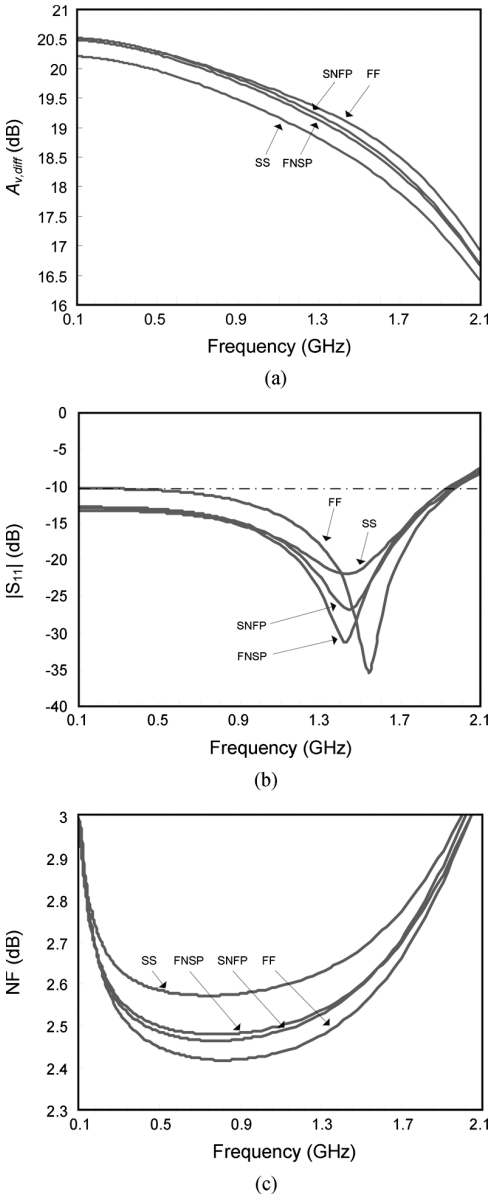

Fig. 14. RF performance in process corners: FAST-FAST (FF), SLOW-SLOW (SS), FAST-NMOS-SLOW-PMOS (FNSP) and SLOW-NMOS-FAST-PMOS (SNFP). (a) $A_{v,\mathrm{diff}}$, (b) $|\mathrm{S}_{11}|$, and (c) NF.

to the LNA in active mode. This technique simultaneously pulls up V_{b1} to V_{DD}, guaranteeing M_1 and M_2 of the LNA are also shut down in the same manner.

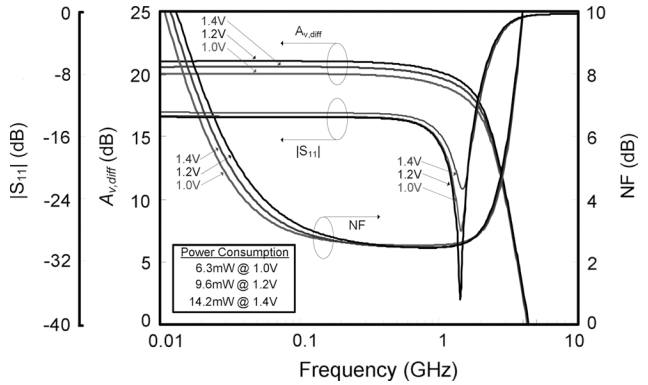

Fig. 15. RF performances versus supply voltage variation.

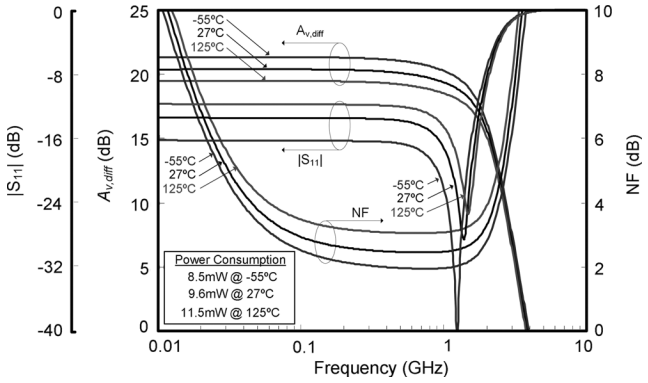

Fig. 16. RF performances versus temperature variation.

D. Mixed-Voltage ESD Protection Scheme

Protecting the nanoscale thin-oxide devices from ESD events requires well-designed discharge paths to the supply rails. Fig. 11 shows the designed mixed-voltage ESD clamps. Power clamps based on p+/n-well diode chains efficiently realize a sufficient high-trigger voltage that is greater than the supply, such that the leakage current and the chance of accidental latching due to normal supply fluctuation are minimized. For instance, with a silicon diode threshold voltage of ~ 0.65 V, the $V_{\mathrm{DD,I/O}}$-*GND* power clamp needs five diodes in series, whereas for V_{DD}-*GND* only three are necessary. The selected number of diodes in the $V_{\mathrm{DD,I/O}} - V_{\mathrm{DD}}$ power clamp have had the precaution of different supply start-up sequences. For instance, $V_{\mathrm{DD,I/O}}$ may start before V_{DD}. The proposed scheme is optimized to avoid the happening of any forward-bias current in all supply start-up sequences.

The dimension of $D_{\mathrm{P}}(D_{\mathrm{N}})$ is $1\ \mu\mathrm{m}/501\ \mu\mathrm{m} \times 10$. Since the technology determines that the parasitic capacitances resulting from D_{P} and D_{N} per unit area are $C_{\mathrm{DP}} = 0.9\ \mathrm{fF}/\mu\mathrm{m}^2$ and $C_{\mathrm{DN}} = 0.74\ \mathrm{fF}/\mu\mathrm{m}^2$, respectively, the imposed total parasitic capacitance at the input is ~ 870 fF, which occupies 44% of the total C_{IN} budget. The remaining C_{IN} budget can be reserved for the $C_{\mathrm{PAD}}(\sim 300\ \mathrm{fF})$, the input parasitic capacitance of M_1, and the parasitic capacitances of C_2, C_4, and C_5, which are all metal-over-metal (MoM) capacitors.

TABLE III
BRIEF PERFORMANCE COMPARISON OF RECENTLY PUBLISHED WIDEBAND LNAS

Ref - Year	Technology	Bandwidth (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	Power (mW)	No. of inductors	ESD protection
[15] & This work S	90nm CMOS	0.1 ~ 1.89	20.6 VG	<2.7	+10.8 @ 0.7 GHz	1.2 *	9.6	0	± 4 kV
[16] JSSC'08 M	65nm CMOS	0.2 ~ 5.2	13 -15.6 VG	<3.5	> 0	1.2	21	0	No
[17] JSSC'08 M	130nm CMOS	0.8 ~ 2.1	14.5 VG	2.6	+16	1.5	17.4	0	No
[18] ASSCC'07 M	180nm CMOS	0.05 -0.86	15 VG	2.5	+ 8.3	1.8	7.2	0	No
[19] RFIC'07 m	90nm CMOS	0.4 ~ 1	16 PG	<5.3	–17 @ 1 GHz	1.2	16.8	0	No
[20] TCAS-II'07 S	130nm CMOS	0.2 ~ 3.8	11.2 VG	<2.85	–2.7 @ 3 GHz	1.2	1.9	0	No
[20] TCAS-II'07 S	130nm CMOS	0.2 ~ 6.2	10.5 VG	<2.85	–2.7 @ 3 GHz	1.2	1.9	2	No
[21] TCAS-I'07 M	180nm CMOS	2.8 ~7.2	19.1 PG	<3.8	-1 @ 6 GHz	1.8	32	7	No
[22] PRIME'06 S	130nm CMOS	0.9 ~ 2.5	17 PG	2	–5	1.2	15.6	4	No
[23] RFIC'05 M	130nm CMOS	0.1 ~ 0.93	13 PG	4	–10.2	1.2	0.72	0	No
[24] CICC'05 M	130nm CMOS	0.1 ~ 6.5	19 PG	<4.2	+1	1.8	11.7	4	No
[25] ESSCIRC'05 M	130nm CMOS	3 ~ 5	26 VG	4	-13	1.5	45	4	± 1.5 kV
[26] ISCAS'05 S	130nm CMOS	3 ~ 10.7	11 PG	3	–8.2	1.2	4.8	5	No
[27] ASSCC'05 M	180nm CMOS	0.04 ~ 0.9	20.3 PG	4	–10.8 ~ –12.7	1.8	43.2	0	No
[28] ISCAS'05 S	180nm CMOS	1.5 ~ 2.6	15.4 PG	0.9	–2.5	1.5	11	4	No
[28] ISCAS'05 S	180nm CMOS	3.2 ~ 4.8	17.9 PG	1.6	–4.5	1.5	13.2	4	No
[29] JSSC'05 M	180nm CMOS	2 ~ 4.6	9.8 PG	<5.2	–7	1.8	12.6	3	No
[30] TCAS-I'05 M	250nm CMOS	3.2 ~ 4.8	7 PG	<3.7	4 @ 4GHz	2.5	20	2	No
[31] ISSCC'04 M	180nm CMOS	2.3 ~ 9.2	9.3 PG	5.2	–6.7	1.8	9	5	No
[31] ISSCC'04 M	180nm CMOS	2.4 ~ 9.5	10.4 PG	5.3	–8.8	1.8	9	5	No
[32] MWSCAS'03 S	180nm CMOS	3 ~ 7	15.3 PG	<1.9	N/A	1.8	15	4	No

S: simulation results M: measurement results *: 2.5 V for ESD protection diode PG: power gain VG: voltage gain

IV. SIMULATION RESULTS, DISCUSSIONS, AND BENCHMARKS

The LNA has been extensively characterized in *Cadence* environment with SPECTRE as the simulator. The device dimensions are listed in Table II. The package effects and parasitic capacitances at the input and output nodes have been modeled in all simulations. An extra load capacitor of 0.3 pF is added to account for the input capacitance of the succeeding polyphase I/Q-mixer scheme. The ESD robustness of the RF-input pins to rail is tested using the Human Body Model (HBM) reference circuit [14]. A $\pm$HBM voltage pulse is applied to the LNA's input to induce a large $\pm$ zapping discharge current that has a rising/falling time of $\sim$ 8 ns. Verified in all combinations, the LNA can withstand minimally ± 4 kV of ESD zapping without causing internal or protection devices failure. This result fulfills the standard of "safe level" (i.e., ± 4 kV) in the chip-level ESD specifications.

It would be interesting to compare the effectiveness of the double-current reuse technique to the simple capacitive cross coupling. As shown in Fig. 12, with M_3 serving as an amplification device, there are roughly 1-dB and 3-dB improvements in terms of NF and $A_{v,\mathrm{diff}}$, respectively.

Multiband reception of mobile-TV standards does not pose rigid group-delay variation specification as the bandwidth usage of each standard is relatively small in comparing with that of the LNA. The simulated inband gain delay is 233 ± 21 ps.

The in-band linearity is verified by two-tone tests as shown in Fig. 13. Thank to the cascode-free structure of the LNA and optimal gate–source voltage biasing, high IIP3 of $+10.8$ dBm and -1-dB input-referred compression point (ICP) of -7.6 dBm are concurrently achieved. Other IIP3s among the desired signal band varies between $+10.5$ to $+13.7$ dBm. An out-of-band two-tone test at 2.0 and 2.1 GHz is also conducted (not shown), obtaining an out-of-band IIP3 of $+9.9$ dBm and a -1-dB ICP of -3.5 dBm. Both demonstrate superior linearity performance metrics in this 1.2-V 9.6-mW LNA design. The power-down leakage is 47 μW.

The effects of differential imbalance to the performances of the LNA are simulated. A 10% size mismatch between M_1 and M_2 still maintain the in-band common-mode and supply rejection ratios $>$ 50 dB. Since the LNA is intended to drive an integrated mixer, testing the reverse isolation S_{12} necessitating using a 50-Ω test buffer cannot tell the stability information of the LNA in its true operating condition. Thus, only the reverse voltage gain (i.e., the differential outputs coupled back to the input node) and transient simulation results can help to estimate the stability of the LNA. The simulated in-band reverse voltage gain is < -28 dB. The tolerable C_{L} is up to 1 pF without affecting the targeted $|\mathrm{S}_{11}|$ of -10 dB. These tests give confidence that the LNA will be stable in practice.

As the impact of transistor variability in nanoscale process is continuously increasing, process corner and Monte Carlo (MC) simulations are essential to investigate the robustness of the

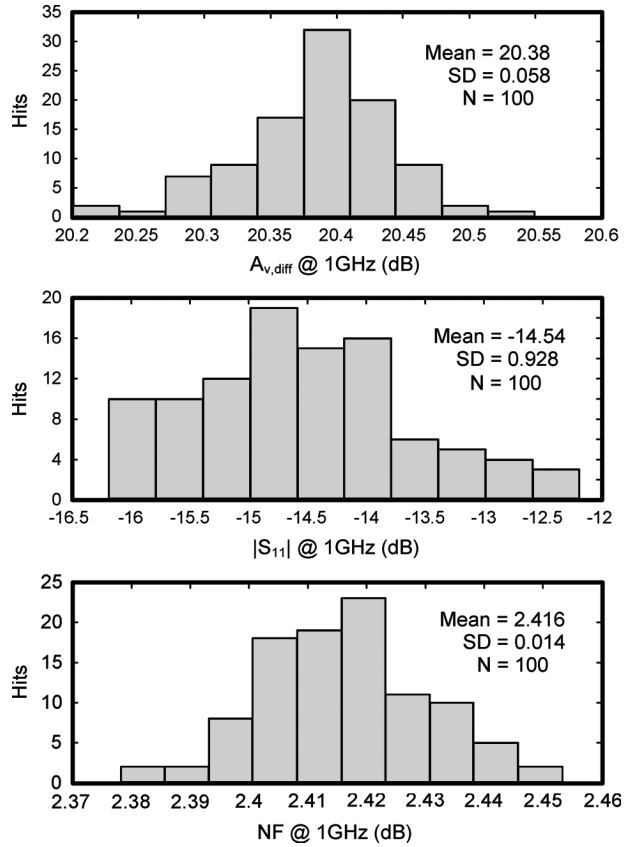

Fig. 17. 100-time MC simulation results of the RF performances.

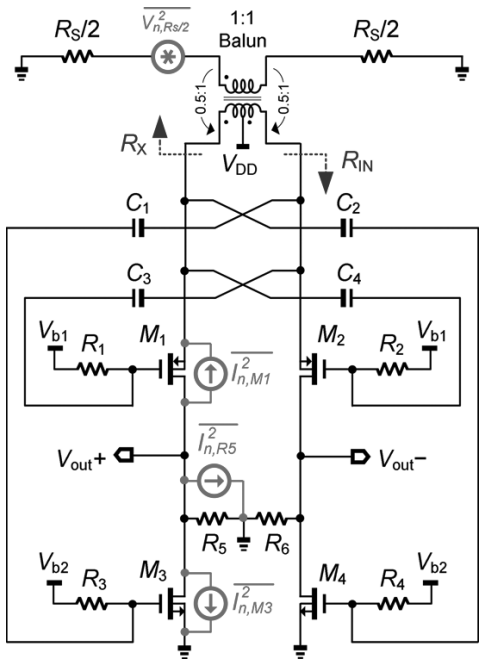

Fig. 18. Noise model of the proposed LNA.

RF performances over PVT. A set of simulation counting the process (Fig. 14), supply voltage (Fig. 15), and temperature (Fig. 16) variations have been conducted. In addition, a set of 100-time MC simulation of the RF performances was done (Fig. 17). These presilicon results rigidly verify the effectiveness of the proposed circuit techniques and the completeness of the design consideration. The LNA will be experimentally verified with the entire TV tuner.

Table III gives a comparison of the proposed LNA with respect to the recently published wideband CMOS LNAs [15]–[32] (design with both simulation and measurement results are considered). It can be observed that most performance metrics of the current design are superior, in particular the voltage gain, power and linearity, even under high ESD protection.

V. Conclusion

An ESD-protected UWB LNA covering 170 to 1700 MHz for full-band mobile TV tuners in a 90-nm CMOS process has been described. ±4-kV ESD robustness at the RF input pins and +10.8-dBm IIP3 have been concurrently achieved by exploiting a 1.2/2.5-V-mixed ESD protection scheme and a pMOS-based open-source input structure. Reliability- and PVT-conscious bias techniques lead to competitive and robust RF performances. The LNA core employed double-current reuse and single-stage thermal-noise cancellation achieves 20.6-dB voltage gain and <2.7-dB NF with 9.6-mW power consumption.

Appendix

The noise factor F of the proposed LNA is calculated by considering first the noise model of the key devices, as shown in Fig. 18. Due to differential symmetry, separating $R_{\rm S}$ into two $R_{\rm S}/2$ resistors and calculating the left-half circuit is sufficient as the noise contribution of M_1, M_3, and R_5 are equal to that of M_2, M_4, and R_6, respectively. The four sources of noise, $R_S/2$, M_3, R_5, and M_1, are given by

$$\overline{V^2_{n,Rs/2}} = 4KT\frac{R_S}{2} \tag{A1}$$

$$\overline{I^2_{n,M3}} = 4KTg_{m3}\frac{\gamma_3}{\alpha_3} \tag{A2}$$

$$\overline{I^2_{n,R5}} = \frac{4KT}{R_5} \tag{A3}$$

$$\overline{I^2_{n,M1}} = 4KTg_{m1}\frac{\gamma_1}{\alpha_1}. \tag{A4}$$

Second, the principle of superposition will be applied to calculate the differential output squared noise current due to each noise source, yielding

$$I^2_{n,Rs/2,diffout} = \left|\frac{2R_{\rm IN}}{R_S+2R_{\rm IN}}\frac{4R_{\rm IN}}{R_S+2R_{\rm IN}}G_mV_{n,Rs/2}\right|^2 \tag{A5}$$

$$I^2_{n,\rm M3,diffout} = \left|I_{n,M3}\right|^2 \tag{A6}$$

$$I^2_{n,\rm R5,diffout} = \left|I_{n,\rm R5}\right|^2 \tag{A7}$$

$$I^2_{n,\rm M1,diffout} = \left|\left(\frac{2R_XR_{\rm IN}}{R_X+R_{\rm IN}}G_m-1\right)I_{n,\rm M1}\right|^2. \tag{A8}$$

R_X in (A8) represents the impedance observing from the LNA's input back to the balun as given by

$$R_X = \left[\left(\frac{2}{1}\right)^2 R_{\rm IN} \Big\| \left(\frac{R_S}{2} + \frac{R_S}{2}\right)\right]\left(\frac{1}{2}\right)^2 = \frac{R_S R_{\rm IN}}{R_S + 4R_{\rm IN}}. \quad \text{(A9)}$$

Finally, F in (7) is obtained by dividing the total output noise power by the noise power of $R_S/2$ as given by

$$F = 1 + \frac{I^2_{n,\rm M1,diffout} + I^2_{n,\rm M3,diffout} + I^2_{n,\rm R5,diffout}}{I^2_{n,\rm Rs/2,diffout}}. \quad \text{(A10)}$$

Theoretically, for a perfectly matched input impedance (i.e., $R_{\rm S} = 2R_{\rm IN}$) and ideal cross-coupling networks ($A_x = A_y = 1$), the noise contribution of M_1 can be fully cancelled in a single stage by setting $g_{m3} = 2g_{m1}$, recalling that $G_{\rm m} = (1 + A_x)g_{m1} + A_y g_{m3}$.

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