Experimental 1-V flexible-IF CMOS analogue-baseband chain for IEEE 802.11a/b/g WLAN receivers

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Abstract: A low-voltage low-power analogue-baseband chain designed for IEEE 802.11a/b/g wireless local-area network (WLAN) receivers is described. It features architecturally a 'two-step channel selection' to complement the radio front-end, and a flexible intermediate frequency (IF) reception capability to alleviate the cancellation of frequency and DC-offset. In circuit implementation, a double-quadrature downconverter based on a 'series-switching' mixer-quad realises a wideband-accurate I/Q demodulation. A 'switched-current-resistor' programmable-gain amplifier (PGA) minimises the bandwidth variation and transient in gain tuning by stabilising, concurrently, the PGA's feedback factor and quiescent-operating point. An 'inside-OpAmp' DC-offset canceller creates area-efficiently a very low cut-off frequency high-pass pole at DC while providing a fast settling of DC-offset transients. Fabricated in a 0.35 μm complementary metal-oxide semiconductor (CMOS) process without resorting to any specialised device, the prototype consumes 14 mW per channel at 1 V. The transient time in a 52-dB gain step is <1 μs and the stopband rejection ratio at 20/40 MHz is 32/90 dB. The error vector magnitudes are -27 and -17 dB for 802.11a/g and b modes, respectively.

1 Introduction

The widespread adoption of wireless local-area network (WLAN) in the past few years has led to the development of multi-band multi-mode WLAN transceivers [1], such that the most accepted protocols (e.g. IEEE 802.11 family [2]) are capable of being supported by a single terminal. Although WLAN system-on-chip (SoC) solutions [3] have been successfully developed in a complementary metal-oxide semiconductor (CMOS) to address this demand, the silicon area ($\sim$45 mm^2) and power dissipation ($\sim$400 mW) are currently still sizable for many embedded systems. Dominated by the digital logic and memory that perform various system-level functions in the physical layer, WLAN SoCs are indeed capable of taking advantage of nanoscale technologies for cost and power reduction [4]. Yet, the thinner gate oxide of nanoscale transistors poses unprecedented challenges to the design of the analogue parts. While a sub-1 V supply needs to maintain device reliability, a relatively large threshold voltage is also necessary to limit the leakage current. A continuous drop of supply-to-threshold voltage ratio is therefore anticipated, rendering the re-use of conventional solutions, which were developed formerly without that precaution, inefficient.

The research basis of the present work lies on the possibility of developing multi-mode transceiver architectures as well as low-voltage operational circuits that will be useful for the full integration of multi-band multi-mode wireless systems [5] in nanoscale technologies in the future. In this paper, we report the design and implementation of an experimental 1-V receiver-analogue-baseband (BB) chain that was designed in compliance with the IEEE 802.11a/b/g standards. Novel architecture and circuit techniques are proposed for CMOS integration, to meet the standard requirements and to overcome the challenges associated with the need of low-power operation under low-voltage constraints.

Although the fabrication remains at 0.35-μm CMOS ($V_{T,n} = 0.52$ V, $|V_{T,p}| = 0.65$ V) the reinforced techniques used lead to the implementation of the lowest-voltage receiver-analogue-BB chain ever reported [6–11]. Moreover, the achieved 14-mW power consumption is also competitive with a state-of-the-art solution [10] designed in 90-nm CMOS, which consumes 13.5 mW at 1.4 V. Consequently, the overall architectural techniques presented and experimentally demonstrated here hold the promise of continuously being effective in the upcoming sub-1 V CMOS technologies [12].

Section 2 briefly summarises the basic features of the IEEE 802.11a/b/g WLAN standards. Section 3 analyses the standards and presents the proposed architectural techniques. The realised analogue-BB chain and its circuit implementation are described in Sections 4 and 5, respectively. Finally, the experimental results are reported in Section 6.

2 IEEE 802.11a/b/g WLAN standards

The IEEE 802.11 family is dedicated to high-speed WLAN communications. Currently, the most relevant physical layers are the 802.11a/b/g. The basic 802.11 mode is seldom used today, although the latest 802.11n will be ratified soon.

This work is focused on the 802.11a/b/g standards. The 11a is based on the orthogonal frequency-division multiplexing (OFDM) technique. It can deliver a high data rate up to 54 Mb/s by using the 64-quadrature amplitude modulation (64-QAM) in the 5-GHz band. For the 11b, it operates

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Table 1: IEEE 802.11 a/b/g characteristics

	802.11a	802.11b	802.11 g
modulation	OFDM: BPSK/QPSK/QAM	DSSS: D-BPSK/D-QPSK/CCK	DSSS: D-BPSK/D-QPSK/CCK OFDM: BPSK/QPSK/QAM
frequency band	5 GHz	2.4 GHz	2.4 GHz
channel bandwidth	16.25 MHz	22 MHz	16.25–22 MHz
bit rate	6–54 Mb/s	1–11 Mb/s	1–54 Mb/s

in the 2.4-GHz band. The complementary code keying (CCK) modulation can deliver a maximum data rate of 11 Mb/s. A mix of the previous mentioned 11a and b is obtained with the 11 g, which supports a data rate up to 54 Mb/s by using the OFDM technique with 64-QAM modulation in the 2.4-GHz band, and it is backward compliant with the 11b for lower data-rate options. Their main characteristics are tabulated in Table 1.

3 Proposed architectural techniques

3.1 Flexible-IF reception for multi-standard compliance

Architecturally, the receiver radiofrequency (RF) front-end experiences no difference between the zero-intermediate frequency (ZIF) and the low-IF (LIF) downconversion. Thus, the analogue-BB chain can flexibly choose the best fit IF for each mode of operation. In this paper, a ZIF–LIF mixed solution is proposed and the justifications to use it are the following.

ZIF is well suited for the 11b/g-CCK mode because of the wideband nature of the channel. DC-offset and $1/f$ noise can be simply removed by using high-pass filters (HPFs) throughout the BB chain. However, it is not that straightforward for the 11a/g-OFDM mode. An improper choice of the highpass pole frequency may result in a significant distortion of those close-to-zero subcarriers. Alternatively, a non-zero IF (e.g. 10 MHz for 11a, 12.5 MHz for 11 g) appears to be more effective since the image-rejection ratio (IRR) requirement at such a LIF value is still practical to achieve (i.e. 30 dB) for an error vector magnitude (EVM) of -25 dB. In addition, a LIF can alleviate the trade-offs encountered by DC-offset cancellation. This idea is illustrated by comparing the ZIF (Fig. 1*a*) and +LIF-to-BB (Fig. 1*b*) downconversion of an OFDM channel. First, comparing with the ZIF–HPF, the cut-off frequency of the LIF/HPF1 can be highly increased, leading to significant area saving, while shortening the receiver settling time in DC-offset transients. Second, since the tolerable instability of the reference crystal is ± 20 ppm, a mixed-mode automatic frequency control (AFC) would be essential for ZIF [13]. The AFC digitally estimates the frequency error (which is as high as 214 kHz at 5.35 GHz), and then compensates it in the analogue domain by offsetting the frequency of the RF local oscillator (LORF) in the same amount. In contrast, a LIF can endure much larger frequency errors at HPF1 (i.e.

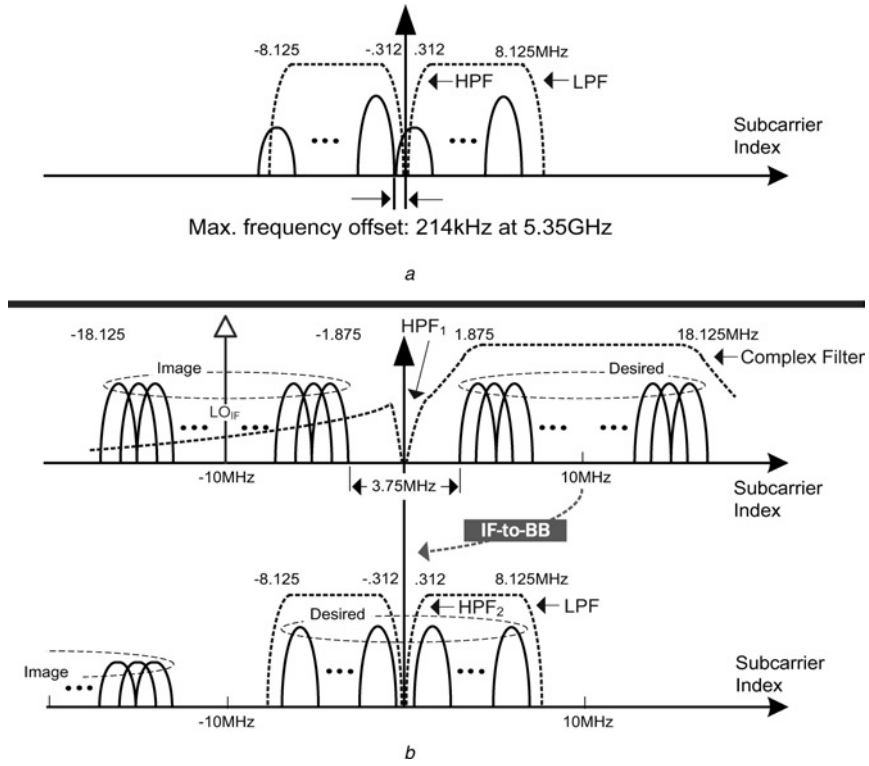

Fig. 1 *Downconversion of 5-GHz band OFDM channel*
a ZIF
b +LIF-to-BB approaches

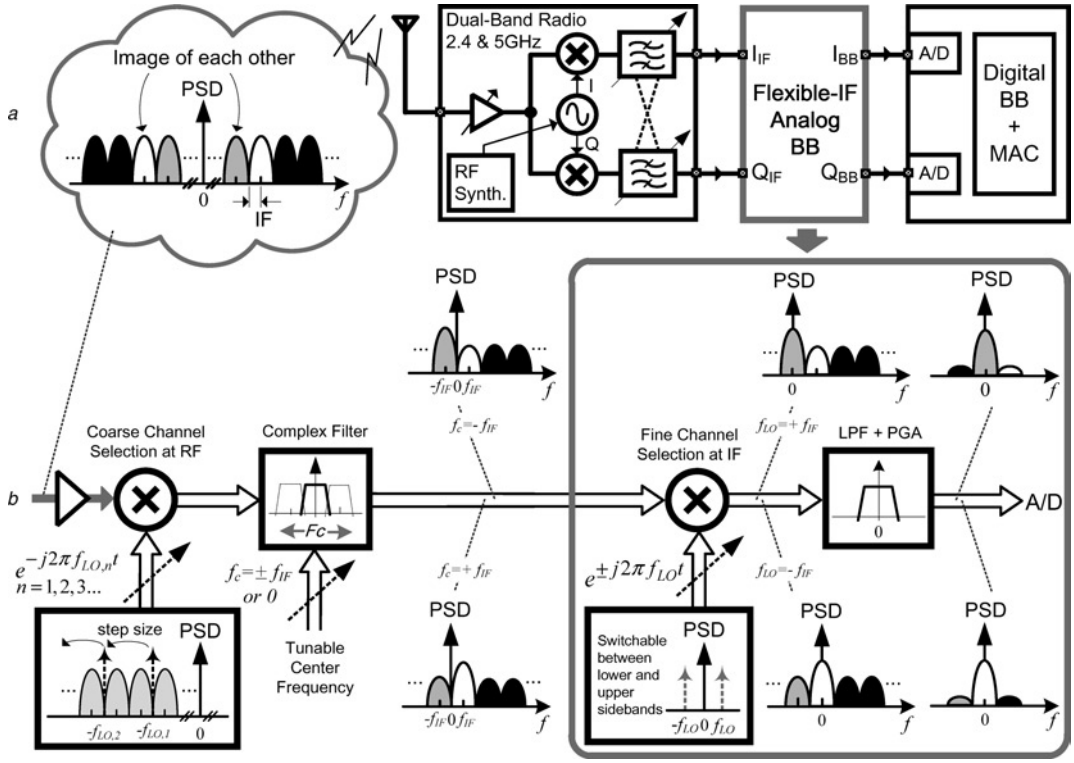

Fig. 2 *Proposed receiver architecture*

a System partition
b Its operation in two different LIF modes: +LIF/−LIF to BB

3.75 MHz). The compensation is therefore possible to be transferred to the IF LO (LOIF), which benefits from the simplicity of a much lower operating frequency (≤12.5 MHz).

3.2 BB-signal conditioning for cost-efficient reconfiguration

The efficiency of the proposed flexible-IF reception is critically determined by the permutation of the functional blocks. The system partition of the proposed receiver architecture is presented in Fig. 2*a*, and its block-level operation is illustrated in Fig. 2*b*. The RF channels after the RF-to-IF downconversion are filtered by a tunable centre frequency (i.e. at +IF, −IF or DC) complex filter [5]. Afterwards, an IF-to-BB downconversion is performed, placing the desired channel at DC before filtering and amplification. With such a permutation, the specifications of the channel-selection low-pass filter (LPF), programmable-gain amplifier (PGA) and even the analogue-to-digital (A/D) converter (that is assumed to be resided in the digital BB) can be maintained in any of the modes therefore maximising block sharing.

3.3 Two-step channel selection for radio front-end simplification

The proposed receiver has two frequency conversions (i.e. RF→ Flexible-IF → BB), allowing the use of 'two-step channel selection' [5] to simplify the RF front-end. This claim is described in Fig. 2*b* as well. In LIF mode, the selected IF (i.e. one-half the channel spacing) implies that the desired channel and its first adjacent are the image of each other. As a consequence of that fact, the RF-to-IF downconversion translates both of them to the identical IF and conjugates their phases. With a tunable centre frequency between ±IF, the complex filter can flexibly pass either the desired channel or its image. The selected channel is then downconverted to DC by using a complex-IF mixer driven by LOIF. Also, LOIF is made switchable between $e^{j2\pi f_{IF}t}$ and $e^{-j2\pi f_{IF}t}$ to perform sideband selection. In brief, this technique allows channel selection at IF without an extra IF frequency synthesiser.

On the other hand, the adoption of such a technique implies a relaxed specification of the RF frequency synthesiser (assuming an integer-*N* type) since this is intended to cover only the frequency range of every channel pair. Applying this concept to the 11a mode, ten LO locking positions are sufficient to cover the 19 channels in the 5.15–5.725 GHz band (Fig. 3). Comparing this with the conventional single-step channel selection, the number of locking positions is almost halved, whereas the LORF step size is doubled (from 20 to 40 MHz). A doubled step size permits the use of a doubled reference frequency to enlarge the loop bandwidth of the phase-locked loop (PLL), and to reduce the modulus of the division ratio. The former shortens the PLL settling time and lowers the LORF in-lock phase noise, whereas the latter lowers the LORF close-in phase noise. The trade-offs of designing an RF frequency synthesiser can be found in [14].

4 Proposed analogue-BB chain

The functionality and feature of each block are presented briefly here first, whereas the implementation details are given in Section 5.

Fig. 4 shows the block diagram of the implemented analogue-BB chain. The dual-mode preselect filter features a single/double-channel BW for the ZIF/LIF mode. Its main function is to prevent the residual in-band channels,

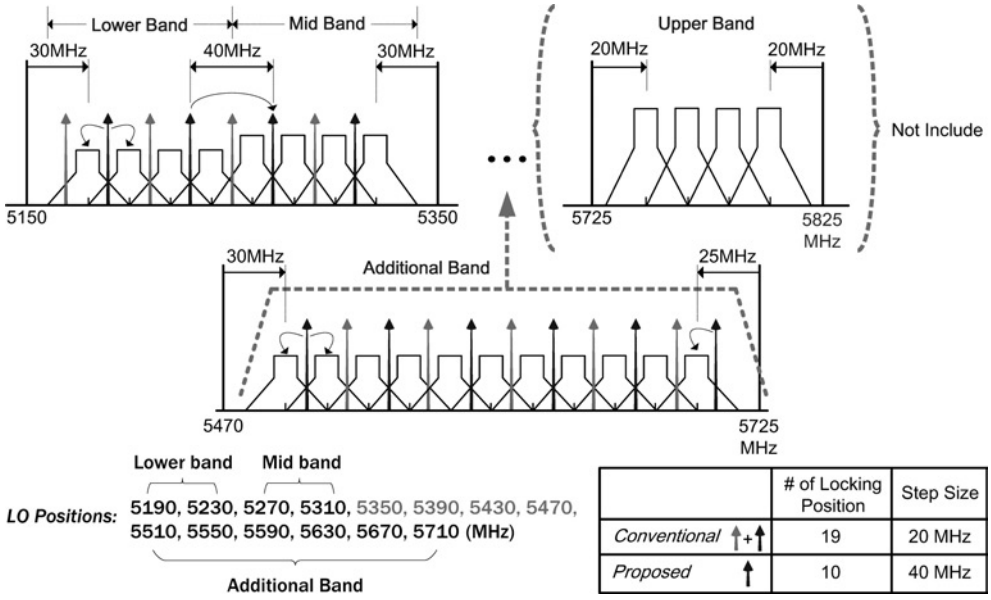

Fig. 3 *5-GHz LO plan with and without using two-step channel selection*

and out-of-band white noise, from folding back into the signal band in the subsequent mixing. The double-quadrature downconverter (DQDC) is made up of a series-switching mixer-quad. The mixing signal is generated by a digital clock generator (CLKGEN), which has a clock-rate-defined output to match different IFs. The cooperation of such DQDC and CLKGEN realises a wide-band and mismatch-insensitive I/Q demodulation.

In order to complete the second step of channel selection, the output of the DQDC is designed to have a sideband selection feature [i.e. switch the phase (0°, 180°) of its I/Q-coupled paths]. Since the downconversion is performed preceding the filtering and amplification, the reconfiguration needed for the mode switching involves just two simple reconfigurations: that is, double/halve the BW of the preselect filter and enable/disable the DQDC and CLKGEN for the LIF/ZIF mode, respectively.

With ZIF or LIF receiver architecture, the signal levels arriving at the BB are scaled to the vicinity of 0 dBm for the A/D conversion. The dynamic-range requirement of 802.11a/b/g from the antenna to the BB is ~0–80 dB, with the majority of this gain provided in the BB. Assuming the RF front-end offers a 0–30 dB gain range, the BB, LPF and PGA have to provide another 0–50 dB of controllable gain. In practice, although a cascade use of multiple PGAs can attain such a high-gain range, the PGA has to feature an excess BW, roughly ten times wider than that of the LPF to ensure that the selectivity is stable against the gain. The proposed switched-current-resistor (SCR) PGA is to address this issue. It realises a constant-BW transient-free gain control to minimise the BW requirement of the PGA and enhances its settling time in gain change. The reduced BW also enhances the stopband rejection, resulting in a 2-fold relaxation of the LPF's order from the fifth to third.

The DC-offset can easily saturate the LPF and the PGA because of a large cascaded gain. In the 11b/g-CCK mode, the composite high-pass pole must have a value close to tens of kilo Hertz to prevent deeply damaging the signal. Therefore the resulting chip area impact would be very

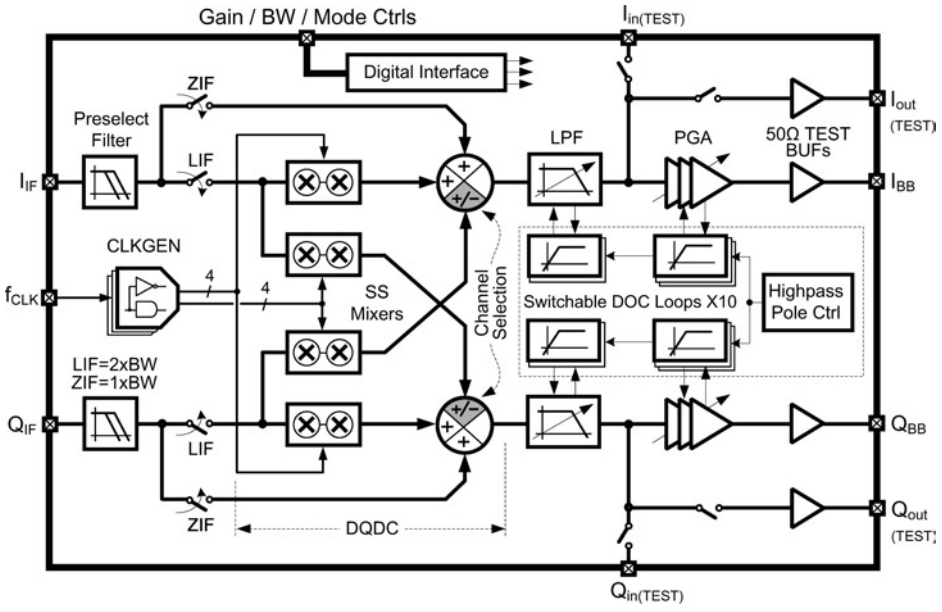

Fig. 4 *Architecture of the analogue-BB chain*

large and a long DC-offset transient in the automatic gain control (AGC) can occur. To eliminate this drawback, this paper introduces an inside-OpAmp DC-offset canceller (DOC) for area savings and switchability. A switchable high-pass pole is created inside each LPF's and PGA's OpAmp, by which the differential signals are locally balanced and the composite high-pass pole is agilely switchable during the AGC (just 5.6 μs is allowed in the physical layer convergence protocol preamble field). The receiver settling time is therefore only governed by the AC-coupler (not shown) that eventually interfaces the PGA to the A/D converter (mostly, 9-bit resolution [15]). The AC-coupler has an extended lower −3 dB point of 1 MHz to receive only the pilot tones. In the ZIF mode, all DOCs are switched on but maintain a composite lower −3 dB point < 10 kHz. This low-frequency value ensures a low intersymbol interference in processing the CCK channel.

The gain, BW and operating mode are all controlled digitally. A built-in setup and additional 50-Ω test buffers enable both full-chip and functional-block measurements.

5 Circuit implementation

5.1 Preselect filter, DQDC and CLKGEN

The schematics of the I-channel (Q-channel is identical) dual-mode preselect filter and DQDC are shown in Fig. 5*a*. The front-end resistor-capacitor (i.e. R_{PF} and C_{PF}) matrix offers single-pole preselect low-pass filtering and linear voltage-to-current conversion. The value of R_{PF} determines the noise figure (NF) of the entire analogue-BB chain. With $R_{PF} = 2.5\ k\Omega$, the desired NF specifications (< 30 dB) are safely met.

The DQDC has a double-balanced structure to cancel the unwanted I/Q demodulating carrier at the output. Using the clock phases of the timing diagram from Fig. 5*b*, the co-switching of the swapper and S_M switches produce two quasi-I/Q sequences with a normalised amplitude, that is, $I = [\ldots 1,\ 0,\ -1,\ 0\ldots]$ and $Q = [\ldots 0,\ 1,\ 0,\ -1\ldots]$ and their frequency is a quarter of the reference clock (CLK). The reset-switch S_{RS} is activated during swapping of the differential branches for minimisation of the conversion loss and memory effect.

The conversion gain (CG) of this switching mixer is determined by the duty cycle δ as given by

$$CG = \frac{2}{\pi}\sin(\pi\delta) \tag{1}$$

In this work, the duty cycle is 25%, implying a CG of 0.45. Although this attenuation can rise its input-referred NF by 7 dB, the standard-recommended NF of 14 dB can still be safely met by adopting an RF front-end with a 30-dB gain and a 5-dB NF [13]. They jointly yield an overall receiver NF of 8.5 dB.

Linearity is determined by two factors: (i) the ratio of RPF to the overall on-resistance of the swapper and SM and (ii) the overdrive voltage of the switches. Here, r_{on} is 213 Ω (8.5% of RPF) such that a third-harmonic distortion of −80 dB is guaranteed. Moreover, to maximise the overdrive voltage under a low-voltage supply of just 1 V, the differential virtual ground is biased to a value very close to ground (i.e. 0.1 V) by means of an input common-mode feedback circuit (CMFB).

The clock phases are generated by the digital circuitry shown in Fig. 6. A 40/50-MHz CLK generates a 10/12.5-MHz pseudo-I/Q waveform through the multiplication of the main and auxiliary phases in the analogue domain. The main phases are co-generated by two D-flip-flops (D-FFs), D1 and D2, and a pair of non-overlapping clocks that have a matched duty cycle. The required 90° phase shift is generated in the auxiliary clock by inserting an inverter N1 between D3 and D5. It is noted that the N1 induces a minor phase error as the auxiliary clock swaps the inverse terminals recursively at zero-crossings. A global reset initialises all D-FFs at startup. Finally, the IF

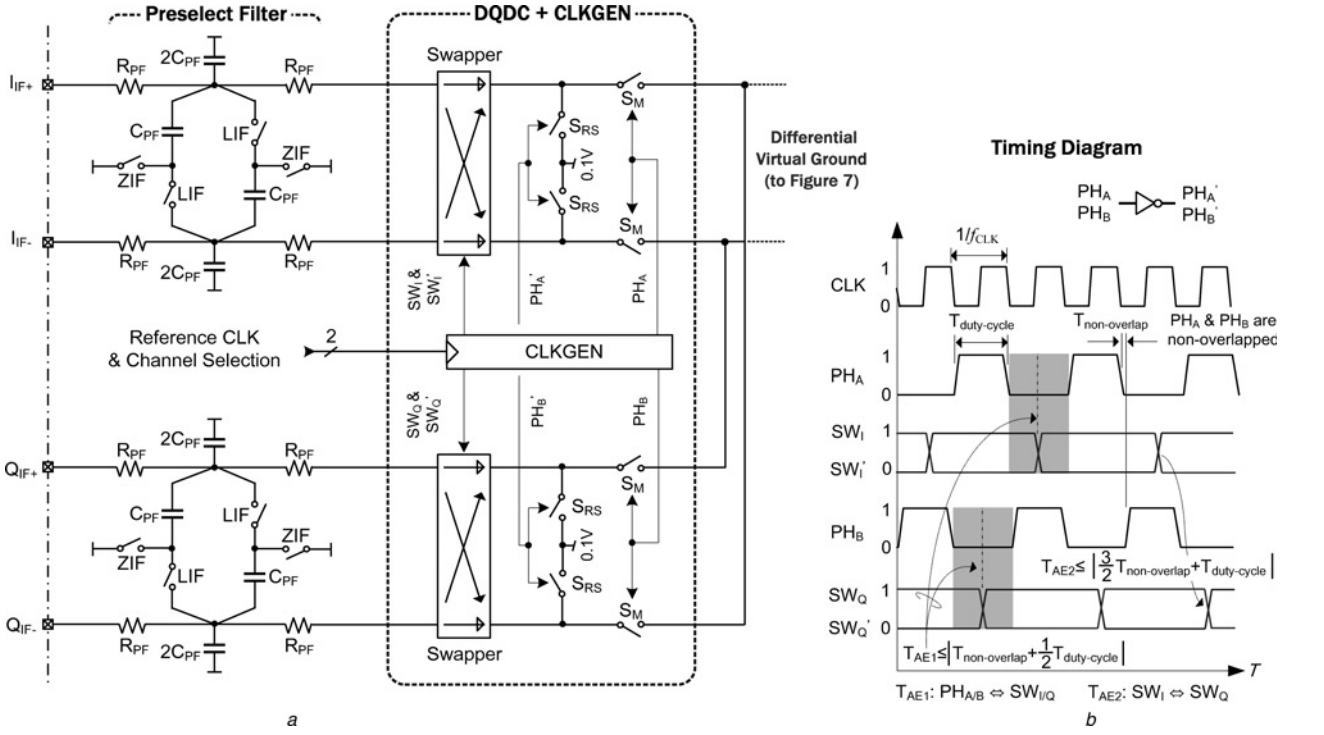

Fig. 5 *I-channel preselect-filter, DQDC and CLKGEN*

a Schematics
b Timing diagram of the DQDC

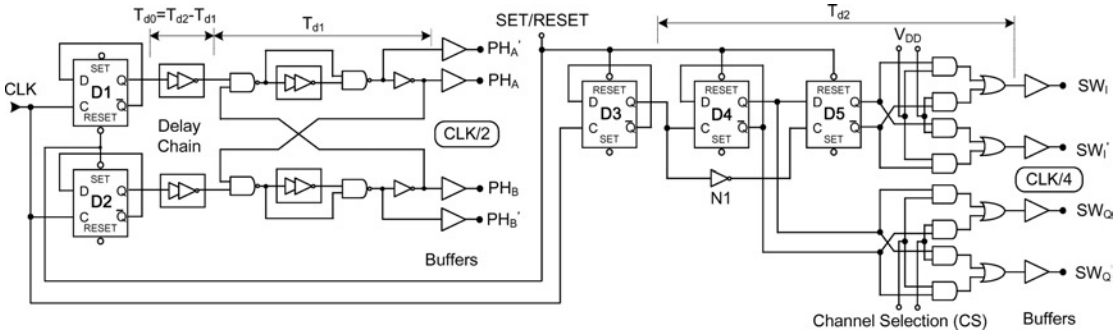

Fig. 6 *Schematic of the CLKGEN*

channel selection is executed by switching the phases between SW_Q and SW_Q'.

In addition to the main features mentioned, other advantages of the proposed DQDC and CLKGEN are also worth emphasising: (i) the duty cycle variation of the CLK only produces an amplitude mismatch between I and Q outputs and does not affect the phase; (ii) because the waveforms of I/Q sequences are non-overlapping and are always return-to-zero, the orthogonal relationship is still exact against a large timing error (i.e. $T_{AE1} \leq 25/20$ ns and $T_{AE2} \leq 50/40$ ns for 10/12.5-MHz IF as shown in Fig. 5*b*). This nature ensures that I/Q demodulation is wideband-accurate and mismatch insensitive; (iii) as the swapper is only activated when S_M is in open state, the charge injection from the swapper and self-mixing (in the overall circuit) are avoided. Of course, S_M itself induces charge injection, but it is out of the signal band (i.e. two times the IF); (iv) because the preselect-filter exhibits a symmetric low-pass function between its input and output terminals, the swapping-induced charge that couples back to the RF front-end can also be suppressed, improving the reverse isolation.

Although the tolerable timing error of the proposed DQDC is the same as that in [16], the current design features a higher CG of 0.45 (0.24 in [16]) while requesting a lower CLK rate of 4-fold the IF value (8-fold in [16]).

5.2 Channel-selection filter and PGA

The block schematics of the implemented channel-selection LPF and PGA are depicted in Fig. 7. A third-order Butterworth active-RC LPF (1 uniquad plus 1 biquad with $Q = 1.3065$) in conjunction with a 3-stage 17-MHz-constant-BW PGA provides the required selectivity and a controllable gain range from -2 to 50 dB with a 2-dB step size. Two coarse-stages (6-dB step size) followed by a fine-stage (2-dB step size) gain controls optimise the gain-switching transients in the PGA. Through iterative simulations and with a positive zero (R_{ff} and C_z) added to the PGA's third-stage, the optimised (through simulation) group-delay peaking at the band edge is 14.8 ns. The resistor RBW is a resistor array for tuning the BW digitally with a 5-bit control word.

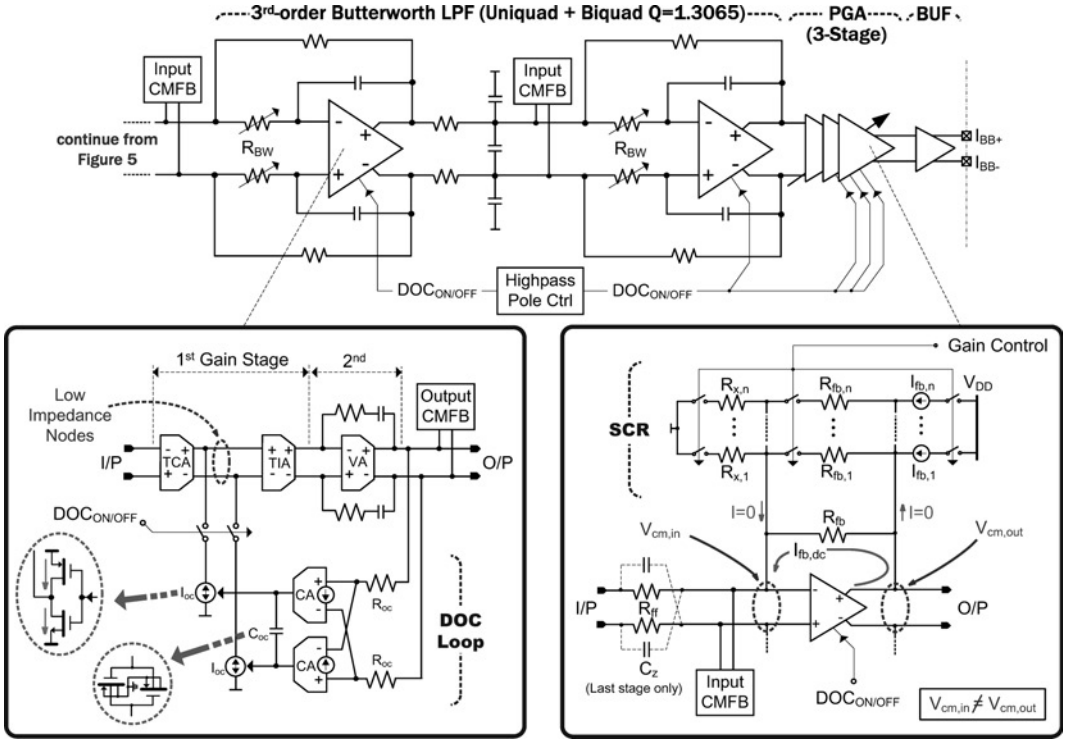

Fig. 7 *I-channel channel-selection LPF and PGA*

Lower-left: OpAmp with built-in DOC loop
Lower-right: one stage of the SCR PGA

To operate the OpAmp at a minimum supply voltage, the common-mode voltage of its virtual ground ($V_{cm,in}$) has to be near to one of the supply rails (here: $V_{cm,in} = V_{DD}/10 = 0.1$ V) [17]. This constraint will create transients in gain tuning since the output common-mode voltage of the OpAmp ($V_{cm,out}$) must be in mid-rail of the supply for maximum output swing (here: $V_{cm,out} = V_{DD}/2 = 0.5$ V). To tackle this problem, a current-source bank [$I_{fb,1}$, ..., $I_{fb,n}$] and a resistor bank [Rx,1, ..., Rx,n] are added. The former replaces the OpAmp to deliver the gain-dependent DC current for the gain-tuning resistors [$R_{fb,1}$, ..., $R_{fb,n}$], whereas the latter sinks the same current out from the virtual ground. The whole operation is governed by

$$I_{fb,n} = \frac{V_{cm,out} - V_{cm,in}}{R_{fb,n}} = \frac{V_{cm,in}}{R_{x,n}} \text{ for } n = 1, 2, 3, \ldots \quad (2)$$

and the feedback resistor R_{fb} can be successfully isolated from the gain switching elements. A stable DC current $I_{fb,DC}$ maintains the DC operating points of the OpAmp, with input and output CMFBs unchanged over gain, thereby leading to a transient-free gain control.

To ensure the operation is robust over process, voltage and temperature (PVT) variations, the references of [$I_{fb,1}$, ..., $I_{fb,n}$], $V_{cm,in}$ and $V_{cm,out}$ (i.e. [$I'_{fb,1}$, ..., $I'_{fb,n}$], $V_{ref,in}$ and $V_{ref,out}$, respectively) are generated by an on-chip resistor-to-current (R-to-I) converter (Fig. 8). This contains an error amplifier A_{error} operating in a feedback loop to track the absolute value of R_3 under a fixed voltage Vz. The corresponding reference current $I_{fb,ref}$ is therefore $\propto 1/R_3$. Vz is a mirror of Vx that is set to 0.1 V ($V_{DD}/10$), enabling A_{error} to be a simple p-channel differential pair. The R_3-tracked $I_{fb,ref}$ is then mirrored to the switched current sources [$I'_{fb,1}$, ..., $I'_{fb,n}$] through transistors M_1 to [$M_{b,1}$, ..., $M_{b,n}$], which features the same ratios of $R_{fb,1}$ to [$R_{fb,1}$, ..., $R_{fb,n}$]. Normalising $R_{fb,1}$ as the basic elements among [$R_{fb,1}$, ..., $R_{fb,n}$] implies that [$I'_{fb,1}$, ..., $I'_{fb,n}$] become a function of R_3, that is

$$I'_{fb,n} = \frac{V_z}{R_3}\left(\frac{R_{fb,1}}{R_{fb,n}}\right) \text{ for } n = 1, 2, 3, \ldots \quad (3)$$

The next step is to involve [$R_{fb,1}$, ..., $R_{fb,n}$] in (3) such that $I'_{fb,n} \propto 1/R_{fb,n}$. Matching R_3 to $R_{fb,1}$ with $R_3 = R_{fb,1}/4$ simultaneously meets that goal and equalises the numerator of (3) to that of the second term in (2) (i.e. $4Vz = V_{cm,out} - V_{cm,in}$), yielding

$$I'_{fb,n} = \frac{4V_z}{R_{fb,n}} \text{ for } n = 1, 2, 3, \ldots \quad (4)$$

Substituting (4) back to the first term of (2), and replacing $R_{fb,n}$ and $R_{x,n}$ according to $\alpha_n R_u = R_{fb,n} = 4Rx,n$ for $n = 1, 2, 3, \ldots$(where R_u denotes the unit resistor and αn is a positive integer representing a resistive ratio), a practical expression of (2) can be obtained, that is

$$\frac{4V_z}{\alpha_n R_u} = \frac{V_{cm,out} - V_{cm,in}}{\alpha_n R_u} = \frac{V_{cm,in}}{\alpha_n/4R_u} \text{ for } n = 1, 2, 3, \ldots \quad (5)$$

Recalling that Vz, $V_{cm,out}$ and $V_{cm,in}$, respectively, are mirrors of Vx ($V_{DD}/10$), $V_{ref,out}$ ($V_{DD}/2$) and $V_{ref,in}$ ($V_{DD}/10$), the error voltage ($V\Delta$) associated to V_{DD}, and the error resistance ($R\Delta$) associated to R_u, induce no effect on the balancing of (5) as given by

$$\frac{4(V_{DD} \pm V_\Delta)/10}{\alpha_n(R_u \pm R_\Delta)} = \frac{(V_{DD} \pm V_\Delta)/2 - (V_{DD} \pm V_\Delta)/10}{\alpha_n(R_u \pm R_\Delta)} = \frac{(V_{DD} \pm V_\Delta)/10}{\alpha_n/4(R_u \pm R_\Delta)} \quad (6)$$

As a result, the SCR is made PVT-insensitive.

The static and dynamic performances of the SCR technique are further improved by applying the following circuit practices: (i) The current mirroring, M_1 to [$M_{b,1}$, ..., $M_{b,n}$], is improved in precision by adding R_4 where $R_4 = R_3(V_D - V_z)/V_z$, level-shifting the drain voltage (V_D) of M_1 to that of [$M_{b,1}$, ..., $M_{b,n}$]. (ii) The overall resistor matching, and the ground-noise rejection of A_{error} and A_{ref} (A_{ref} forms a non-inverting amplifier for buffering $V_{ref,out}$), become better by selecting $R_1 = R_2/9 = R_3 = R_4/4 = R_5 = R_6/4$, and limiting the resistor spread to 9. (iii) [$I'_{fb,1}$, ..., $I'_{fb,n}$] are switched through [$M_{s,1}$, ..., $M_{s,n}$] rather than [$M_{b,1}$, ..., $M_{b,n}$] such that [$M_{s,1}$, ..., $M_{s,n}$] obtain the maximum overdrive voltage, leading to reduced device sizes and thereby charge injection. Moreover, since only the current paths are opened, the gate-to-source capacitance of [$M_{b,1}$, ..., $M_{b,n}$] are kept charged for a faster turn-on time. (iv) Connecting the bodies of [$M_{b,1}$, ..., $M_{b,n}$] to V_{DD} prevents the charge injection of [$M_{s,1}$, ..., $M_{s,n}$] from coupling to their gates through their body-to-gate capacitance, yielding 200–300% (depending on the gain step) shorter transient settling time in simulation.

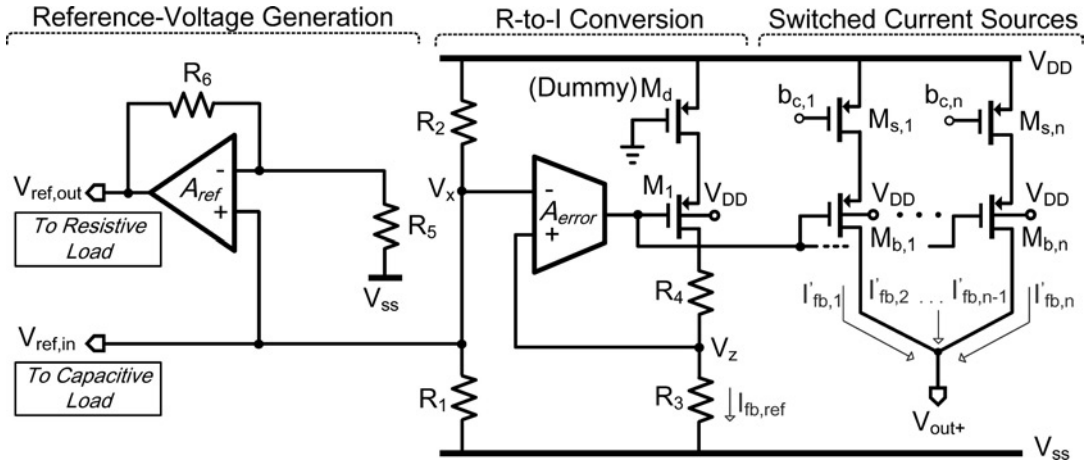

Fig. 8 *R-to-I converter for generating the reference voltage and switched current sources*

The second property (i.e. constant BW gain control) of the SCR PGA is related to its feedback factor β_{PGA} as given by

$$\beta_{PGA} = \frac{1}{1 + (R_{fb}//R_{fb,1} \cdots //R_{fb,n}/R_{ff}//R_{x,1} \cdots //R_{x,n})} \quad (7)$$

where it is possible to observe that by keeping the ratio of $[R_{fb,1}, \ldots, R_{fb,n}]$ to $[R_{x,1}, \ldots, R_{x,n}]$ identical to that of R_{fb} to R_{ff}, a stable β_{PGA} can be achieved. Considering this request together with (2), a transient-free and constant-BW gain control can be simultaneously achieved under the following two conditions, that is

$$\frac{R_{fb}}{R_{ff}} = \frac{R_{fb,n}}{R_{x,n}} \leq \frac{V_{cm,out} - V_{cm,in}}{V_{cm,in}} \quad \text{for } n = 1, 2, 3, \ldots \quad (8)$$

and

$$\beta_{PGA} \leq \frac{V_{cm,in}}{V_{cm,out}} \quad (9)$$

A simple example illustrates this concept: with a 1 V supply, the $V_{cm,in}$ and $V_{cm,out}$ are set to 0.1 and 0.5 V, respectively. To offer a gain range of -12 to 12 dB with a 6-dB step size, we set $R_{fb} = 4R_{ff}$ and $4R_{x,3-n} = R_{fb,3-n} = 2^n R_{ff}$ for $n = -1, 0, 1, 2$, resulting in a constant β_{PGA} of 0.2 while satisfying (2) for a transient-free operation. Without applying this technique, β_{PGA} can vary between 0.2 (at 12 dB) and 0.8 (at -12 dB), which is equivalent to a 4-fold BW variation.

5.3 OpAmp and DOC

Inherent to negative feedback is the imposition to an OpAmp in closed-loop of a BW extension [18]. Considering such a property in the design of the DOC, each OpAmp is internally made highpass prior to closed-loop use, such that its high-pass pole will be shifted to a lower frequency by the loop gain. Thus, instead of using area to realise the time constant, a very low cut-off frequency DOC can be attained.

The circuit structure of the proposed OpAmp with DOC is shown in Fig. 7. Since the DOC loop has to be switchable for fast DC-offset transients, the feedback node is selected in between the transconductance (TCA) and transimpedance amplifiers. Together they form the first gain stage of the OpAmp to drive the second stage voltage amplifier, while offering a low-impedance level at their interface that is important to minimise the switching transient of the DOC. Moreover, since the DOC is preceded by the TCA and is operated inside the OpAmp, its induced noise can be effectively lowered by the TCA and the loop gain. The DOC is realised by two balanced current amplifiers (CAs) and a differential capacitor (C_{oc}). By using a resistive input (R_{oc}), the CAs can directly absorb the high swing output signal from the OpAmp. The transistor-level implementation is summarised next.

Figs. 9*a* and *b* show the schematics of the OpAmp and DOC, respectively. $A_1(s)$ is a p-channel differential pair. The gate of M_1/M_2 is biased at one V_{DSsat} (0.1 V), implying that the minimum supply voltage (V_{DD}) is around 1 V (i.e. $V_{DD} \geq |V_{T,p}| + 2V_{SDsat} + V_{DSsat}$). A cross-coupled active load (M_{3A}/M_{3B} and M_{4A}/M_{4B}) [19] forms a wideband n-channel folded-cascode intermediate stage. $A_2(s)$ is a common-gate amplifier (M_5/M_6). Its low-input impedance (at x_{L^+}) offers a good current summation node for the

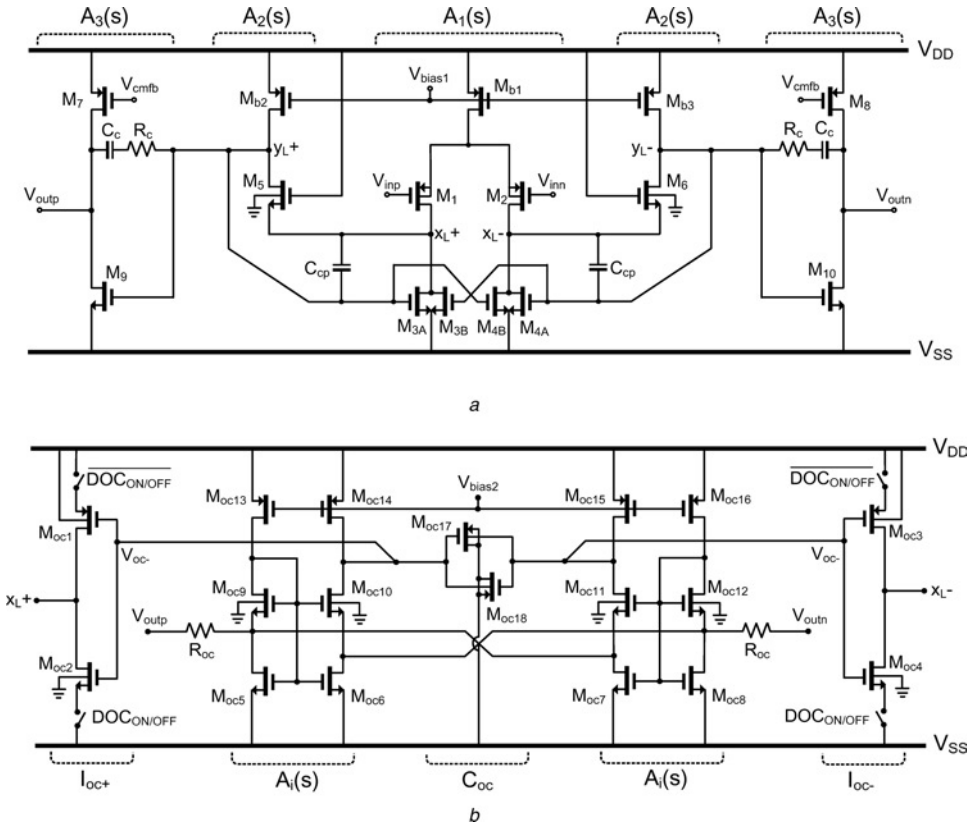

Fig. 9 *Full-circuit schematics*

a OpAmp
b DOC

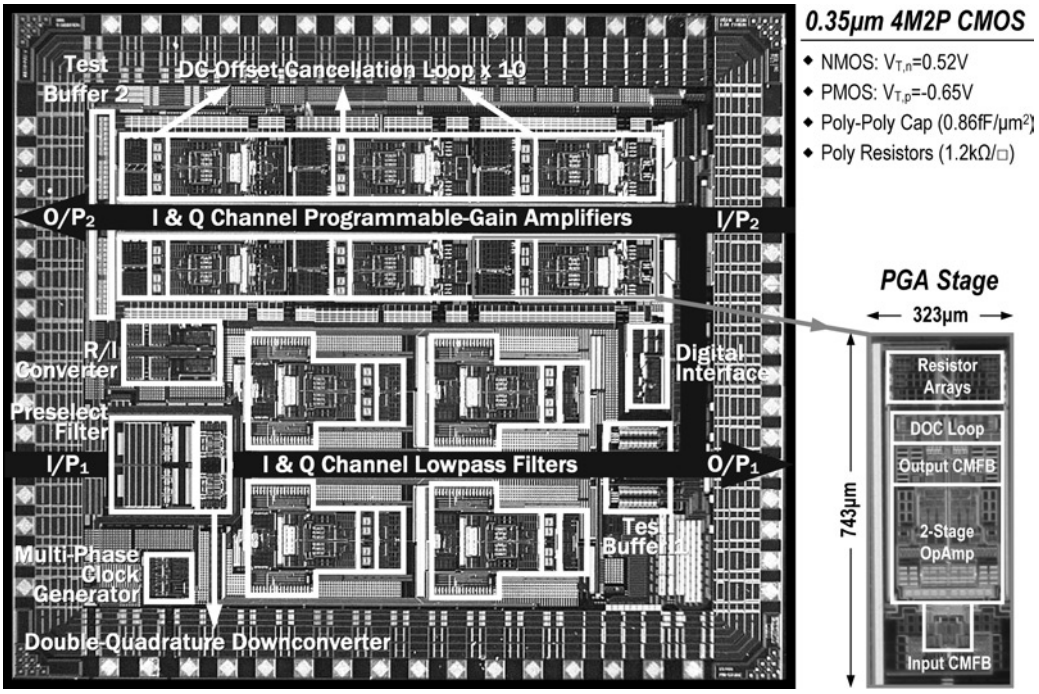

Fig. 10 *Chip micrograph*

DOC. On the other hand, its output impedance at y_{L+} is high only for the differential signal, eliminating the need of common-mode control at that node. Thus, only the final-stage common-source amplifier $A_3(s)$ is involved in the output CMFB, resulting in better stability. The phase margin is optimised by adding C_{cp} in $A_2(s)$ and adding R_c and C_c (i.e. Miller compensation) in $A_3(s)$.

To realise a large time constant, in the order of 0.1 ms, two circuit techniques are applied to the DOC: (i) the first comprises the use of self-biased subthreshold cascode current mirror to realise the $A_i(s)$. As shown in Fig. 9*b*, M_{oc5} and M_{oc6} are biased in the saturation region to absorb the DC current (~10 µA) from V_{outp} and V_{outn}, respectively. Owing to the body effect associated with M_{oc9} and M_{oc10}, they can simply be biased into the subthreshold region by using long channel length devices for M_{oc13} and M_{oc14}. It is known that a subthreshold-biased MOS transistor offers a very high intrinsic DC gain that is independent of device geometry [20], making it highly appropriate to realise a large time-constant integrator on-chip; (ii) A sink-/source-exchangeable charge pump (M_{oc1}–M_{oc2}) serves as the output stage, to relax the linearity requirement of $A_i(s)$ and to reduce the signal swing applied at C_{oc}. Low signal across C_{oc} allows it to be implemented by weakly nonlinear depletion-mode MOS capacitors (M_{oc17} and M_{oc18}) for further area savings (a 9-fold reduction in area is achieved when compared with poly–poly capacitors).

6 Experimental results

The prototype is fabricated in a 0.35-µm CMOS process. The chip micrograph is shown in Fig. 10. Dual channels (I and Q) are integrated differentially with 3-mm^2 core

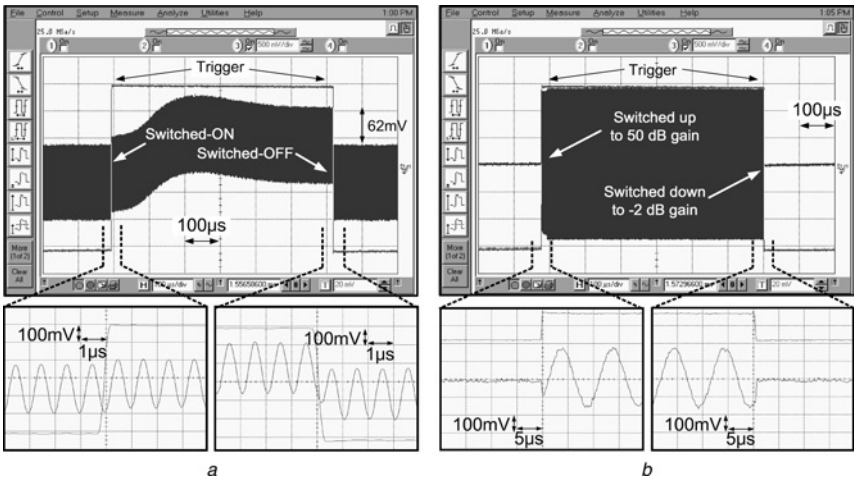

Fig. 11 *Dynamic performance*
a DOC-loop switching
b Gain switching

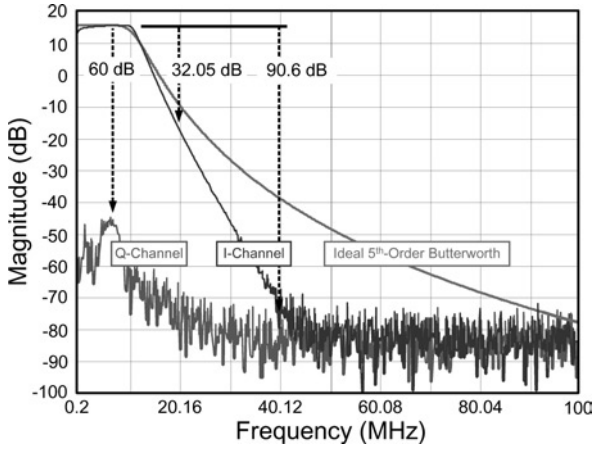

Fig. 12 *I/Q isolation test and stopband rejection ratio*

size. Each channel consists of five 0.02-mm^2 DOC loops distributed inside each LPF's and PGA's OpAmp. The supplies are bred through separated pins for the analogue and the digital parts while using a common ground with on-chip MOS capacitors for decoupling.

The dynamic performances of the implemented analogue-BB chain are characterised in three different ways to demonstrate its compliance with the standards: that is, all tuning operations must be settled within 5.6 μs out of the short preamble field. Fig. 11*a* shows the switching of the DOC loop, where a negligible transient settling at the start and stop slots is observed. For the gain tuning, as shown in Fig. 11*b*, the gain-switched transient in a 52-dB gain step settles within 1 μs. The last test is the channel-selection transient, which is measured to be 0.38 μs (not shown).

In the frequency domain, I/Q channel isolation is measured to be >60 dB (Fig. 12) by applying the test source only at one channel while measuring both. Fig. 12 also shows the achieved stopband rejection ratio at the adjacent (32 dB at 20 MHz) and alternate (90 dB at 40 MHz) channels. Both values safely meet the 11a/g-OFDM mode: 16 dB at 20 MHz and 32 dB at 40 MHz. However, additional filtering would be necessary in the digital domain for 11b/g-CCK mode [21] since the demanded adjacent channel rejection is 35 dB.

We account the image rejection by measuring the mismatches of the I and Q channels. The gain/phase mismatches are measured to be 0.17 dB/0.39° and 0.16 dB/0.7° for 11a/g, respectively. Those results correspond to an averaged IRR of ~40 dB over the entire signal band, which is much better than the targeted 30 dB (Section 3.1).

System performances are measured with modulation signals to test the conformity of the analogue-BB chain. Fig. 13*a* shows the constellation diagram and EVM results of 11a/g mode by injecting a 54-Mps, −31.8-dBm, 64-QAM OFDM signal. It measures an EVM of −27.03 dB (4.45%) that meets the standard allowed −25 dB (5.6%) with a good enough margin. Similar results of the 11b mode (Fig. 13*b*) are measured by using an 11-Mps, −32.7-dBm, DSSS-CCK signal as the test source. It achieves an EVM of −17.04 dB (14.07%), which also satisfies well the standard allowed −9 dB (35.5%).

The main performance metrics are summarised in Table 2, and the block-level measurement results are summarised elsewhere [22].

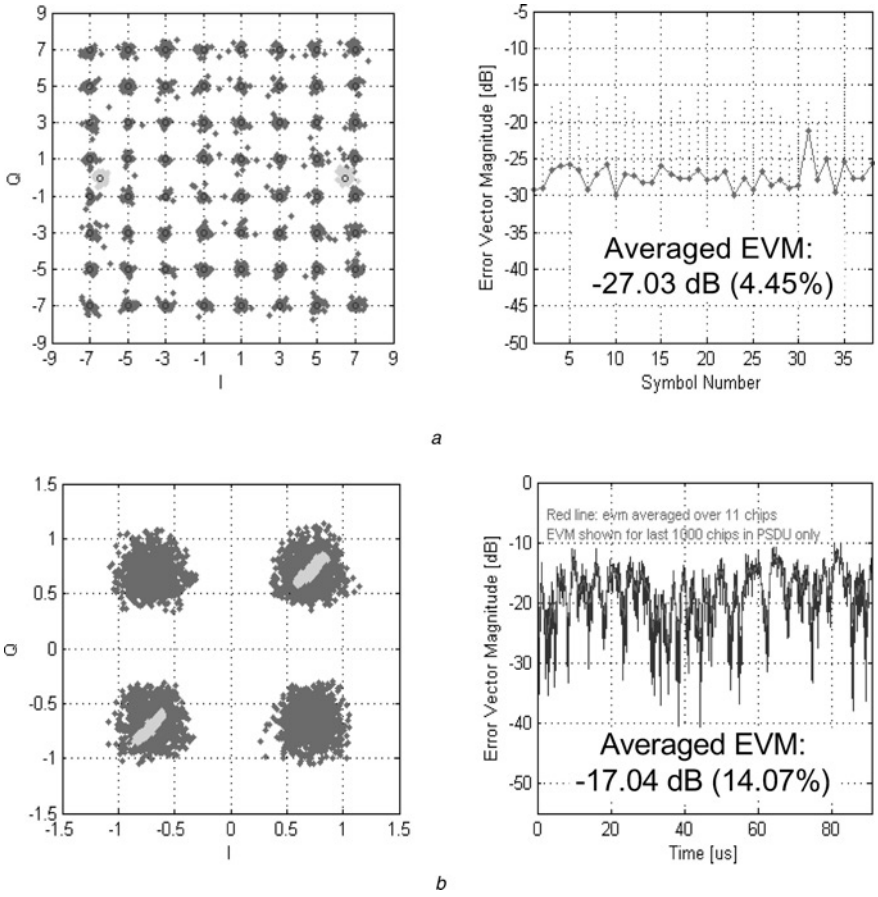

Fig. 13 *Constellation diagram and EVM*

a 11a/g mode: OFDM signal
b 11b mode: CCK signal

Table 2: Chip summary

Parameter		Value
supported intermediate frequencies for 802.11a/b/g		10/0/12.5 MHz
supported modulations/bands	802.11a	OFDM/5.15–5.725 GHz
	802.11b	CCK/2.40–2.58 GHz
	802.11g	OFDM, CCK/2.40–2.58 GHz
power supply		1 V ±10%
voltage-gain range		−2 dB · · · +50 dB (2 dB/step)
upper/lower −3 dB point (upper one is tunable)		6.54–8.95 MHz/3 kHz
standard deviation (σ) of upper/lower −3 dB point over 52 dB gain range		8.6/12.4 %
gain-switched transient time (tested by a 52 dB gain step)		<1 μs
IF channel-selection transient time		0.38 μs
in-band IIP3 at minimum gain (referred to 50 Ω)		+15.2 dBm
stopband rejection at 20/40 MHz offset frequency (8.5 MHz BW, maximum gain)		32.05/90.6 dB
EVM – OFDM/CCK mode		−27.03/−17.04 dB
I/Q Isolation		>60 dB
averaged in-band I/Q impairment in 802.11a/g mode	amplitude	0.175/0.158 dB
	phase	0.39/0.7°
input-referred white noise spectral density/noise figure (white)		22.5 nV/√Hz/< 30 dB
power per channel at 0.9/1/1.1 V (excluded the test buffers)		13/14/16.5 mW
technology		0.35 μm 4M2P CMOS
active core area (I/Q PGAs + I/Q LPFs + preselect filter & DQDC + CLK + other blocks)		3.06 mm^2 (1.44 + 1.12 + 0.25 + 0.05 + 0.2)

Table 3: Brief comparison of state-of-the-art analogue-BB chains

	Elwan *et al.* [6]	Jussila *et al.* [7]	Elwan *et al.* [8]	Lee *et al.* [9]	Elmala *et al.* [10]	This work
applications	GSM/DECT	WCDMA	Bluetooth	ZigBee	802.11a/b/g WLAN	802.11a/b/g WLAN
supply voltage	3 V	2.7 V . . . 3 V	3 V	1.8 V	1.4 V	1 V
power per channel	4.47 mW	58.5 mW	3.6 mW	2.43 mW	13.5 mW	14 mW
input-referred noise/ noise density /noise figure (NF)	30.2 nV/√ Hz	11 μV$_{rms}$ (integrated from 100 Hz . . . 20 MHz)	43.2 nV/√ Hz	31 dB NF	19 nV/√ Hz	22.5 nV/√ Hz
IIP3	+31 dBm	+14 dBm	+12.2 dBm	+30 dBm	+2 dBm	+15.2 dBm
Stopband attenuation	N/A	N/A	62 dB at 15 MHz	72 dB at 5 MHz	N/A	32/90 dB at 20/40 MHz
Gain range	−6 . . . + 24 dB	−9 . . . + 69 dB	+12 . . . + 30 dB	+12 . . . + 55 dB	+13.5 . . . + 67.5 dB	−2 . . . + 50 dB
Technology	2 μm CMOS	0.35 μm BiCMOS	1.2 μm CMOS	0.18 μm CMOS	90 nm CMOS	0.35 μm CMOS

7 Conclusions and benchmarks

In summary, we have demonstrated the feasibility of realising the required reconfigurable analogue-BB functions of IEEE 802.11a/b/g-WLAN receivers under a low-voltage supply of 1 V. A proper permutation of the functional blocks together with the use of a ZIF/LIF-mixed downconversion has successfully optimised the reception of OFDM and CCK channels through a simple reconfiguration. In terms of circuit implementation, newly proposed functional blocks, namely series-switching mixer-quad, switched-current-resistor PGA and inside-OpAmp DOC, in cooperation, have met the standard requirements with low power consumption. All circuit techniques are generally applicable for different wireless systems.

A comparison of this work with state-of-the-art implementations is made in Table 3 [6–11]. This work exhibits the lowest-voltage standard-compliant analogue-BB chain ever reported, while measuring a competitive performance when compared with [10] that targets the same WLAN applications.

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