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INTERACTIVE IIR SC MULTIRATE COMPILER APPLIED TO MULTISTAGE DECIMATOR DESIGN

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This paper proposes an interactive architecture compiler for SC multirate circuits that allows the automated design from the frequency specifications to the building block implementation, applied to the design and synthesis of multistage SC decimators. The compiler provides a library of different topologies that comprises a few independent multi-decimation building blocks. New building blocks defined by the users are also available for the design of a specific stage. A design example of a 7th order SC decimator illustrates the efficient synthesis of the corresponding resulting circuits that achieve the required anti-aliasing amplitude responses with respect to the speed requirements of the operational amplifiers and also the minimum capacitance spread and total capacitor area.

Keywords: IIR filter; multistage; switched capacitors; decimator design; compiler.

1. Introduction

While the computer-assisted tools for the design of digital circuits with multirate technique have already attained a considerable degree of maturity, there are fewer tools for the engineers working on the analog portion of the decimator and interpolator chips.[1–4] Here, there is an important need to provide designers with computer-aided tools for designing of SC multirate circuits, which usually consists of a program for automatic synthesis of a analog multirate circuit, making use of the available architectures and techniques to optimize the implementation of a circuit. The compiler should present in its structure the following three major levels of hierarchy:

(i) System level synthesis;
(ii) Building block level synthesis;
(iii) Simulation (functional and electrical) and layout level synthesis.

The system level synthesis will generate a filter prototype from the frequency specifications. The building block synthesis will allow selection and search of the appropriate interconnection of different building blocks in order to obtain a specific functionality. The simulation and layout synthesis comprises the simulation of the circuit followed by the layout design that will be determined by an adequate selection of the library of cells including previously designed operational amplifiers (OAs), switches and arrays of capacitors.[5] The choice of different components will be made automatically based on the specifications and values of circuit components. To implement Switched Capacitor (SC) multirate circuits (decimators and/or interpolators), several architectures and techniques were presented since the early 80's. In conventional designs of SC, decimators were only implemented based on a standard single building block, like ladder structures or cascaded biquad building blocks.[6–11] Those solutions are usually not suitable and flexible for the implementation of an higher order complex filter with a large decimation factor.

In this paper, we present a computer-aided tool designated as Interactive Switched Capacitor Multirate Compiler (ISCMRATE) with three levels of synthesis that can be used in the automated design of multirate circuits from the specifications to layout. The compiler architecture presents, for multistage decimator design, an improved solution that allows the implementation of mixed architectures comprising a library of topologies including different and independent multi-decimation building blocks. For optimizing IIR SC decimating circuit performance while simultaneously minimizing silicon area,[8] a set of rules are also presented to select the most suitable steps in programming based on a statistical approach.[9,10]

2. ISCMRATE Compiler — General Architecture

The general architecture of ISCMRATE for the design of SC multirate circuits is schematically presented in Fig. 1.

The interactive computer program ISCMRATE, which has been developed in around 4500 lines of C++ code and a textual user interface, runs on SUN SPARC workstation. The basic architecture of the program comprehends the system level and the building block level linked to a few existing programs.[8,9] The automated layout generation of the circuit (under development) will allow the selection of the different electronic components (OAs, switches and capacitors) from a library of cells. For the practical feasibility and compatibility of the compiler, the building blocks in each stage are therefore determined independently. New building blocks defined by the users are also available for the design of a specific stage.[10–12] The design space exploration of the compiler (e.g., range of parameters, variation of design components) has been discussed in Ref. 10. The multirate and multistage algorithm of ISCMRATE for decimator design is partially shown in Fig. 2.

Program starts with filter specification and a given decimating factor. After the selection of a particular topology, a file of component values will be generated for SWITCAP.[13]

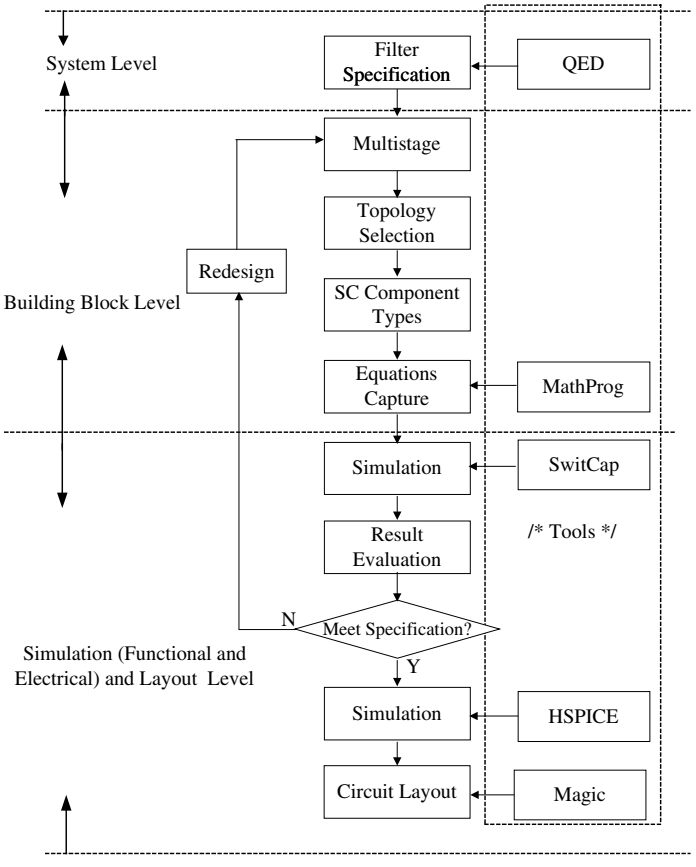

Fig. 1. General architecture of the ISCMRATE compiler for SC multirate circuits design.

3. Design Critera of Multirate and Multistage Circuit and Topology Selection

Based on a statistical approach, the optimum decimating factors and ripple, pole-zero assignment of the system level synthesis at the corresponding stages is obtained according to the following design criteria:

(a) Decompose the overall ripple of a filter in different values by ascending order to reduce the decimator order.
(b) Implement the first stage with the largest multiple decomposed from the decimating factor (M) and decompose M in prime factors by descending order in order to minimize the speed requirements of the amplifiers.
(c) The decimating factors in each building blocks or stages should not be too large ($M < 10$), especially in the decimators with internally cascaded or ladder structure.[10]

```
for (each P in permutations of total decimating factor M)
 {
 last_output = terminal;
     for (each stage with decimating factor Mi in P)
        {
        for (each block b with Mi)
           {
                Switch (block type of b)
                Case externally: build_externally (last_output);
                Case internally: build_internally (last_output);
                Case ladder: build_ladder (last_output);
                Otherwise: new_block: build_new (last_output);
           }
        }
 maximize_dynamic_range ( );
 /* the same output level at each OA */
 minimize_capacitance_spread ( );
 /* (a) by the capacitances scaling */
 /* (b) by presetting the coupling capacitors */
 }
```

Fig. 2. ISCMRATE — Multirate and multistage independent building blocks algorithm.

Then, the optimum sequence of the corresponding topology at the building block level synthesis is obtained according to the next design rules:

(d) The optimum sequence for the organization of a topology should first include externally cascaded blocks followed by internally cascaded, and then ladder blocks, since decomposing M in prime factors by descending order implies that the latter is restricted to moderate values of the decimating factors.
(e) Adjacent structures of internally cascaded will not allow two or more same blocks with the damping type (E damping or F damping).
(f) The selection of preferred circuit topologies is also considered its performance behavior under nonideal characteristics of the amplifiers, namely the finite dc gain and bandwidth.

The points of views (a)–(c) have been introduced in Ref. 5. Also, the effectiveness of the proposed approaches (d)–(f) have been discussed in Ref. 10.

4. Automated Design of a Multistage Decimator — Example

The performance of the ISCMRATE compiler can be illustrated by means of an example of a 7th order lowpass SC filter prototype with sampling frequency

500 MHz, passband ripple of 0.165 dB, cutoff frequency $f_c = 1$ MHz, and minimum rejection of 100 dB above 5 MHz.

In order to be possible to implement this prototype filter in CMOS technology, multirate techniques must be used.[5] Based on these techniques, this prototype can be implemented by means of a mutistage decimator. This decimator will reduce the sampling frequency from 500 MHz at the input, to 50 MHz at the output with a multistage implementation. With an overall decimation factor of $M = 10$ that can be automatically factored into the product $M = M_1 M_2$, meaning that only two stages are needed for the implementation of the decimator. The multistage steps followed by the program at the system level synthesis are shown in Fig. 3.

The selection by the program of an optimum sequence of topologies allows the determination of an architecture with a 4th order internally cascaded building block with $M_1 = 5$, followed by a 3rd order ladder structure with $M_2 = 2$, according to the above design criteria. The corresponding steps at the building block level synthesis are shown in Fig. 4.

After scaling for the maximum signal handling capability and normalizing with respect to the unit capacitance values, the decimator presents an acceptable maximum capacitance spread of 19 and a total capacitance area close to 176 capacitor units for the complete circuit, selected from six different solutions (different damping types and building block topologies). The selected overall circuit structure of

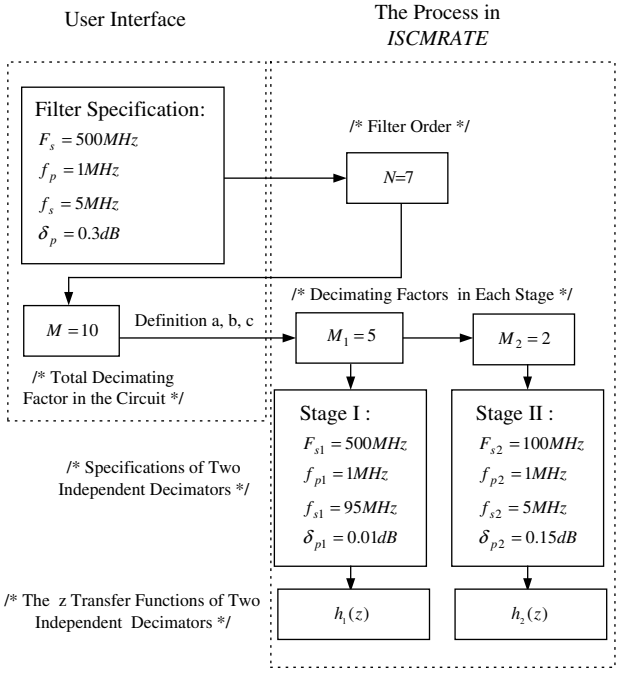

Fig. 3. Compiler steps for multistage design decimator at system level in ISCMRATE.

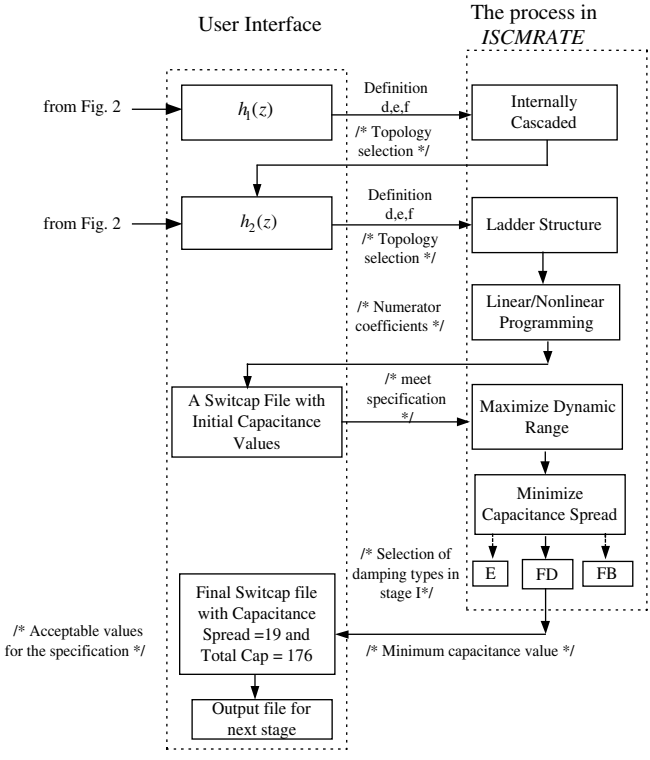

Fig. 4. Compiler steps for multistage design decimator at building block level synthesis in ISCMRATE.

the SC decimator, automatically designed, is presented in Fig. 5. Following the automated methodology presented in Fig. 1, the compiler enters in simulation and layout synthesis level and generates initially the input file for SWITCAP, in order to simulate functionally the overall decimators. The nominal passband and overall computer simulated amplitude responses with ideal gain amplifiers are shown in Figs. 6(a) and 6(b), the nominal passband and overall amplitude responses with finite gain amplifiers are shown in Figs. 7(a) and 7(b), respectively. This result shows a good performance with respect to amplitude response accuracy and dynamic range, and anti-aliasing characteristics. Total optimation process in above case is above 25 min.

After the functional simulation based on the values of the different components, an electrical simulation and layout synthesis will be followed (this part is still under development).

5. Conclusions

This paper proposes an interactive architecture compiler ISCMRATE applied to the design of multistage IIR SC decimators with large decimating factors. The compiler

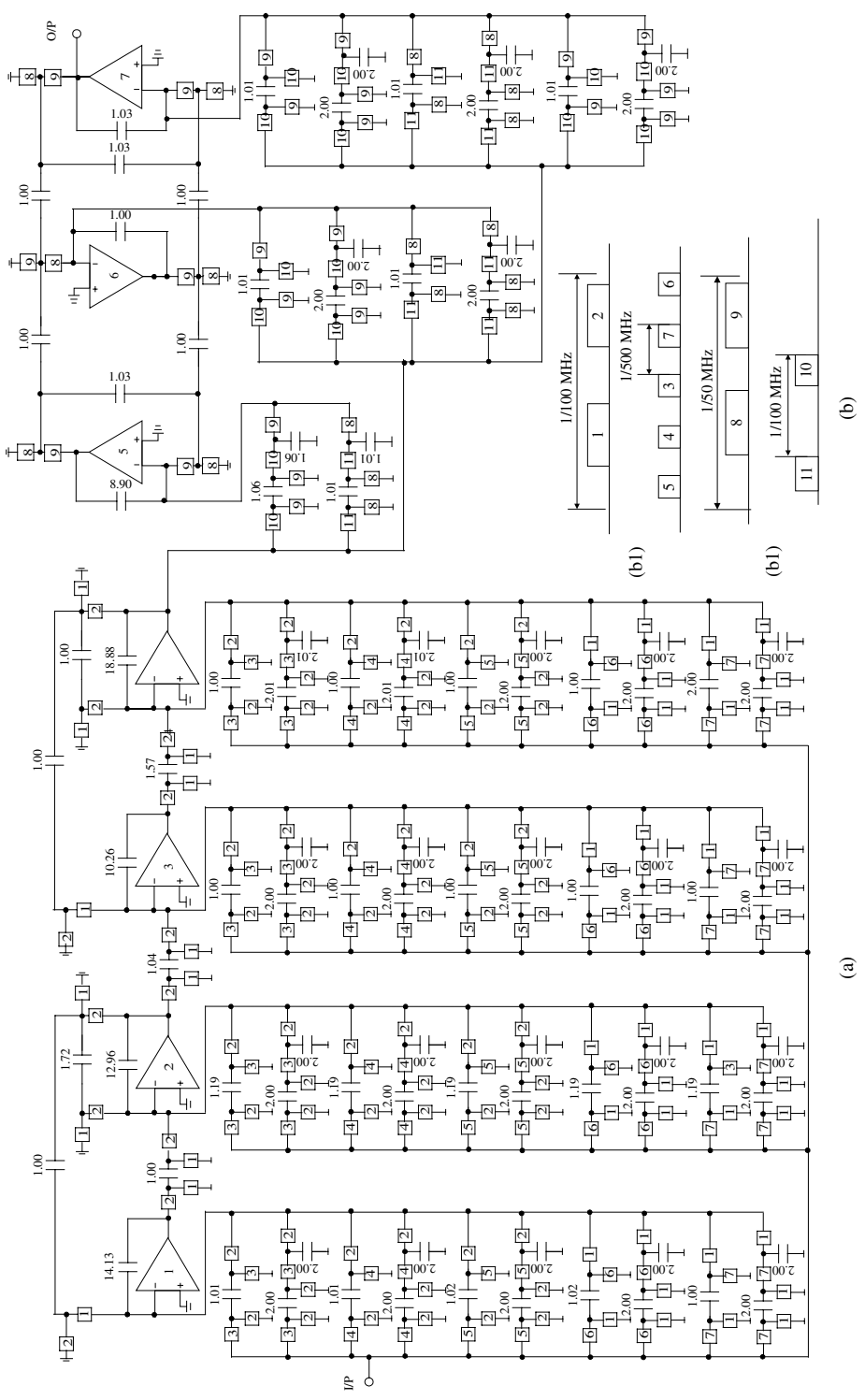

Fig. 5. (a) SC circuit and (b) switching waveforms ((b1) internally cascaded and (b2) ladder structure).

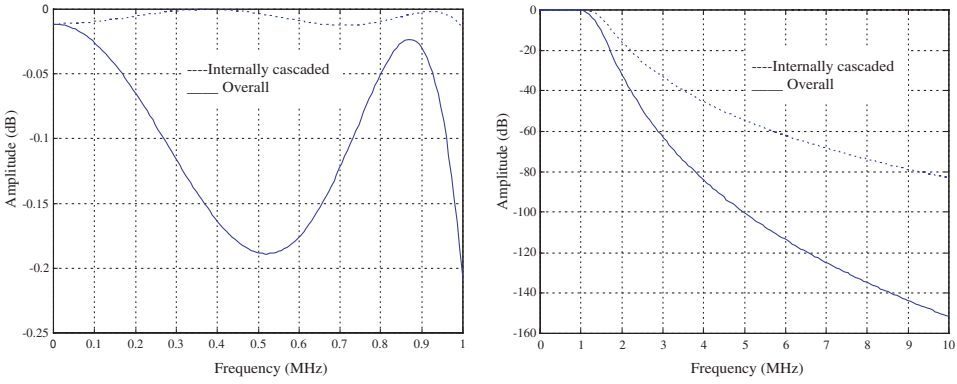

Fig. 6. Computer simulated (a) passband and (b) overall amplitude responses with ideal dc gain amplifiers.

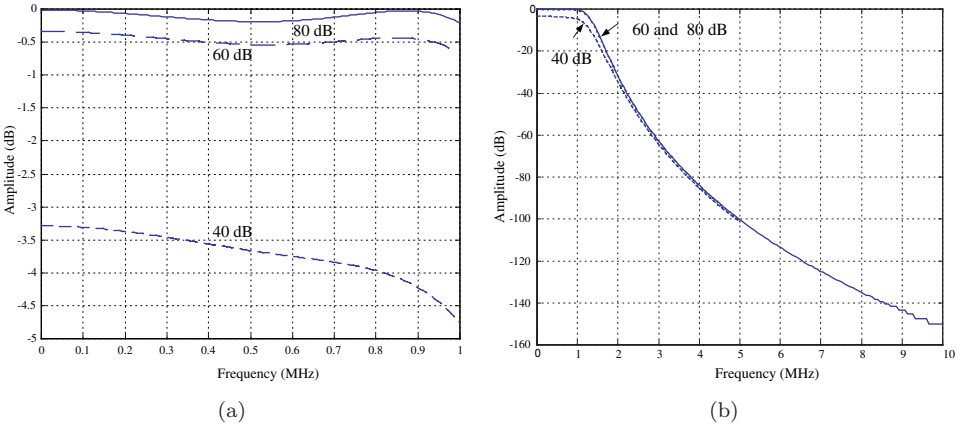

Fig. 7. Computer simulated (a) passband and (b) overall amplitude responses with finite dc gain amplifiers.

presents three different levels, namely the system synthesis, the building block and the simulation and layout. In the first level of synthesis, the multi-decimation cascaded and ladder blocks or new building blocks are independently determined in order to fulfill user's different requirements. The methods allow designers to quickly compute the exact capacitance ratios and realize a predetermined set of design specifications, are also available in the second level.

Finally, in the third level, the verification of the behaviors of the circuit by simulation and consequent layout design is obtained. The design example presented the multiple decimating structures that can effectively eliminate treacherous aliasing frequency components arising on SC multistage externally cascaded decimating filters and demonstrates the compiler feasibility and compatibility.

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