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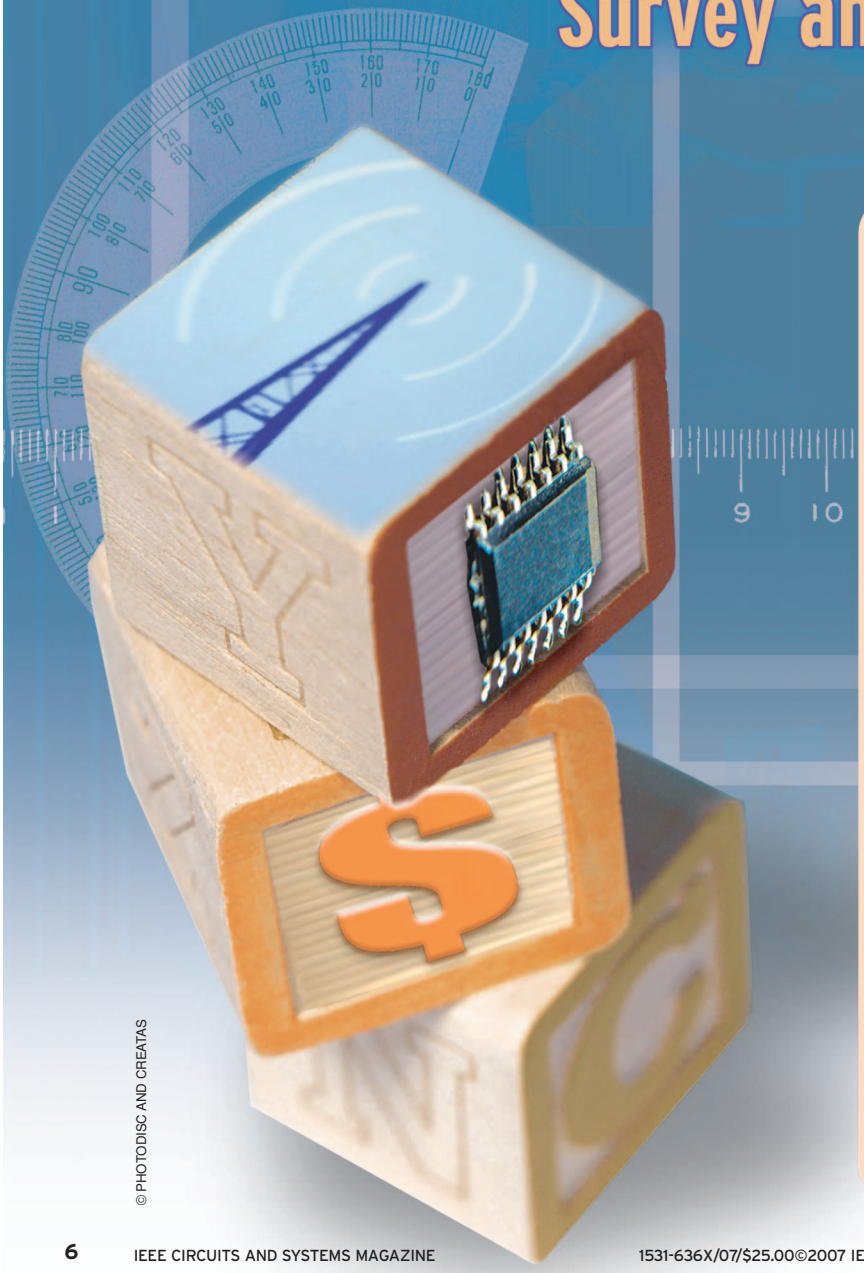
Transceiver Architecture Selection:

Review, State-of-the-Art Survey and Case Study



Abstract

Realizing multi-standard transceivers with maximum hardware reuse amongst the given standards is of great importance to minimize the manufacturing cost of emerging multi-service wireless terminals. A well-defined architecture in conjunction with a reconfigurable building-block synthesis is essential to formulate such a kind of tunable transceiver under a wide range of specifications. In this paper, we present both fundamental and state-of-the-art techniques that help selecting transceiver architecture for single-/multi-standard design. We begin by reviewing the basic schemes and examining their suitability for use in modern wireless communication systems (GSM, WCDMA, IEEE 802.11, Bluetooth, ZigBee and Ultra Wideband). The justifications are confirmed with the state-of-the-art choices through a survey (with 100+ references) of the most frequently used receiver and transmitter architectures reported in 1997 to 2005 IEEE solid-state circuit forums: ISSCC, CICC, VLSI and ESSCIRC. State-of-the-art techniques for multi-standability are analyzed through careful case studies of a cellular receiver for GSM/DCS/PCS/WCDMA, and several WPAN/WLAN transceivers for Bluetooth and IEEE 802.11a/b/g. They disclose, on the architecture and circuit levels, many ideas that have successfully inspired the recent development of wireless circuits and systems.

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I. Introduction

The trend in wireless communications is toward creating a network-ubiquitous era in the years to come. It will not be surprising that the next-generation mobile devices will become a universal multi-service wireless terminal. Yet, to operate a wireless device under different network protocols, a multi-standard transceiver is mandatory [I, 1], [I, 2].

Although a multi-standard design can be achieved simply by duplicating more than one transceiver, this does not appear as an economical choice for manufacturing and further development. On the other hand, a fully-reconfigurable transceiver (e.g., software-defined radio) befitting the wanted standards via block reconfiguration can effectively minimize the cost. The associated challenge is, of course, a wide-range tunable performance in each building block. These design considerations constitute a hard tradeoff between cost and design efficiency. Obtaining a fine compromise requires not only the extensive understanding of the basic transceiver architectures and standard requirements, but also an adequate knowledge of the state-of-the-art devices that have already hinted at many practical-problem-solving solutions.

This paper attempts to offer the designers working in wireless circuits and systems some decisive information that helps making their transceiver design a successful single-/multi-standard compliance. The fundamental receiver and transmitter architectures are reviewed in Sections II and III, respectively. Their suitability for use in modern wireless-communication systems is analyzed and discussed in Section IV. A survey and case studies of the state-of-the-art works are presented in Section V.

II. Receiver (RX) Architectures

A. Superheterodyne RX

The high reliability of superheterodyne RX [I, 3] has made it the dominant choice for many decades. Its generic scheme is shown in Figure 1. With a band-selection filter rejecting the out-of-band interference, the in-band radio-frequency (RF) channels are free from amplification by a low-noise amplifier (LNA). A high-Q off-chip image-rejection filter prevents the image channel from being superimposed into the desired channel in the RF-to-intermediate frequency (IF) downconversion. The channel selection requires a voltage-controlled oscillator (VCO) driven by an RF frequency synthesizer and a high-Q off-chip surface-acoustic-wave (SAW) channel-selection filter (CSF). The signal level of the selected channel is properly adjusted by a programmable-gain amplifier (PGA) prior to the IF-to-baseband (BB) quadrature downconversion. This downconversion requires another phase-locked loop (PLL) and a quadrature VCO (QVCO) for generating the in-phase (I) and quadrature-phase (Q) components. The BB lowpass filters (LPFs) are of low-Q requirement but high in filter order for ultimate channel selection. The BB PGAs adjusts the signal swing for an optimum-scale analog-to-digital (A/D) conversion.

The superior I/Q matching because of low operating frequency, as well as the avoidance of dc-offset and $1/f$-noise problems, are the pros of super-heterodyne. Whereas the low integration level and high power consumption for the on/off-chip buffering are its cons. There also exists a tradeoff in IF selection; a high IF (e.g., ~70 MHz) improves the sensitivity due to higher

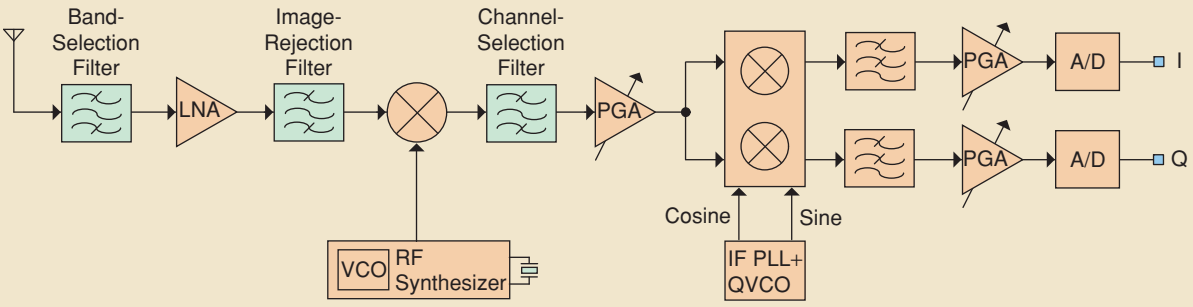

Figure 1. Superheterodyne RX.

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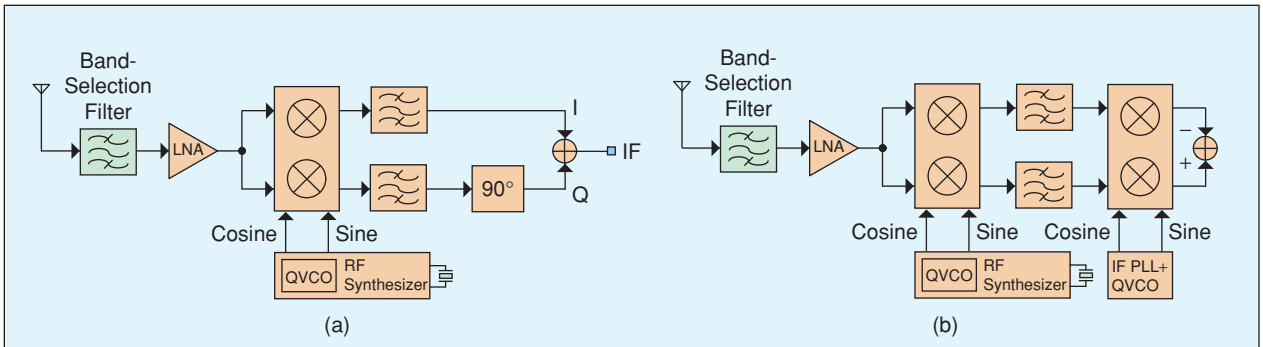

Figure 2. Image-rejection RX: (a) Hartley and (b) Weaver.

attenuation can be offered by the image-rejection filter, while a low IF (e.g., ~10 MHz) enhances the selectivity due to a lower Q requirement from the SAW filter. On the other hand, due to the restricted IF choice of 10.7 or 71 MHz for commercial filters, a multi-standard design normally constitutes a high cost for filtering at different IFs.

B. Image-Reject RX: Hartley and Weaver

The principle of image-rejection RX is to process the desired channel and its image in such a way that the image can be eliminated eventually by signal cancellation. Hartley [I, 4] proposed such an idea with the architecture shown in Figure 2(a). The RF signal in the downconversion is split into two components by using two matched mixers, a QVCO and an RF frequency synthesizer. The outputs, namely in-phase (I) and quadrature-phase (Q), are then filtered by the LPFs. With a 90°-phase-shifter added to the Q channel, the image can be canceled after the summation of I and Q outputs. In practice, a perfect-quadrature downconversion and a precise 90°-phase-shifter cannot be implemented in an analog domain, especially at high frequency. The practical values of static gain/phase mismatches are 0.2 to 0.6 dB/1° to 5°, corresponding to an image rejection of roughly 30 to 40 dB.

The Weaver RX [I, 5], as shown in Figure 2(b), is identical to Hartley's one except that the 90°-phase-shifter is replaced by a quadrature downconverter. The key advantage of such a replacement is related with the fact that a downconverter can realize relatively much wideband quadrature matching. The overheads are the additional IF mixers, PLL and QVCO. Both Hartley and Weaver schemes feature high integratability and are convenient to use in multi-standard design.

C. Zero-IF RX

Similar to an image-reject RX, a zero-IF RX obviates the need to use any off-chip component. As shown in Figure 3, the desired channel is translated [I, 6] directly to dc through the I and Q channels. The image is eliminated through signal cancellation rather than filtering. Since the image is the desired channel itself, the demanded I/Q matching is practically achievable for most applications.

The fundamental limitation of the zero-IF RX is its high sensitivity to low-frequency interference, i.e., dc-offset and $1/f$ noise. With them superimposed on the desired channel, a substantial degradation in signal-to-noise ratio (SNR) or complete desensitizing of the system due to a large baseband gain may result. A capacitive-coupling and a servo loop are common choices to alleviate this problem, but at the expense of long settling time and large chip area for realizing the very low cutoff frequency highpass pole.

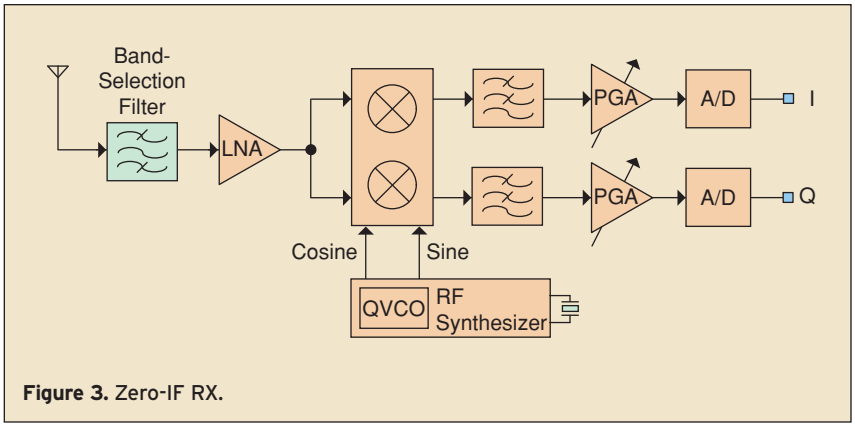

Figure 3. Zero-IF RX.

D. Low-IF RX

The Low-IF RX [I, 7] features a similar integratability as the zero-IF one but is less susceptible to the low-frequency interference. The desired channel is downconverted to a very low-frequency bin around dc, typically ranging from a half to a few channel spacings. Unlike the

zero-IF RX, the image is not the desired channel itself. The required image rejection is normally higher as the power of the image can be significantly larger than that of the desired channel. Depending on the permutation of the building blocks, a low-IF RX can have more than one possible architecture, as shown in Figure 4(a) to (d).

- Case-I performs the IF-to-BB downconversion digitally, eliminating the secondary image problem while permitting a pole-frequency-relaxed dc-offset cancellation adopted in the analog BB. The disadvantages are a higher bandwidth requirement (compared with the zero-IF) from the LPFs and PGAs, and a higher conversion rate required from the A/Ds.
- Case-II is identical to Case-I except the LPFs are replaced by a pair of filters operating in the complex domain, namely a polyphase filter or a complex filter. Such a filter performs not only channel selection, but also relaxes the I/Q matching requirement from the PGAs and A/Ds.
- Case-III is another combination employing a complex filter together with an analog IF-to-BB downconverter for doubling the image rejection. With such a structure, the I/Q matching required from the following PGA and A/D is very relaxed. The bandwidth of the PGAs and the conversion rate of the A/Ds are reduced to their minimum like zero-IF. The associated overhead is a low cutoff frequency highpass pole in the dc-offset cancellation that is necessary in the PGAs due to the high baseband gain. The chip area impact is therefore very significant since the systems containing I and Q channels are typically differential (i.e., four highpass poles).
- Case-IV positions an analog IF-to-BB downconverter prior to the A/Ds such that the conversion rate of the A/Ds can be minimized. Unlike in Case-III, the pole-frequency of the dc-offset cancellation circuit can be relaxed.

Comparing with the zero-IF RX, the low-IF RX is less sensitive to $1/f$ noise and dc-offset at the expense of a higher image-rejection requirement.

E. Comparison of Different RX Architectures

Table I gives a summary of the presented RX architectures. Their characteristics determine their appropriateness for modern wireless communication systems, as presented in Section IV.

III. Transmitter (TX) architectures

A. Superheterodyne TX

Architecturally, the superheterodyne TX (Figure 5) is a reverse of operation from its RX counterpart with the A/D conversion replaced by a digital-to-analog (D/A) conversion. However, they are very different in the design specification. For instance, in transmission, only one channel will be upconverted in the TX. Its power level is well-determined throughout the TX path. There are differences in the signal reception, the power of the incoming signals is variable and the desired channel is surrounded with numerous unknown-power in-band and out-of-band interferences. Thus, PGAs is essential for the RX to relax the dynamic range of the A/D converter, but can be omitted in the TX if the power control could be fully implemented by the power amplifier (PA). Similarly, since the channel in the TX is progressively amplified toward the antenna and

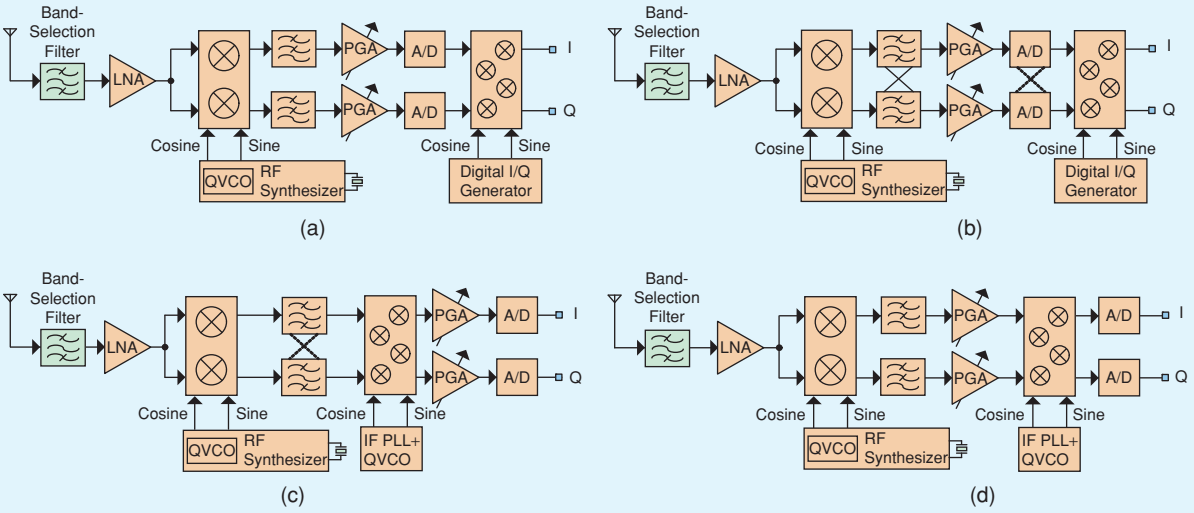

Figure 4. Low-IF RX: (a) Case-I (b) Case-II (c) Case-III (d) Case-IV.

finally radiated by a PA, the linearity of the whole TX is dominated by the PA. Whereas it is the noise contribution of the LNA that dominates the whole RX noise figure.

B. Direct-up TX

The direct-up TX (Figure 6) features an equal integratability as the zero-IF RX, but is limited by the well-known LO pulling. To meet the standard required modulation mask, techniques such as offset VCO and LO-leakage calibration are somehow necessary. Again, it is noteworthy that albeit the functional blocks in RX and TX are identical, their design specifications are largely different. For instance, the RX-LPF has to feature a high out-of-band linearity due to the co-existence of adjacent channels, whereas it is not demanded from TX-LPF.

C. Two-step-up TX

Similar to the low-IF RX, two-step-up TXs can be structured into four possible schemes as shown in Figure 7(a) to (d).

- Case-I frequency-up-translates the desired channel digitally prior to D/A conversion such that the low-frequency interference from the D/A and LPF can be canceled by means of an ac-coupling or a servo loop, avoiding the transmission of DC-to-LO-mixing products. In this case, the required conversion rate of the D/A and the bandwidth of the LPF must be increased.
- Case-II employs complex filters to reject the image resulting from I/Q mismatch between the I and Q D/As and filters to improve the purity of the output spectrum. Other properties are similar to Case-I.
- Case-III alternatively employs an analog BB-to-IF upconverter to reject the image. With such a permutation, only an LPF would be required and the output spectrum is purified.
- Case-IV locates the analog BB-to-IF upconverter between the D/A converter and complex filters, delivering doubled image rejection and allowing a

Table I.
Summary of different RX architectures.

RX Architecture	Advantages	Disadvantages
Superheterodyne	+Reliable performance +Flexible frequency plan +No DC-offset and 1/f noise	—Expensive and bulky, high power —Difficult to share the SAW filters for multistandard
Image-Reject (Hartley and Weaver)	+Low cost +No DC-offset and 1/f noise +High integratability	—Quadrature RF-to-BB downconversion —Suffer from first and secondary images —Narrowband (Hartley) —High I/Q matching
Zero-IF	+Low cost +Simple frequency plan for multistandard +High integratability +No Image problem	—Quadrature RF-to-BB downconversion —DC-offset and 1/f-noise problems
Low-IF	+Low cost +High integratability +Small DC-offset and 1/f noise	—Image is a problem —Quadrature RF-to-IF and double-quadrature IF-to-BB downconversions

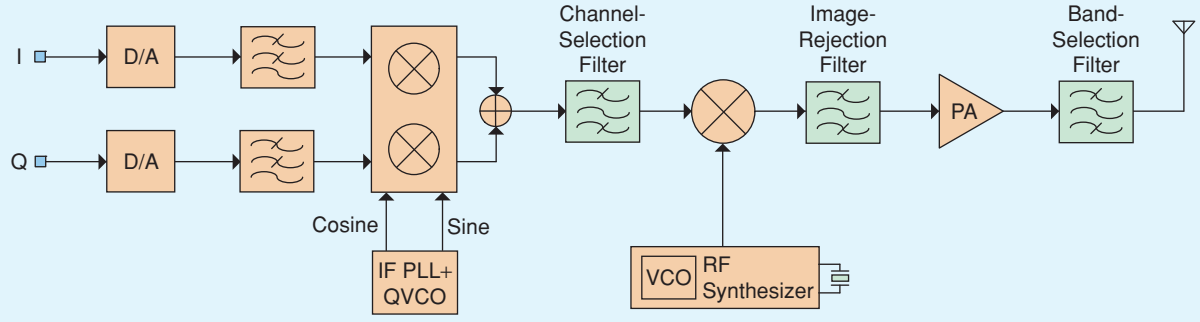

Figure 5. Superheterodyne TX.

capacitive coupling (or by a servo loop) between the upconverter and filter, and between the filter and IF-to-RF upconverter. One key advantage of this scheme is the allowance of independent dc-biasing for each block.

Compared with the direct-up TX, the LO feedthrough is reduced (of course, the amount depends on the selected IF and port-to-port isolation) as the first and second VCOs can be offset from each other (i.e., $LO = VCO_1 + VCO_2$). The overheads are the additional power and area consumption required for the mixing, filtering and frequency synthesis.

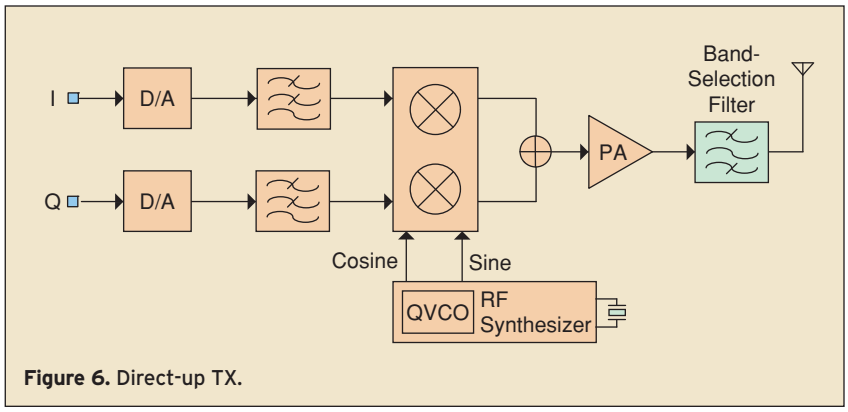

Figure 6. Direct-up TX.

D. Comparison of Different TX Architectures

Table II summarizes the presented TX architectures. Similar to the RXs, their characteristics determine their appropriateness for modern wireless communication systems, as presented next.

IV. RX and TX Architectures for Modern Wireless Communication Systems

A. GSM/DCS/PCS

GSM [I, 8] and its copies, DCS and PCS, are currently the dominating standards for cellular communications. Except for their differences in frequency band and geographical use, the PHY-relevant data are alike, as listed in Table III. With the Gaussian minimum shift keying (GMSK) as the modulation method, a time-division 200-kHz channel can deliver a data rate of 270 kb/s. GSM/DCS/PCS RX using superheterodyne [II, 1] , low-IF [II, 14] or zero-IF [II, 15] architecture has been successfully realized.

The TX typically follows the RX architecture to share the SAW filter (if any) and frequency synthesizing components. There are following examples: [II, 13] using superheterodyne RX with TX, and [II, 5] [II, 6] using a zero-IF/low-IF RX with a direct-up TX. In addition to them, there are other possible types of TX. The two-step-up TX [II, 16] can gain advantages from the frequency relationship between the GSM (0.9 GHz) and DCS (1.8 GHz) to realize a dual-mode solution. PLL [II, 18] [II, 20] and polar

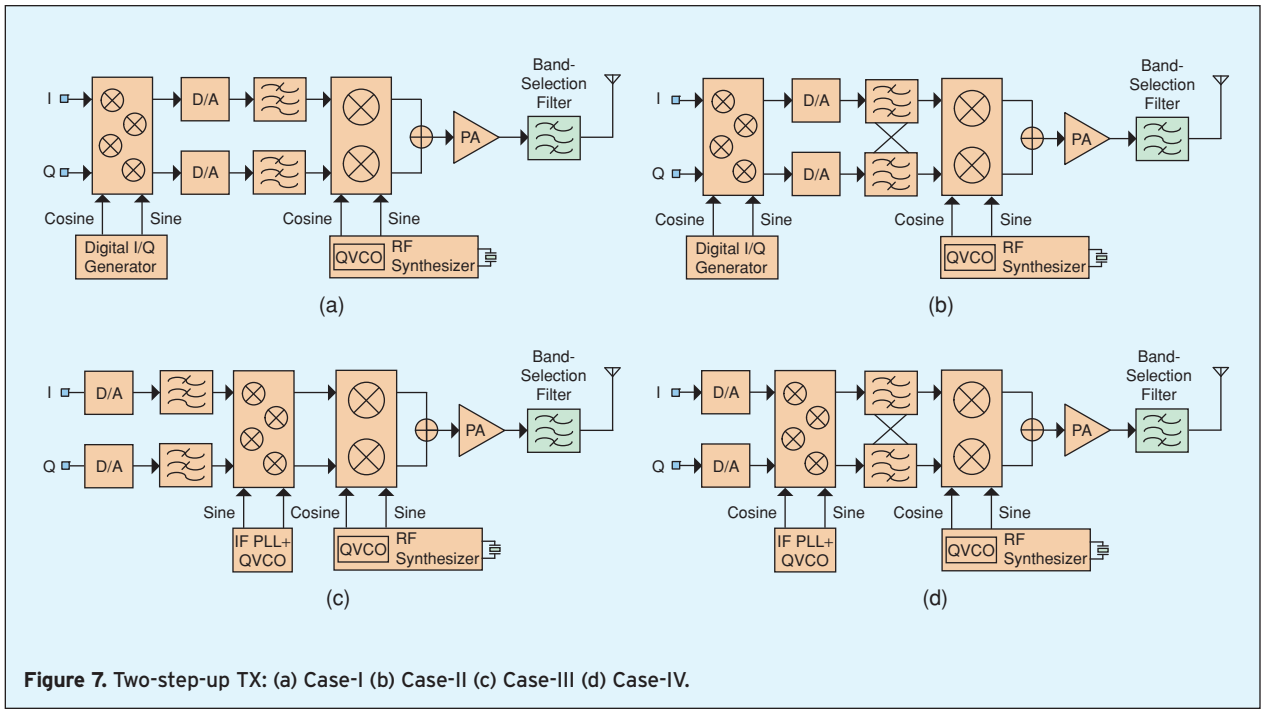

Figure 7. Two-step-up TX: (a) Case-I (b) Case-II (c) Case-III (d) Case-IV.

Table II.
Summary of different TX architectures.

TX Architecture	Advantages	Disadvantages
Superheterodyne	+Reliable performance +Flexible frequency plan +No LO leakage +Simple DC-offset cancellation at BB	−Expensive and bulky, high power −Difficult to share the SAW filters for multistandard
Direct-Up	+Low cost +Simple frequency plan for multistandard +High integratability +No image problem	−Quadrature BB-to-RF downconversion −LO leakage −DC-offset cancellation is difficult at BB (area and settling time impacts)
Two-Step-Up	+Low cost +High integratability +Simple DC-offset cancellation at BB	−Image is a problem −Quadrature IF-to-RF and double-quadrature BB-to-IF downconversions −LO leakage (depends on the IF)

Table III.
GSM/DCS/PCS characteristics.

	GSM	DCS	PCS
Modulation	GMSK	GMSK	GMSK
Frequency Band	890–960 MHz	1710–1850 MHz	1880–1930 MHz
Channel Bandwidth	200 kHz	200 kHz	200 kHz
Bit Rate	270 kb/s	270 kb/s	270 kb/s

Table IV.
WCDMA characteristics.

	WCDMA
Modulation	QPSK
Frequency Band	1920–2170 MHz
Channel Bandwidth	3.84 MHz
Bit Rate	3.84 Mb/s

[II, 19] [II, 21] [II, 22] modulation-based TXs are also possible due to the constant amplitude of GMSK signal.

B. WCDMA (UMTS)

The 3G wireless system is known as WCDMA or UMTS [I, 9]. It can deliver a data rate up to 3.84 Mb/s. A pseudo-random sequence spreads the quadrature phase-shift keying (QPSK) modulated signal to a 3.84-MHz bandwidth. Its main characteristics are listed in Table IV.

The wideband and spread spectrum nature of WCDMA stimulates the use of zero-IF RX [II, 25] providing that the dc-offset and $1/f$ noise are comfortably eliminated through, for instance, ac coupling or servo loop. The required image rejection with a zero IF is very relaxed, i.e., 25 dB. The induced intersymbol interference (ISI) is uncritical as long as the highpass pole of the dc-offset cancellation is sufficiently small (<10 kHz). The concurrent transmit and receive operations, however, require a very linear RF path.

WCDMA TX using superheterodyne [II, 35], direct-up [II, 36] or two-step-up [II, 37] architecture has all been tried. However, if a zero-IF RX has been chosen, a direct-up TX is efficient to follow such that the blocks for frequency synthesis can be reused. The problem of LO pulling requires calibration circuits (or other type of circuitry) to suppress the carrier leakage [II, 36].

C. 802.11x and HiperLAN 2

WLAN is intended to provide high-speed internet access whenever wired LANs are not possible (also economically feasible) or many subscribers are dispersed within a relatively large place such as an airport or a hotel. The IEEE 802.11 [I, 10] family is dedicated to high-speed WLAN communications. Currently, the most relevant PHY-layers are 802.11a, b and g. The older FH and DS modes are seldom used today, while the latest 802.11n will be ratified soon.

The 802.11FH and 802.11DS operating in the 2.4-GHz ISM band provide a maximum data rate of 2 Mb/s by using the frequency-hopping spread spectrum (FHSS) and direct-sequence spread spectrum (DSSS) techniques, respectively. The 802.11a based on the orthogonal frequency-division multiplexing (OFDM) technique delivers a high data rate up to 54 Mb/s by using 64-quadrature amplitude modulation (64-QAM) in the 5-GHz UNII band. For 802.11b, the maximum data rate is 11 Mb/s by exploiting Complementary Code Keying (CCK) modulation in the 2.4-GHz band. A mix of a and b is g, which supports a data rate up to 54 Mb/s using the OFDM with 64-QAM in the

2.4-GHz ISM band, and backward complies with b for lower date-rate options. The HiperLAN 2 [I, 11] is harmonized with the 802.11a. Their characteristics are tabulated in Table V.

The wideband nature of 802.11a/b/g and HiperLANs again suggests the use of zero-IF RX [II, 44] [II, 48]. However, the low-IF [II, 54] is found effective for OFDM mode in 802.11a/g, a frequency error in frequency conversion can locate the ±1st subcarriers on the notch of the dc-offset cancellation. The dual-conversion [II, 52] [II, 53] is similar to superheterodyne but using a relatively high IF (such as 3 GHz) to allow the image rejection to be fully realized on-chip. Moreover, since the channel selection is at IF, lower power and better phase-noise LO is expected when comparing it with the zero-IF design. The frequency plan is critical to maximize the functional blocks sharing in the dual-conversion.

The architectural choice of WLAN TX is typically consistent with that of the RX [II, 47]–[II, 50].

D. Bluetooth (802.15.1), HomeRF, ZigBee (802.15.4) and Ultra Wideband (802.15.3)

A couple of standards have been deployed for wireless personal-area network (WPAN) focusing on low-cost low-power RF technology. The dominant standards are Bluetooth, HomeRF, ZigBee and Ultra Wideband (UWB). Their characteristics are tabulated in Table VI.

Bluetooth, also known as 802.15.1 [I, 12], uses FHSS with Gaussian frequency shift keying (GFSK) as the modulation, delivering a data rate of 1 Mb/s using a 1-MHz channel at the 2.4-GHz ISM band. Most of the solutions for Bluetooth are low-IF RXs with direct-up TXs [II, 58] known for their simplicity but adequate performances. The PLL TXs [II, 67]–[II, 70] are also proved to be feasible since the frequency synthesizer generates the constant-amplitude GFSK channels without a separated TX path.

HomeRF [I, 13] is similar to Bluetooth; it also uses FHSS access technique, GFSK modulation and the 2.4-GHz ISM band, the exception being the channel bandwidth that is 5 MHz for a higher data rate of 5 Mb/s. Many characteristics of HomeRF align with Bluetooth. With a bandwidth tunable baseband, a Bluetooth solution can be reused for HomeRF.

ZigBee, also known as 802.15.4 [I, 14], is another low-cost technology. It employs 5-MHz GFSK channels to communicate at the 2.4-GHz ISM band, delivering a data rate up to 250 kb/s. A complete TXR has been reported for this standard [II, 78]. Consistent to our previous considerations, its narrowband nature recommends the use of a low-IF RX together with a direct-up TX.

UWB, also known as 802.15.3 [I, 15], is an evolutionary standard highly different from the existing ones. One UWB band is between 3.1–10.6 GHz with a bandwidth of 500 MHz, delivering a data rate up to 480 Mb/s using

Table V.
802.11x and HiperLAN 2 characteristics.

	802.11FH	802.11DS	802.11a	802.11b	802.11g	HiperLAN 2
Modulation	FHSS:	DSSS:	OFDM: BPSK/	DSSS:	DSSS:	OFDM:
	D-BPSK/	D-BPSK/	QPSK/	D-BPSK/D-QPSK	D-BPSK/D-QPSK	FSK/GMSK
	D-QPSK	D-QPSK	QAM	CCK:	CCK:	
					OFDM:	
					BPSK/QPSK/QAM	
Frequency Band	2.4 GHz[a]	2.4 GHz[a]	5 GHz[b]	2.4 GHz[a]	2.4 GHz[a]	5 GHz[c]
Channel Bandwidth	1 MHz	22 MHz	16.25 MHz	22 MHz	16.25–22 MHz	16.25 MHz
Bit Rate	1, 2 Mb/s	1, 2 Mb/s	6-54 Mb/s	1–11 Mb/s	1–54 Mb/s	1.5–54 Mb/s
Remark: a: 2402–2480 MHz, b: 5150–5350 and 5725–5825 MHz, c: 5150–5350 and 5470–5725 MHz						

Table VI.
Bluetooth, HomeRF, ZigBee and Ultra Wideband characteristics.

	Bluetooth	HomeRF	ZigBee	Ultra Wideband
Modulation	FHSS: GFSK	FHSS: GFSK	GFSK	SP/FS-OFDM
Frequency Band	2402–2480 MHz	2402–2480 MHz	2402–2480 MHz	3100–1060 MHz
Channel Bandwidth	1 MHz	1 MHz, 5 MHz	5 MHz	500 MHz
Bit Rate	1 Mb/s	1.6–10 Mb/s	20, 40, 250 kb/s	110–480 Mb/s

Table VII. Abbreviations of TX and RX architectures.	
SH: Superheterodyne	LIF: Low-IF
PLL: Phased-locked Loop Modulation	ZIF: Zero-IF
POLAR: Polar Modulation	DU: Direct-Up
DUAL: Dual-Conversion	2SU: Two-Step-Up
WEAVER: Weaver	HIF: High IF

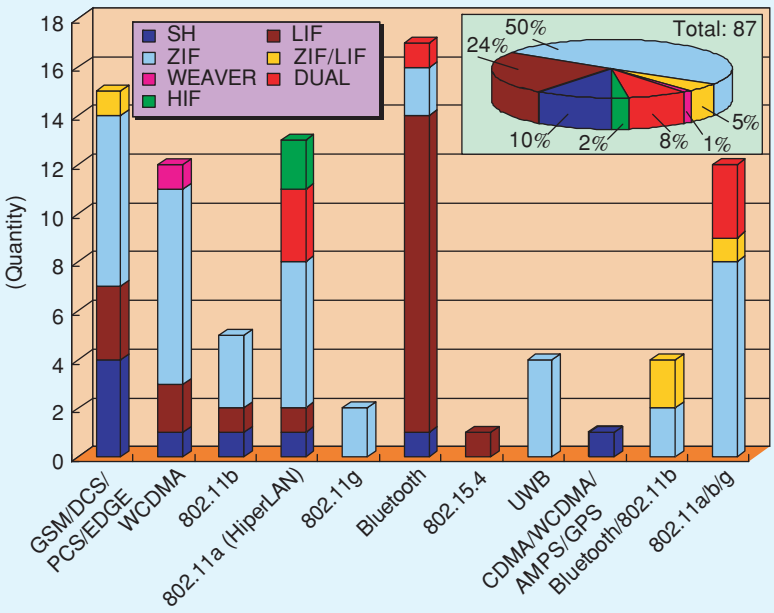

Figure 8. TX architectures employed in the state-of-the-art devices.

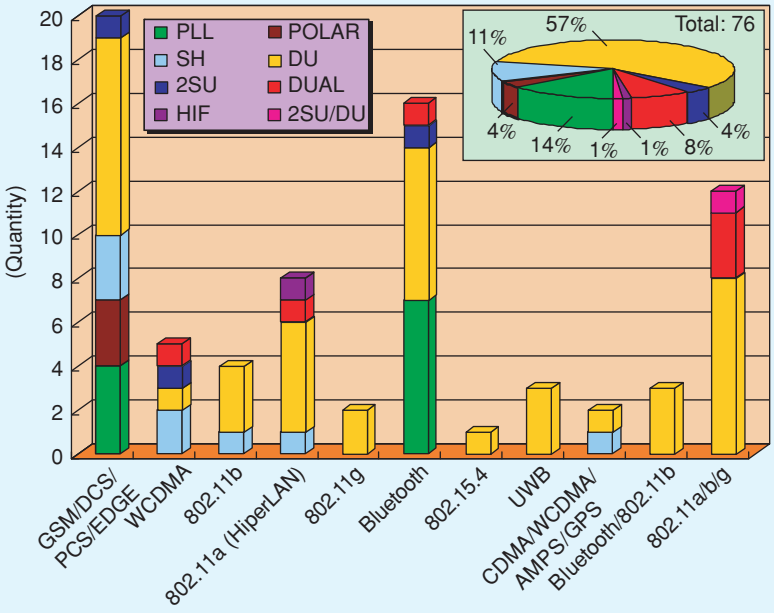

Figure 9. TX architectures employed in the state-of-the-art devices.

shaped-pulse (SP) or frequency-switched OFDM (FS-OFDM) modulation. Such a wideband system suggests, again, the use of zero-IF RX [II, 81], [II, 82] and direct-up TX [II, 83].

V. Survey and Case Studies

A. State-of-the-art Development

The research and development on wireless systems have turned what seemed impractical systems like zero-IF RX to plausible solutions. Simultaneously, the use of traditional superheterodyne architectures has started to fade out due to its high power and high cost. This section will present the statistic results on RX and TX architectures that have been employed in the state-of-the-art works. The papers are collected from the IEEE solid-state circuit forms: ISSCC, VLSI, CICC and ESSCIRC from 1997 to 2005. With the abbreviation of each type RX and TX architecture listed in Table VII, the distributions of each type of RX and TX employed in the modern wireless communication systems are plotted in Figures 8 and 9, respectively. The publications are listed in the References Part II [II, 1]–[II, 101]. They are classified by their applications and corresponding architectures.

For the RX, it is obvious that the dominant superheterodyne RX has been replaced by the zero-IF and low-IF solutions. The zero-IF RX has been tried for all applications except the 802.15.4 and the CDMA/WCDMA/AMPS/GPS. Whereas the low-IF RX has been widely used for narrowband applications such as Bluetooth (13 cases), GSM/DCS/PCS and 802.15.4. Dual-conversion has also been proved effective for high-frequency standards like the 802.11a and HiperLAN.

For the TX, the dominant choice is direct-up. It is not only because of its integratability and

low power, but also to match the RX path that uses zero-IF. The same considerations are applicable for two-step-up and dual-conversion. PLL TX has been used for GSM/DCS/PCS and Bluetooth due to the constant amplitude of their modulation signals. A direct modulation during frequency synthesis eliminates the need of a TX. The following sub-sections discuss the state-of-the-art RXs and transceivers (TXRs) designed for cellular, WPAN/WLAN and WLAN applications, and compare their achieved performances in relation to their architectural choice and levels of block sharing.

B. Case Study—Cellular RX for GSM/DCS/PCS/WCDMA

- **J. Ryynänen et al. [I, 16]**—it is a direct conversion RX (Figure 10) for GSM/DCS/PCS and WCDMA. It contains a single-ended bipolar LNA employing a parallel transistor to select the gain peak at different frequencies while sharing the inductors for area savings. All the circuits after the LNA are fully differential. It uses also a doubled-balanced Gilbert-cell BiCMOS mixer featuring a controllable additional resistive load in parallel with the positive and negative load resistors to reduce the even-order distortion, thereby increasing the IIP2. Two 5th-order gain-controllable channel-selection LPFs are employed at the BB, where the architecture is reconfigurable between Butterworth for GSM/DCS/PCS and Chebyshev for WCDMA. A

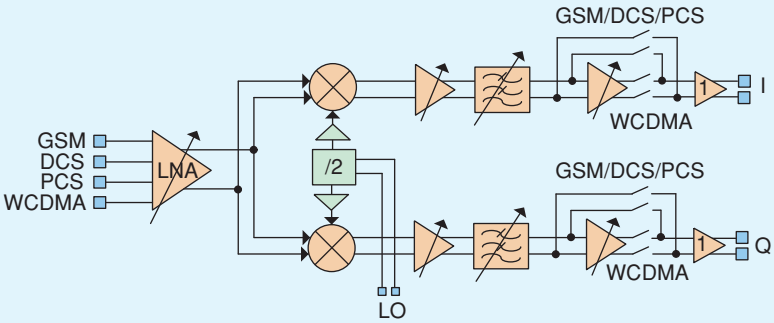

Figure 10. J. Ryynänen's GSM/DCS/PCS/WCDMA receiver.

Table VIII.
Performance summary of J. Ryynänen's GSM/DCS/PCS/WCDMA receiver.

	GSM/DCS/PCS	WCDMA
RX Architecture	Zero-IF	
Integration	Receiver (no A/D, synth. and VCO)	
Technology	0.35-μm SiGe BiCMOS	
Supply Voltage	2.7 V	
Chip Area	9.8 mm^2	
Noise Figure	2.8 to 4.8 dB	3.5 dB
IIP3	−20 to −21dB	−21 dB
IIP2	+42 dB	+47 dB
Power	42 mW	50 mW

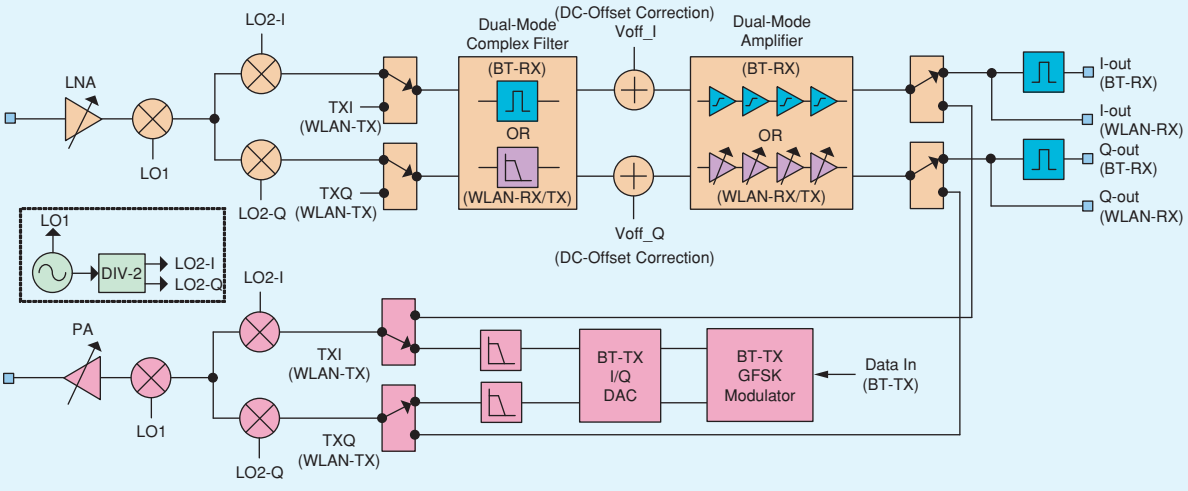

Figure 11. T. Cho's Bluetooth/802.11b transceiver.

feedback loop and ac-coupling using on-chip passives realizes -3-dB cutoff frequencies of 1 and 13 kHz, respectively. A dual-channel 8-bit A/D converter is suggested for I/Q digitization. The performance summary is listed in Table VIII.

C. Case Study—WPAN/WLAN TXRs for Bluetooth/802.11b

- **T. Cho et al. [II, 87]**—this work employs a two-step-down/up TXR architecture (Figure 11) to reduce the LO-to-LO self-mixing. The first IF is one-third of the RF to simplify the generation of the second LO (dividing by 2 the value of the first LO), whereas the second IF is 2 MHz (Low-IF) for Bluetooth and dc (zero-IF) for 802.11b. Because Bluetooth and 802.11b share the identical 2.4 GHz ISM band, the LNA, first and second down/up converters are shared as well. The channel-selection filter is a 5th-order Butterworth 1-MHz complex filter centered at 2-MHz IF for Bluetooth, whereas it is reconfigured as a 7.5-MHz LPF centered at dc for 802.11b. The amplifier is reconfigurable as a limiting and automatic gain control (AGC) for Bluetooth and 802.11b, respectively. Both the filter and amplifier are shared between the RX and TX to further save silicon area. A wideband fractional-N frequency synthesizer satisfies the diverse step size of either mode and achieves a fast RX-TX turn-around time. DC-offset correction conducts in every frame using a D/A feedback.
- **Y. Jung et al. [II, 88]**—this direct-conversion TXR (Figure 12) shares all building blocks between Bluetooth and 802.11b modes. The 6th-order Butterworth LPFs have 0.7-/5.5-MHz bandwidth for Bluetooth/802.11b. The PGAs are embedded with dc-offset cancellation loops, which realize a 1/100

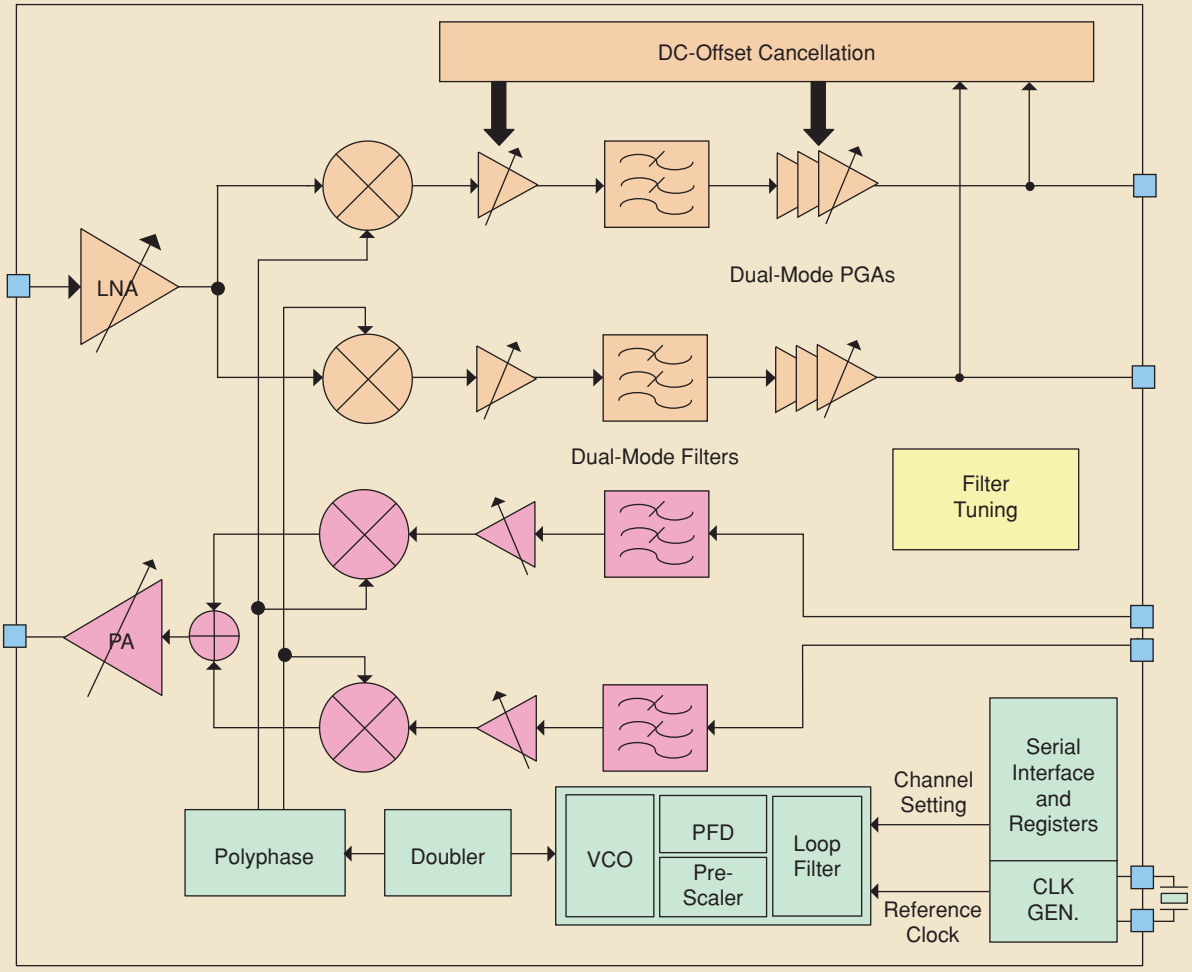

Figure 12. Y. Jung's Bluetooth/802.11b transceiver.

kHz -3-dB cutoff for Bluetooth/802.11b. A fractional-N frequency synthesizer with charge-averaging charge pump scheme for canceling low-frequency spur is used to satisfy several step sizes.

- **H. Darabi et al. [II, 86]**—this TXR, as shown in Figure 13, features a low-IF/zero-IF RX for Bluetooth/802.11b and a direct-up TX for both. A 1.6-GHz VCO self-mixes with its division-by-2 product, i.e., 0.8-GHz, to generate the 2.4-GHz LO. The LNA, first and second down/up converters are shared as both Bluetooth and 802.11b operate in the 2.4-GHz ISM band. Two channel-selection filters are implemented, one is a 5th-order 1-MHz complex filter centered at 2-MHz IF for Bluetooth, another is a 5th-order 7.5-MHz LPF centered at dc for 802.11b. For the baseband amplification, it is a limiter for Bluetooth and a PGA for 802.11b. A fractional-N frequency synthesizer satisfies diverse step sizes. Finally, the dc-offset is removed by a programmable offset cancellation loop, which refreshes the control of the -3-dB cutoff frequency in every packet.

- **Discussion**—all examples complied with the standards under the general conclusion that a low-IF is suitable for narrowband, a zero-IF is useful for wideband, or a zero-IF for both with an appropriate dc-offset cancellation technique. As compared in Table IX with the performances of the

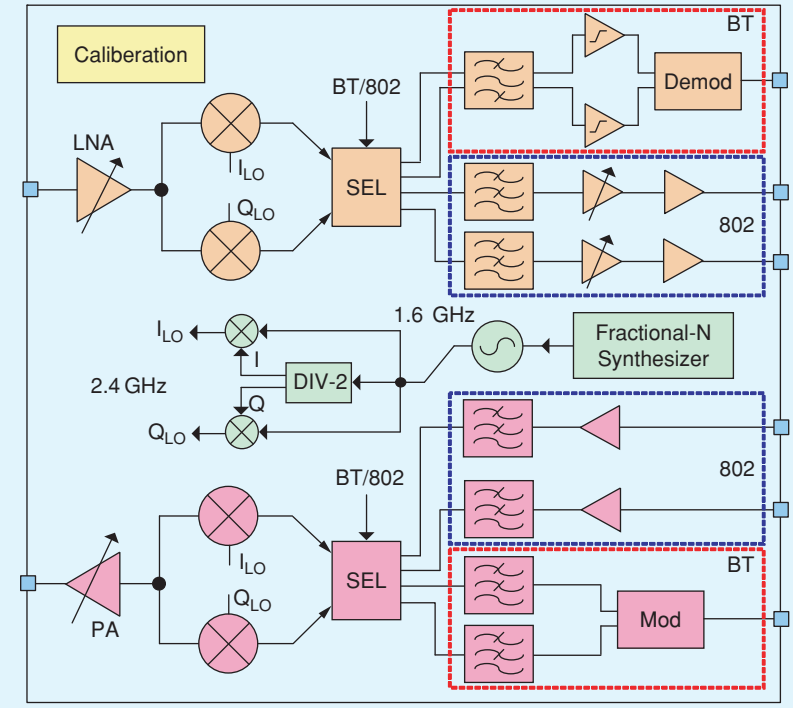

Figure 13. H. Darabi's Bluetooth/802.11b transceiver.

Table IX.
Performance comparison of Bluetooth/802.11b transceivers.

	T. Cho et al.		Y. Jung et al.		H. Darabi et al.	
	Bluetooth	802.11b	Bluetooth	802.11b	Bluetooth	802.11b
RX Architecture	Dual-Conversion with Low-IF	Dual-Conversion with Zero-IF	Zero-IF		Low-IF	Zero-IF
TX Architecture	Direct-Up	Direct-Up	Direct-Up		Direct-Up	Direct-Up
Integration	Transceiver*		Transceiver*		Transceiver*	
Technology	0.18-μm CMOS		0.25-μm CMOS		0.35μm CMOS	
Supply Voltage	1.8 V		2.7 V		3.0 V	
Chip Area	16 mm^2		8.4 mm^2		25 mm^2	
Sensitivity	80 dBm		-87 dBm	-86 dBm	-80 dBm	> -93 dBm
IIP3	-12/+14 dBm$^{\Delta}$		-15 dBm		-7 dBm^{+}	-8 dBm^{+}
Power in RX	108 mW		135 mW	175.5 mW	138 mW	195 mW
Power in TX	72 mW	126 mW	121.5 mW	162 mW	141 mW	234 mW

$^{\Delta}$: LNA high/low gain, $^{+}$: minimum gain,*: no A/D and D/A for 802.11b.

The use of traditional superheterodyne architectures has started to fade out due to its high power and high cost. Simultaneously, research and development on wireless systems have turned what seemed impractical to plausible solutions.

discussed three TXRs, the key advantage of T. Choi's TXR is its compact size due to the sharing not only of the RF front-end, but also the BB blocks between Bluetooth and 802.11b through reconfiguration, and in receive and transmit modes. However, the TX-RX turn-around time becomes an issue by permitting the use of time-continuous dc-offset cancellation loop, which results in a long settling time. Y. Jung's TXR achieves a very small area by using a direct conversion for both RX and TX. A lowpass filter with different bandwidths is much more area- and power-efficient than the realization of a polyphase/ lowpass reconfigurable filter. The dc-offset is suppressed by building a dc-offset cancellation loop in each PGA. H. Darabi's TXR shows similar general architecture with dedicated analog BB for RX and TX, in Bluetooth and 802.11b modes. The chip area is thus relatively large when compared with other devices.

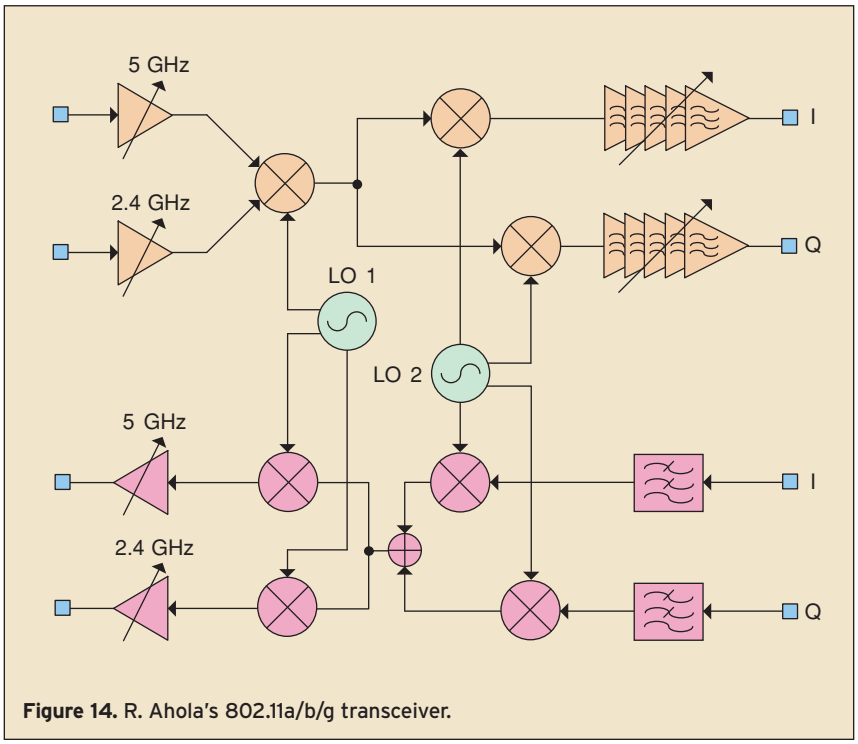

Figure 14. R. Ahola's 802.11a/b/g transceiver.

D. Case Study—WLAN TXRs for IEEE 802.11a/b/g

- **R. Ahola et al. [II, 90]**—this device uses a two-step-up/down architecture (Figure 14) to reduce the LO self-mixing. A common IF of 1.3–1.5 GHz was chosen for both 2.4-GHz and 5-GHz bands. Quadrature demodulation is performed at IF (i.e., make accurate quadrature generation easier) whereas the amplification and filtering are performed at the BB. Excluding the LNAs and power amplifiers, the building blocks are shared between all modes. Two integer-N frequency synthesizers, one generating a fixed LO at 3.84 GHz and the other generating a variable LO at 1.3–1.5 GHz, are designed. The channel-selection LPFs in the receiver and transmitter paths are 4th-order Butterworth and 4th-order Chebyshev, respectively. Their bandwidths are accurately set by a calibration engine. Two highpass poles are inserted in the receiver path; one is in front of the variable-gain amplifier (VGA), and the other is a servo loop round the LPF. The former and latter pole frequencies are <200 Hz and <1 kHz in all process corners, respectively, ensuring that multipath fading and worst-case frequency offset result in no significant performance degradation. The VGA's gain tuning resulted dynamic dc-offset is first minimized by setting the bias conditions of the amplifying devices constant in gain change. The measured dc-offset step in gain change never exceeds 10 mV with this technique.
- **Z. Xu et al. [II, 93]**—it is a direct-conversion TXR (Figure 15) for all 802.11a, b and g. Two LNAs for 2.4 and 5-GHz bands were implemented with shared mixers, channel-selection filters and VGAs. One frequency synthesizer and one VCO shares between different modes, RX and TX. The LO leakage in the transmitter is eliminated by applying a LO-leakage calibration loop. The lowpass channel-selection filter in both RX and TX is of 5th-order and offers a variable gain feature. A successive switching technique implemented in the dc-offset cancellation loop is to improve the settling time in the RX gain adjustment.

For the RX, the dominant superheterodyne RX has been replaced by the zero-IF and low-IF solutions. For the TX, the dominant choice is the direct-up because of its integrability and low power.

- **T. Rühlicke et al. [II, 99]**—as shown in Figure 16, it employs a direct-conversion in the RX for CCK mode (802.11b), but a low-IF one for OFDM mode (802.11a/g) to facilitate, mainly, the dc-offset cancellation. In the TX, two-step-up is kept in use to fulfill the RX-TX turn-around time, whereas it is direct-up for b and g. No on-chip power-amplifier is integrated. Two LNAs for 2.4- and 5-GHz bands and two channel-selection filters (two 5th-order 25-MHz Butterworth polyphase filters centered at 10MHz are used for 802.11 a and g, other two are 5th-order 8-MHz Chebyshev LPFs centered at DC for 802.11b) are implemented with shared mixers and programmable-gain controls (PGCs). The strength of the signal is indicated by a received strength signal indicator (RSSI). One frequency synthesizer with

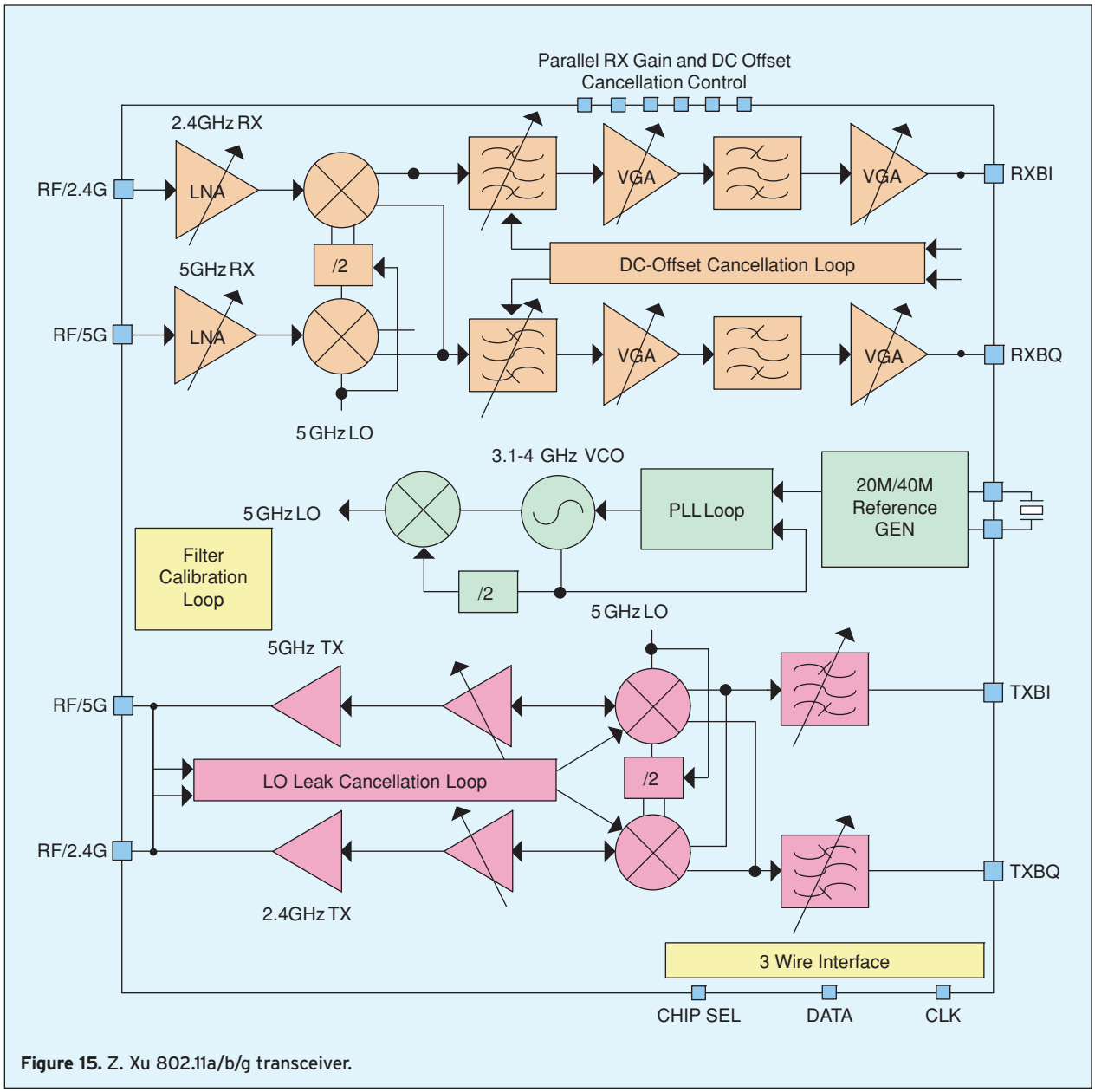

Figure 15. Z. Xu 802.11a/b/g transceiver.

VCO is used between different modes, and the receiver and transmitter. Low-dropout voltage (LDO) regulators are embedded.

- **Discussion**—Table X summarizes the performances of the three TXRs, R. Ahola's transceiver sets a common IF for 802.11a/b/g such that the problem of LO-to-LO self-mixing is reduced, whereas the IF and BB circuitries are shared. Z.

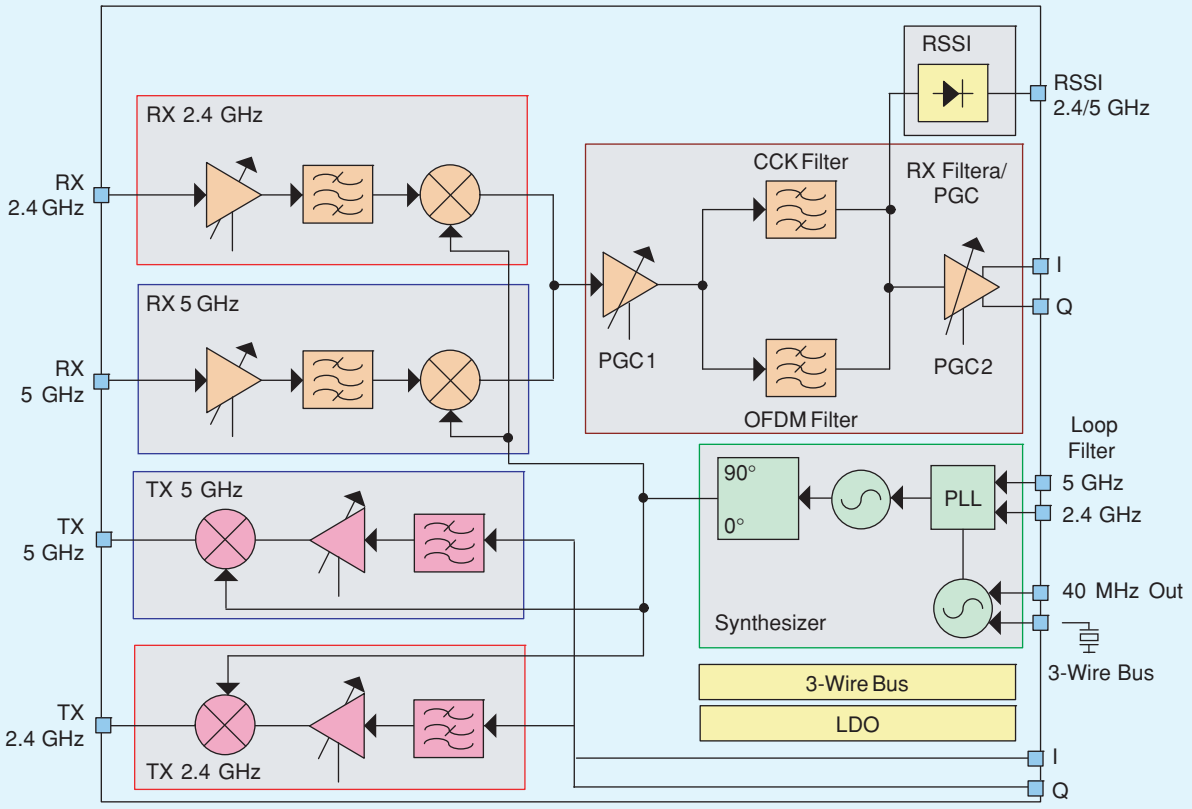

Figure 16. T. Rühlicke 802.11a/b/g transceiver.

Table X.
Performance comparison of 802.11a/b/g transceivers.

	R. Ahola et al.		Z. Xu et al.		T. Rühlicke et al.		
	802.11b/g	**802.11a**	**802.11b/g**	**802.11a**	**802.11a**	**802.11b**	**802.11g**
RX Architecture	Dual-Conversion		Zero-IF		Low-IF	Zero-IF	Zero-IF (CCK) Low-IF (OFDM)
TX Architecture	Dual-Conversion		Direct-Up		2-Step-Up	Direct-Up	Direct-Up
Integration	Transceiver*		Transceiver*		Transceiver*		
Technology	0.18-μm CMOS		0.18-μm CMOS		0.25-μm BiCMOS		
Supply Voltage	1.8 V		1.8 V		3 V		
Chip Area	12 mm^2		6 mm^2		13.5 mm^2		
IIP3 (min. gain)	-1 dBm	-11.8 dBm	-7.3/10 dBm$^{\Delta}$	-8/14.5 dBm$^{\Delta}$	–		
Noise Figure	5.2 dB	5.6 dB	4.9 dB	5.0 dB	–		
Sensitivity^{+}	–		–		-74 dBm	-85 dBm	-74 dBm
Power in RX	194.4 mW	201.6 mW	122.4 mW	115 mW	600 mW	345 mW	345 mW
Power in TX	241.2 mW	241.2 mW	136.8 mW	181.8 mW	465 mW	330 mW	330 mW

$^{\Delta}$: high/low gain, *: no A/D and D/A, $^{+}$: 54 Mb/s for a, g 11Mb/s for b.

New standards like 802.11n and WiMax together with existing ones WCDMA, 802.11a/g, and UWB are believed to be major parts of the future wireless-ubiquitous network.

Xu's transceiver directly downconverts the signal to the BB, resulting in very low power and area consumption. The problems of dc-offset in RX, and LO leakage in TX, are tackled by cancellation loops. T. Rühlicke's transceiver uses a low-IF reception for 802.11a and g in OFDM mode to facilitate the dc-offset cancellation. Two channel-selection filters are required while the wideband PGCs are shared. Their results demonstrate that low power and small area can be achieved together by zero-IF RX with direct-up TX.

VI. Conclusions

In this paper we have summarized some essential information that is worth considering during the transceiver architecture selection. Some general conclusions are drawn below:

Architecturally, to meet the goals of low power and low cost as well as high integration and multi-standard, the superheterodyne architecture should be avoided. Instead, a low-IF/zero-IF-mixed RX [I, 17] appeared as an effective architecture to meet those goals simultaneously, especially because the modern wireless standards consist of both narrowband and wideband applications. On the other hand, the dual-conversion architecture can cooperate with the low-IF and zero-IF ones in the case of a large frequency difference in the given standards. Exploiting a common IF constitutes an efficient way to alleviate the frequency synthesis, filtering and channel selection.

On circuit level, although dedicated LNAs/PAs optimized for each band are normally required for multi-band communication, inductor sharing is still efficient to save chip area. In the dual-conversion scheme, the demodulation can be performed at a common IF such that the mixers, frequency synthesizer and VCO can be shared. Since the frequency synthesizer has to provide two very different step sizes (e.g., 200 kHz and 5 MHz), in order to maintain a high reference frequency, the fractional-N PLL structure is more appropriate than its integer-*N* counterpart. Besides, TDMA standards allow the baseband building circuitry to be shared between TX and RX paths. A complex/real filter with tunable center-frequency and bandwidth can serve both low-IF/zero-IF reception and two-step-up/direct-up transmission. The bandwidth of the employed operational amplifier should be able to scale with the channel's bandwidth to save power. The A/D converter can be based on power- or resolution-scaleable architectures [I, 18], [I, 19].

Summing up, it is obvious that realizing transceivers with high multi-standardability constitutes a very challenging task as many new wireless standards are continuously being deployed, like the recent cases of 802.11n and WiMax. They together with the existing WCDMA, 802.11a/g and UWB, are believed to be the major parts of the future wireless-ubiquitous network. Developing *effective* transceiver solutions that help supporting all (most of) those standards in one terminal will be a very important direction of wireless research in the coming years.

Acknowledgements

This research is financially supported by the Research Committee of University of Macau.

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