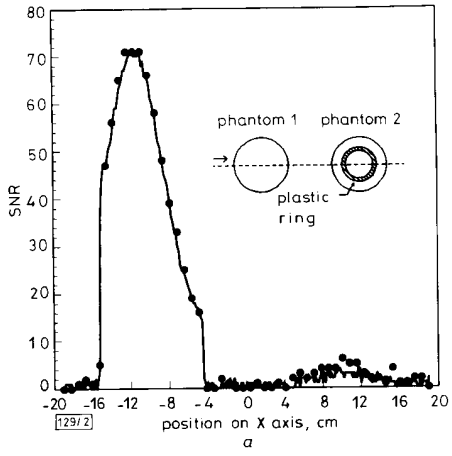
1. In each case images were obtained with $TR = 0{\cdot}3$ s, $TE = 23$ ms, 1 acquisition, 5 cm slice thickness, a 38×38 cm^2 field of view with 256×256 resolution. Acquisition time was 1·3 min per image.

First, separate images were obtained from each coil. The setup from Fig. 1 was modified by removing the crystal filters, second preamplifiers, and the RF switch. For each image, the output from the appropriate preamplifier was directly connected to the receiver. The unused coil was matched and terminated in 50 Ω. Total acquisition time for both images was 2·6 min.

Images were then obtained simultaneously from both coils using the multiplexing system shown in Fig. 1. The same imaging parameters were used, except a 256×512 imaging matrix was used to provide 256 samples of the echo from each coil. In this case, total acquisition time for both images was only 1·3 min. Following reconstruction, the SNR was compared between multiplexed and single channel images. Fig. 2*a* and *b* show relative SNR against position curves for one line through the centre of the images obtained with coil 1 and 2. The shapes of the SNR curves reflect the sensitivity pattern of the receiver coils. Signal dropouts due to a plastic ring inserted into phantom 2 are seen in Fig. 2*b*. The SNR from coil 2 was lower in both cases due to a difference in cabling and preamplifiers. However, no decrease in SNR resulted from the multiplexing. Time multiplexing of the two coils resulted in a decrease in imaging time by a factor of 2 with no penalty in SNR or image contrast.



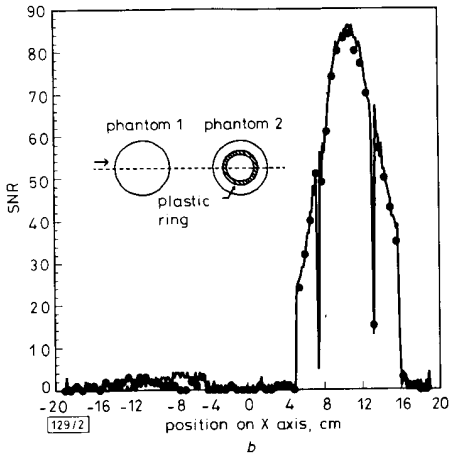


Fig. 2 *Comparison of relative SNR obtained from separately obtained images and multiplexed images*

——— SNR (normal)
● SNR (multiplexed)
Curve represents relative SNR along one line intersecting both phantoms
a Coil 1
b Coil 2

Acknowledgments: The authors gratefully acknowledge support of this project by Medical Advances, Inc. and the Texas Board of Higher Education under TATP grant no. 03-198.

24th October 1991

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OPTIMUM MULTISTAGE MULTIRATE SWITCHED CAPACITOR ARCHITECTURES FOR HIGHLY SELECTIVE INTERFACE FILTERING

R. P. Martins and J. E. Franca

Indexing terms: Filtering, Switched capacitor filters, Analogue–digital conversion

Based on the cascade of switched capacitor decimating sections, with optimum implementation and operating with multiple clock rates, a new design methodology is proposed for implementing highly selective filtering functions for analogue–digital interface systems. When compared with more traditional designs, the proposed solution demonstrates remarkable savings both with respect to the capacitance spread and total capacitor area, and the speed at which the operational amplifiers have to operate. Both attributes are paramount for applications where chip size and power consumption are at premium.

Introduction: Integrated analogue–digital interface systems are currently receiving significant attention worldwide because of the increasing trend to combine in the same chip both analogue and digital signal processing circuitry to reduce the cost of manufacturing mixed-signal application specific integrated circuits and to improve their performance and reliability. One of the main functions to be performed in such analogue–digital interface systems is the antialiasing filtering of the incoming analogue signals. A widely used, mature solution for the CMOS implementation of antialiasing filters consists of the combination of a low selectivity continuous-time active-RC prefilter followed by a highly selective switched capacitor (SC) filter clocked at a rate much higher than the maximum frequency of the analogue signals, as is schematically shown in Fig. 1. A popular solution for the design of such high selective SC filters is based on the cascade of first and second order filter sections [1] but this, despite its simplicity, can still lead to some practical difficulties for integrated circuit implementation. One such difficulty concerns the large capacitance ratios that may arise because of the typically high clocking

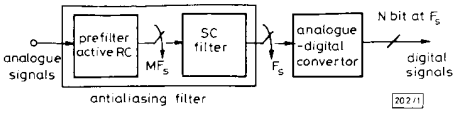

Fig. 1 *Typical architecture of analogue–digital interface system*

rates at which the cascade sections have to operate, and the other is inherently related to the need of employing in such sections high speed operational amplifiers (OAs) that have to settle within rather short clock pulses. Both difficulties may be unsurmountable in applications where chip size and power consumption are at a premium, as in the case of portable communication equipments.*

The purpose of this Letter is to describe an alternative methodology for designing with very low capacitance spread and reduced power consumption highly selective antialiasing SC filters for analogue–digital interface systems, which is based on the cascade of SC decimating sections, with optimum implementation and operating with multiple clock rates. This is illustrated by the example of a 10th order elliptic bandpass antialiasing filter with input clock rate as high as 1·152 MHz for a maximum passband frequency of 3·4 kHz [2]. A comparison with the more traditional design solutions demonstrates remarkable savings concerning both the capacitance spread and total capacitor area and the required operating speed of the OAs.

Multistage single-rate architectures: The classical implementation of a multistage single-rate SC filter is based on the cascade of SC integrators and biquads [3] and the general z-transfer function can be expressed as

$$H(z^{-1}) = k \prod_{i=1}^{F+S} H_i(z^{-1}) \tag{1}$$

where k is a gain factor and the unit delay period corresponds to $1/MF_s$. The order of the denominator polynomial is $N = 2S + F$ with F and S representing, respectively, the number of first and second order filter sections $H_i(z^{-1})$. The design procedure involving the pairing of poles and zeros and their assignment to the various sections is usually carried out to maximise dynamic range and reduce capacitance spread [4]. This, however, may still be too large because of the high clocking rate MF_s and the large ratios that can result between this and the pole/zero frequencies assigned to some sections. Another disadvantage of such architecture is the very high speed requirements of the AOs, which must all operate at MF_s.

* GUILHERME, J., MARTINS, P., and FRANCA, J. E.: 'An audio processor ASIC for a portable radiotelephone'. To be published

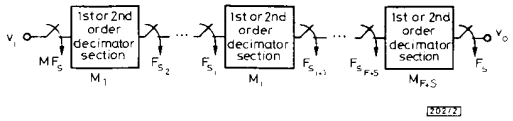

Fig. 2 *Optimum multistage multirate architecture for highly selective SC antialiasing filtering*

Multistage multirate architectures: An improved alternative solution to the above multistage architecture consists also in the cascade of SC integrators and biquads but which are now operated with different clock rates F_{s_i}, being MF_s and F_s, respectively, at the input and output sections. This leads to the modified z-transfer function

$$H(z^{-T_i}) = k \prod_{i=1}^{F+S} H_i(z^{-T_i}) \tag{2}$$

where the delay periods $T_i = MF_s/F_{s_i}$ correspond to the ratios between MF_s and the different values F_{s_i}. For deriving the above modified z-transfer function (eqn. 2) it is no longer possible to carry out the traditional synthesis procedure based on an optimum pole-zero pairing. Instead, we have to derive $F + S$ different z-transfer functions corresponding to each one of the SC sections, and such that the combined amplitude responses meet the original specifications of the overall multistage circuit both for the baseband and antialiasing responses. In comparison with the previous single-rate architecture, this makes it possible to relax the speed requirements of the OAs, except for those placed at the input of the cascade which are still operating at MF_s. Some savings are also obtained for the capacitance spread and total capacitor area because the ratio between F_{s_i} and the different pole/zero frequencies are gradually reduced from the input to the output of the cascade [5].

Optimum multistage multirate architectures: To obtain much further reductions of the capacitance spread, total capacitor area and speed requirements of the OAs, an alternative multistage multirate solution is schematically presented in Fig. 2 [2], which employs optimum 1st and 2nd order SC decimator building blocks [6] clocked at multiple rates. In such buildings blocks, whose general architectures are shown in Fig. 3 [6], the sampling rates at the input F_{s_i} and at the output $F_{s_{i+1}}$ are related by the decimation factor $M_i = F_{s_i}/F_{s_{i+1}}$. Because the optimum circuit implementation requires OAs operating only at the lower output sampling rate $F_{s_{i+1}}$, this yields considerable savings in power consumption. The overall z-transfer function of the optimum multistage multirate architecture can be expressed as

$$H'(z^{-M_i \cdot T_i}) = k \prod_{i=1}^{F+S} H_i'(z^{-M_i \cdot T_i}) \tag{3}$$

where the delay periods in each decimating section correspond now to integer multiples of $(M_i T_i)$, and the normalised periods T_i are obtained from

$$T_i = \prod_{j=1}^{i-1} M_j \qquad T_1 = 1 \tag{4}$$

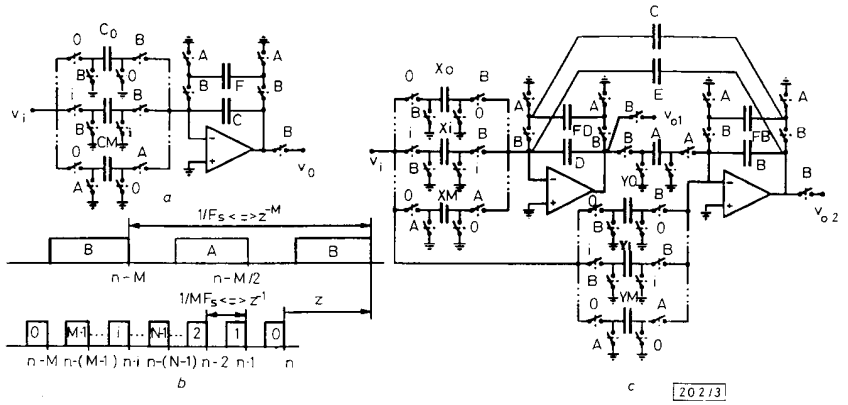

Fig. 3 *IIR SC decimator building blocks with optimum circuit implementation* [6]

a First order
b Switching waveforms
c Second order

The functions $H_i(z^{-M_i \cdot T_i})$ are obtained after the transformation of each $H_i(z^{-T_i})$ in eqn. 2 for optimum implementation [6, 7].

The design methodology for selecting a particular decimating sequence in the above architecture is determined in conjunction with the assigment of poles and zeros to each decimator building block and by taking into account the corresponding frequency-translated aliasing responses [2, 6]. This makes it possible not only to obtain the desired baseband specifications, as in multistage single-rate filter designs, but also the specified antialiasing filtering response. To obtain the preferred sequence of pole-zero-period combination, we must consider the following criteria:

(i) decompose M in prime factors by descending order, to minimise the speed requirements of the OAs

(ii) associate the larger values of the pole/zero frequencies to the lower values of T_i, i.e. minimise F_{si}/f_{pi} and F_{si}/f_{zi}, to minimise capacitance spread and total capacitor area

(iii) implement first lowpass decimator stages with low selectivity poles, i.e. low Q_p, and wide transition bands to reject the alias frequency components at higher frequency

(iv) implement high selectivity lowpass decimator stages at the heart of the cascade structure to increase the attenuation of those aliasing frequency components closer to the passband

(v) implement all high pass decimator stages at the end of the cascade structure, because they only contribute to the definition of the lower stopband of the baseband response.

Design example: To illustrate the proposed methodology and its advantages compared to the more traditional ones, we have designed a multistage SC bandpass antialiasing filter appropriate for application in the receive channel of a voiceband analogue interface system [2]. This filter exhibits a 10th order elliptic amplitude response, obtained by the cascade of five 2nd order decimating sections, with an input sampling rate of 1·152 MHz and an overall sampling rate reduction factor of $M = 120$. This leads to an oversampling ratio of approximately 340 for the passband signals, for which it is sufficient to consider a mere 1st order RC continuous-time prefilter in front of the SC antialiasing filter. The overall antialiasing SC decimating filter possesses a maximum capacitance spread and total capacitor area, respectively, of only 48 and 530. The nominal computer simulated baseband amplitude response is shown in Fig. 4*a*, whereas the response around the most critical aliasing band at 76·8 kHz is shown in Fig. 4*b*, yielding an aliasing rejection of 80 dB which is well above the required specification. The comparison with the two other multistage design methodologies mentioned in this letter is given in Table 1, showing the remarkable advantages of the proposed solution not only in terms of capacitance spread and total capacitor area but also considering the speed requirements of the OAs.

Conclusions: We present a new design methodology for the implementation of highly selective multistage SC filters appropriate for analogue–digital interface filtering, which is based on the cascade of 1st and 2nd order decimating sections, with optimum implementation and multiple clock rates. The application of this methodology to a practical design example of an SC bandpass antialiasing filter for a voiceband analogue interface system shows significant advantages over traditional solutions when comparing the resulting capacitance spread and total capacitor area as well as the speed requirements of the amplifiers.

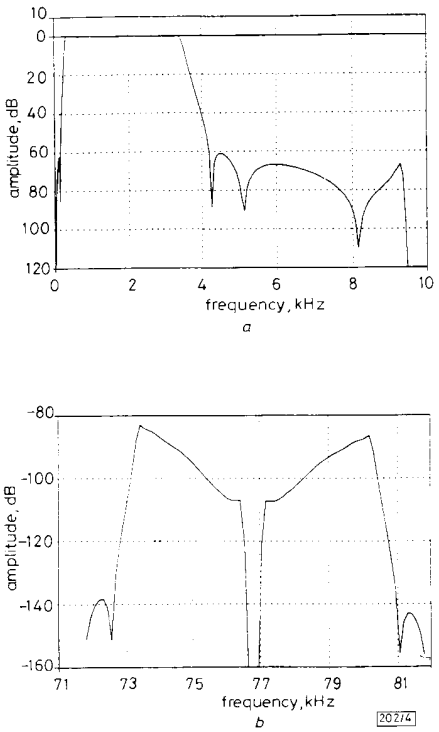

Fig. 4 *Computer simulated amplitude response of optimum SC bandpass decimator*

a Baseband from DC–9·6 kHz
b Aliasing band around 76·8 kHz

9th November 1991

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Table 1 COMPARISON BETWEEN THREE DIFFERENT MULTISTAGE DESIGNS OF SC BANDPASS ANTIALIASING FILTER WITH INPUT SAMPLING RATE OF 1·152 MHz AND OUTPUT SAMPLING RATE OF 9·6 kHz

Design	Spread	Total area (u.c.)	Clock rates defining the speed requirements of the amplifiers (kHz)
Single rate	840	5200	10 OAs at 1152
Multirate	550	1250	2 OAs at 1152, 2 OAs at 384, 2 OAs at 76·8, 2 OAs at 38·4, 2 OAs at 19·2
Optimum* multirate	48	530	2 OAs at 384, 2 OAs at 76·8, 2 OAs at 38·4, 2 OAs at 19·2, 2 OAs at 9·6

* $M_1 = 3, M_2 = 5, M_3 = 2, M_4 = 2, M_5 = 2$

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COPLANAR WAVEGUIDE APERTURE COUPLED PATCH ANTENNAS WITH GROUND PLANE/SUBSTRATE OF FINITE EXTENT

R. N. Simons and R. Q. Lee

Indexing terms: Antennas, Microstrip, Aperture coupled antennas

Coplanar waveguide (CPW)/aperture coupled microstrip patch antennas constructed with ground coplanar waveguide (GCPW), finite coplanar waveguide (FCPW) and channelised coplanar waveguide (CCPW) are demonstrated. The measured characteristics show that the CCPW/aperture coupled microstrip patch antenna has the largest bandwidth, whereas the GCPW/aperture coupled microstrip patch antenna has the best front-to-back ratio.

Introduction: Coplanar waveguide/aperture coupled microstrip patch antennas have attracted much attention because of their suitable geometry for monolithic integration and their broader bandwidth characteristics. Recently, a coplanar waveguide/aperture coupled microstrip patch antenna has been demonstrated and found to have excellent performance characteristics [1]. In this Letter the relative performance of three CPW/aperture coupled patch antenna configurations are compared. The configurations are constructed using a grounded coplanar waveguide (GCPW), a finite ground plane coplanar waveguide (FCPW) [2] and a channelised coplanar waveguide (CCPW) [3]. The performance parameters investigated include modes supported by the CPW feed structure, coupling efficiency, radiation pattern, front-to-back ratio, and bandwidth.

Feed design, fabrication and patch integration: The cross-section view of a GCPW feed is shown in Fig. 1*a*. The semi-width G of the upper ground plane of the GCPW is chosen to be greater than the coplanar waveguide wavelength λ_g at the patch resonance frequency. Consequently, the width $2B$ of the GCPW is greater than $2\lambda_g$. The widths of the centre strip conductor and the slot, denoted as S and W respectively, are chosen to provide a good impedance match to a coaxial connector.

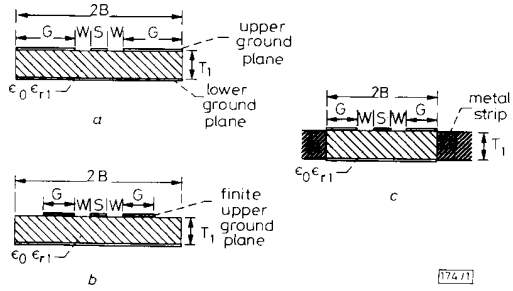

Fig. 1 *Cross-section view of coplanar waveguide (CPW)*
Feeds:
a Grounded CPW:
$S = 0{\cdot}762$ mm, $W = 0{\cdot}254$ mm, $G = 24{\cdot}765$ mm, $\varepsilon_{r1} = 2{\cdot}2$, $T_1 = 0{\cdot}508$ mm, $2B = 50{\cdot}8$ mm
b Finite CPW:
$G = 3{\cdot}937$ mm
c Channelised CPW:
$G = 3{\cdot}937$ mm, $2B = 9{\cdot}144$ mm

The cross-section view of a FCPW feed is shown in Fig. 1*b*. Unlike the GCPW, the upper ground plane of the FCPW is smaller than its lower ground plane. The semi-width G of the FCPW tested is less than $0{\cdot}25\lambda_g$. The other parameters such as the total width $2B$, S and W are the same as for the GCPW.

Fig. 1*c* shows the cross-section view of the CCPW feed. The entire feed structure is very small, and in this example, G and $2B$ are less than $0{\cdot}25\lambda_g$ and $0{\cdot}5\lambda_g$, respectively. The widths S and W are the same as for the GCPW. Further, along the vertical sides of the substrates, metal strips are placed. These metal strips not only provide mechanical support and heat sinking but form a channel with the lower ground plane that provides additional isolation between feed lines in an array.

The integration of the GCPW feed with a patch antenna is shown in Fig. 2*a*. The patch is electromagnetically coupled to the feed through an aperture as explained in Reference 1. Integration for the two other feed structures is realised by replacing the GCPW feed substrate with an FCPW or a CCPW feed substrate as shown in Fig. 2*b* and *c*, respectively.

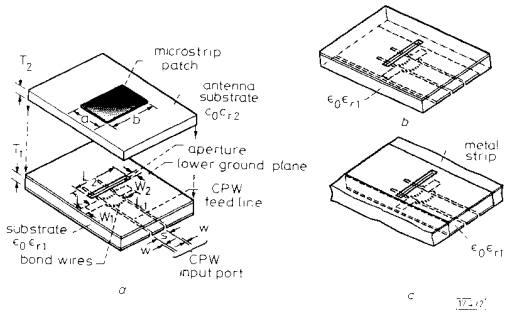

Fig. 2 *Schematic diagram showing integration of CPW feeds with microstrip patch antenna*
a Grounded CPW:
$W_1 = 0{\cdot}762$ mm, $L_1 = 2{\cdot}794$ mm, $L = 6{\cdot}858$ mm
$W_2 = 0{\cdot}254$ mm, $L_2 = 6{\cdot}91$ mm, $\varepsilon_{r2} = 2{\cdot}2$
$T_2 = 0{\cdot}254$ mm, $a = 7{\cdot}6$ mm, $b = 11{\cdot}4$ mm
b Finite CPW
c Channelised CPW

Experimental antenna performance and discussions: The measured performance of the antenna in Fig. 2 over the frequency range of 13·0–14·0 GHz is summarised in Table 1. Because the extent of the ground planes in a GCPW feed is several wavelengths, the feed supports parallel plate modes guided between the CPW plane and the lower conducting plane [4]. These spurious modes are manifest as resonance spikes in a S_{11} measurement made without the patch in place. By reducing the ground plane dimensions as in an FCPW or CCPW feed, the spurious modes are suppressed and give rise to fewer resonance spikes. In all three examples, the measurements show that the magnitude of S_{11} with the patch in place is better

Table 1 RELATIVE PERFORMANCE OF CPW/APERTURE COUPLED MICROSTRIP PATCH ANTENNA CONFIGURATIONS

Transmission line	GCPW	FCPW	CCPW
Spurious modes	Several	Few	Few
Coupling to patch	Excellent	Excellent	Excellent
Radiation pattern	Excellent	Excellent	Excellent
Front-to-back ratio (dB)			
E plane	10·8	10·2	10·3
H plane	14·0	11·1	12·4
2 : 1 VSWR bandwidth (%)	2·3	3·6	4·2
Fabrication	Simple	Simple	Complex
Cost	Low	Low	High