A 2.5-V 57-MHz 15-Tap SC Bandpass Interpolating Filter With 320-MS/s Output for DDFS System in 0.35-μm CMOS

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***Abstract*—A switched-capacitor (SC) bandpass interpolating filter is proposed with the capability of achieving, simultaneously, channel selection and frequency up-translation, together with sampling rate increase, in a multirate configuration at high frequency. This filter has been designed for efficient use in a direct-digital frequency synthesis (DDFS) system with considerable rewards in terms of speed reduction of the digital core plus the digital-to-analog converter (DAC), as well as in the relaxation of the continuous-time (CT) smoothing filter order. It exhibits a 15-tap finite impulse response (FIR), with a bandpass frequency response centered at 57 MHz and a stop-band rejection higher than 45 dB. At the same time, it translates 22–24 MHz input signals at 80 MS/s, to the frequency range of 56–58 MHz in the output at 320 MS/s, allowing also a perfect operation at 400 MS/s, in 0.35-μm CMOS technology. To implement a specific multi-notch FIR function, the filter architecture will comprise an effective low-speed polyphase-based interpolation structure with autozeroing capability, high-speed SC circuitry with fast opamps, and also ultra-low timing-skew multiple phase generation in order to achieve high-performance operation at high frequency. The prototype ICs present a signal-to-noise-and-distortion ratio (SNDR) of 61 dB, with a dynamic range of 69 dB, for 1% THD, and 61 dB, for 1% IM3. It consumes 2 mm^2 of active silicon area, 120 mW (analog) and 16 mW (digital) power, with a single 2.5-V supply, which corresponds to 8.6 mW of analog power per zero.**

***Index Terms*—Autozeroing, bandpass filters, CMOS analog integrated circuits, direct-digital synthesis, frequency-translated filtering, interpolation, multirate signal processing, sampled data circuits, signal sampling/reconstruction, switched-capacitor filters.**

I. Introduction

TRENDS IN high-speed communications demand that high-frequency analog filtering, which has traditionally been implemented by external analog components, be integrated as much as possible on a system chip. Switched-capacitor (SC) filters provide higher dynamic range with high accuracy and programmability of the time constants without requiring any tuning system, which is usually needed for continuous-time (CT) filters. However, the need for high gain and bandwidth operational amplifiers (opamps) in standard SC circuits, for high frequency of operation, results in higher power consumption and also reduced design headroom. Several topologies using double-sampling [1]–[3], precise opamp gain (POG) approach [3], pseudo-differential approach [1], or parallel N-path [4], [5], as well as multirate [5]–[8] techniques have been proposed for high-frequency applications. Among them, the multirate solution leads to extra benefits in the simplification of CT antialiasing or smoothing filters together with a significant speed relaxation also in data conversion and DSP core operation [9].

Frequency-translated sampled-data analog (SDA) filtering, which emerged from multirate signal processing, was introduced first in very narrow-band filtering [10] and later extended to other areas, from which we can select the notable example of the radio wireless receiver [7], [11], [12], that comprises a subsampling architecture using decimation filtering to realize, simultaneously, the combined functions of channel selection and frequency downconversion. However, complementary to SDA decimation filtering, where operation at the highest frequency relies mainly on passive input sampling, interpolation filtering faces the obstacle of achieving with active circuitry, accurate output signals at the system's highest sampling rate. In addition, traditional SDA interpolating filter response seriously suffers from frequency-shaping imposed by the multiple zero-notch characteristic within the output Nyquist band, due to the sampled-and-held (S/H) nature of input signals at the lower rate [13]. Moreover, image sidebands and fixed pattern-noise tones, induced by phase timing-skew error and dc offset effects, respectively, located within the output Nyquist band and without inherent attenuation by the system response (as it happens in decimation filtering), will degrade the signal purity and are significantly important in the frequency-translated mode, especially in operation at high frequency. Therefore, the highest output sampling rates reported in SC interpolating filters were both achieved in the baseband filtering path of a GSM transmitter, one at 13 MHz (third-order low-pass) [14] and another at 8.667 MHz (fourth-order low-pass) [15]. Furthermore, the highest output sampling rate reported in a CMOS SC filter was 200 MS/s in a low-pass biquad section (with POG and double-sampling) that employed an extra gain-control closed loop to compensate the finite gain effect [3].

This paper presents the design and implementation of a multirate SC bandpass interpolating filter with 57-MHz center frequency, a stop-band rejection larger than 45 dB, and a typical 320-MS/s output (which can be moved further up to 400 MS/s with a stop-band rejection around 40 dB), for a 8-bit direct-

Manuscript received February 21, 2003; revised July 17, 2003. This work was supported by the Research Committee of University of Macau, Instituto Superior Técnico /Universidade Técnica de Lisboa, and Fundação Oriente.

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Digital Object Identifier 10.1109/JSSC.2003.820855

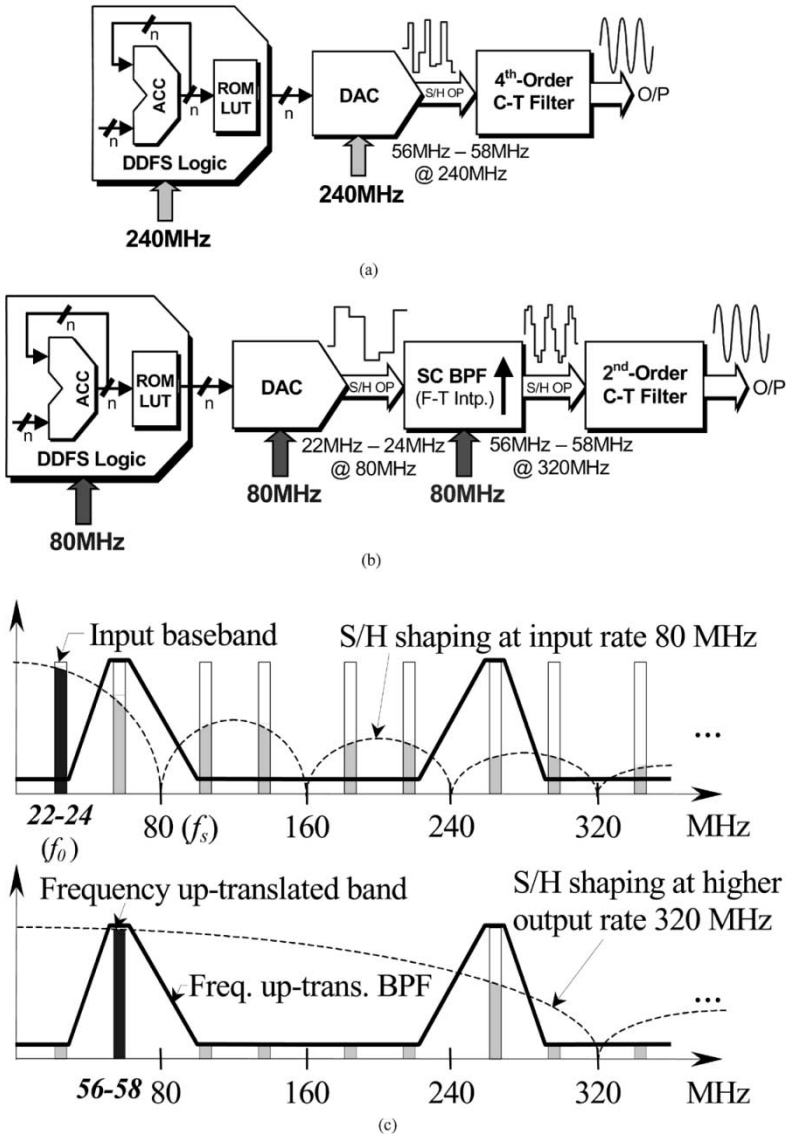

Fig. 1. ROM-based DDFS system architecture. (a) Traditional. (b) Proposed with frequency-translated SC bandpass interpolation filtering. (c) Signal spectrum of (b).

digital frequency synthesis (DDFS) system in 0.35-μm CMOS technology, with a single 2.5-V supply [16]. This interpolating filter implements with extreme precision (overcoming most of the aforementioned obstacles) a 15-tap-weighted finite impulse response (FIR) system function and performs a fourfold sampling rate increase, embedding also a 2-MHz frequency-band up-translation.

Section II will briefly present the alternative solution of using frequency-translated interpolation filtering mode in a DDFS system. In Section III, an improved polyphase-based multirate system topology with its specific multi-notch FIR system function will be described. The corresponding SC circuit implementation and layout, which were designed considering different practical nonidealities, will be presented in Section IV. Section V reports the experimental results obtained from the prototype test chips. Finally, in Section VI, conclusions will be drawn containing a summary of this work and its significance in SDA high-frequency filtering.

II. Frequency Up-Translated Filtering for DDFS

DDFS systems have been increasingly employed in modern wireless communications systems. To synthesize a desired tone (sine-wave signal) in the 56–58-MHz frequency band used in the DECT system, the traditional ROM-based DDFS system includes a digital phase accumulator with phase-to-sine amplitude ROM look-up table, followed by a linear digital-to-analog converter (DAC) which operates at a frequency that must be three to four times higher than the signal band (thus, at 240 MS/s) so as to simplify the CT smoothing filter, as shown in Fig. 1(a). However, this conventional architecture implies the need of a fourth-order CT filter together with complex on-chip tuning circuitry. Here, we propose a new architecture, as presented in Fig. 1(b), that is characterized by the insertion of an SC bandpass interpolating filter between the DDFS digital core plus DAC (DDFS + DAC) and the CT filter, to allow the translation of a 22-24-MHz frequency

band to 56-58 MHz, including an embedded sampling rate increase from 80 to 320 MHz. This arrangement determines first a threefold speed relaxation of the DDFS + DAC to only 80 MS/s, with also a lower value of the synthesized signal frequencies at 22-24 MHz, and allows later a twofold order reduction of the CT filter (which can be implemented by a simple biquad section). Hence, the design headroom and performance of those blocks will be also significantly enhanced with considerable gains in the overall system area and power consumption. The spectral characteristic of this new architecture which combines the DDFS + DAC and the frequency-translated SC bandpass filter is presented in Fig. 1(c). The frequency-translated bands of the DDFS + DAC output signal baseband, centered at f_0, appear at the multiples of the clock rate f_s, i.e., $nf_s \pm f_0$. Thus, the frequency up-translation interpolation is achieved by selecting the desired frequency band and rejecting the remaining unwanted ones through bandpass filtering plus sampling rate increase. The resulting up-translated signals can be further smoothed by either a simple low-pass or bandpass analog filter. The sampled-and-held nature of the DDFS + DAC output signal introduces different gain errors in each frequency band according to the $\sin x/x$ shaping at lower 80 MHz (typical in SDA interpolation) that must be compensated by an extra degree of functionality of the SC bandpass interpolating filter [13].

III. System Topology

A. Multi-Notch FIR System Function

To meet the aforementioned requirements of the DDFS system, if an infinite impulse response (IIR) function is selected, it will be necessary to adopt a sixth-order with $Q > 20$ to achieve the stop-band rejection higher than 45 dB. However, its implementation will result in poor passband sensitivity that cannot be compensated by precise post-tuning of the sampling clock, as widely used in standard high-Q SC filtering [1], [4], due to the process of frequency band translation. Moreover, since an IIR multirate transformation [17] is also necessary, it will lead to a high value of 25 nonrecursive filter taps. Conversely, FIR function with lower passband sensitivity still demands 30 (Parks–McClellan) or even 40 taps (Windowing), simultaneously, with an unacceptable coefficient spread. Hence, in order to overcome these disadvantages, an FIR function with specific optimum zero-placement as shown in the zero-plot diagram of Fig. 2 will be employed here. The zeros are placed at the input and unwanted imaging bands either exactly on the spot or in the nearby region, to ensure the necessary image rejection, as well as to eliminate the spurs occurring close to the passband and imposed by the dc modulation of the DAC output offset. The final number of zeros and their locations are determined and optimized by a Monte Carlo sensitivity analysis that takes into account also practical capacitance ratio mismatches. Then, an FIR function with 15-tap weights meets the adequate requirements of the application with a very satisfactory maximum spread of only 6.

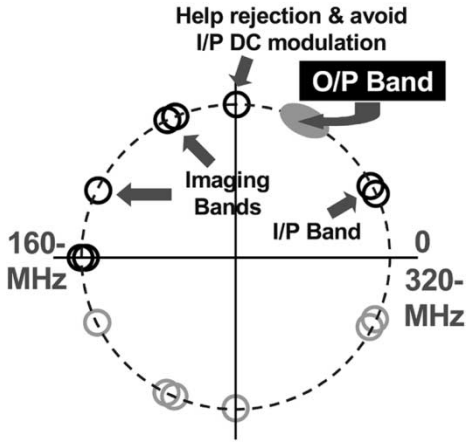

Fig. 2. Zero-plot of 15-tap multi-notch FIR function.

B. Improved Polyphase Interpolation Structure

The polyphase interpolation structure will allow the decomposition of the original 15-tap FIR system function into L subfilters $H_m(z^L)$ leading to

$$\begin{aligned} H(z) &= \sum_{n=0}^{14} h_n \cdot z^{-n} \\ &= \sum_{m=0}^{L-1} H_m(z^L) \cdot z^{-m} \\ &= \sum_{m=0}^{L-1} \left(\sum_{i=0}^{I_m-1} h_{iL+m} z^{-iL} \right) \cdot z^{-m} \end{aligned} \tag{1}$$

where $L = 4$ is the interpolation factor and I_m is the minimum integer satisfying $I_m \geq (14-m)/L$. Consequently, each polyphase subfilter $H_m(z^L)$ will efficiently operate at the lower input sampling rate of 80 MHz (with its own output accumulator) with the proper circuit structure to eliminate the $\sin x/x$ shaping gain error, over the entire frequency axis [13].

In each polyphase subfilter, there will be a maximum delay value of 12 period units that are not easily achieved only by active coefficient branches. A possible solution would be to use a complex rotating switching matrix that will result in a significant increase of the overall area, digital circuitry, layout, and routing complexity, as well as parallel-path mismatch sensitivity. Thus, a better alternative was chosen for the design that uses an active delayed block (ADB) polyphase structure where the subfilters share a common low-speed serial ADB delay line.

Normally, SC ADBs and accumulators are affected by opamp dc offsets, charge injection, and clock feedthrough that impose a fixed pattern noise level which must be kept low enough, implying that the overall subfilter path offset should be controlled through the standard deviation given by [18]

$$\sigma_{os} = \frac{A}{\sqrt{2}} \cdot 10^{-\mathrm{SNR}_{os}/20} \tag{2}$$

where A is the signal amplitude. Thus, if $\mathrm{SNR}_{os} > 45$ dB, then $\sigma_{os} < 2$ mV, which would be hardly achieved in a standard CMOS process without special compensation techniques, especially at the filter order and operating frequency required in this

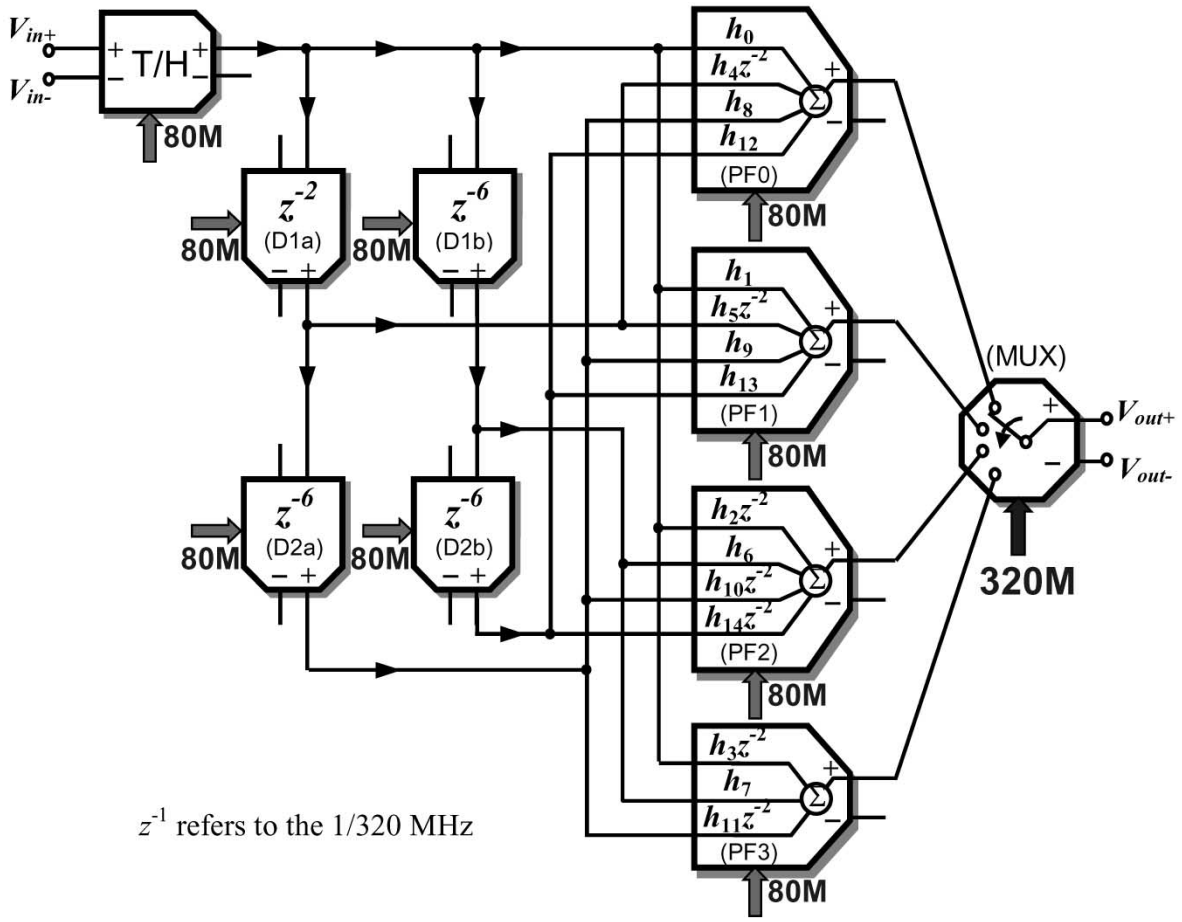

Fig. 3. Time-interleaved serial ADB polyphase structure with autozeroing.

application. Hence, the autozeroing technique is used to overcome such offset effects. In order to minimize the number of serial ADBs and its respective power consumption and error accumulation, a specific time-interleaved serial ADB polyphase structure (with autozeroing configuration) has been designed, as shown in Fig. 3. This structure implements a specific delay for each coefficient through an optimum combination of a time-interleaved signal path, that usually comprises multi-unit ADB cells, plus delay-free or multi-unit delay polyphase branches. Finally, only four ADBs are required for the 15-tap FIR system function. An important feature of this architecture is the fact that both the ADBs and accumulators (for each polyphase subfilter), which constitute the most power-hungry and accuracy-dependent core of the filter, will fully operate at the input lower sampling rate of 80 MHz, thus leaving only the simpler operation at the higher output rate for the output counterclockwise multiplexer (MUX).

IV. SC Circuit Implementation

The filter was implemented with a fully differential architecture in 0.35-μm double-poly triple-metal CMOS technology with a single 2.5-V supply and 0.95-V common-mode level. The simplified schematic of the circuit and clock phases are presented in Fig. 4. It contains the autozeroed filter core composed by the SC ADBs and polyphase subfilters, the input track-and-hold (T/H), and the output high-speed MUX stage.

A. Low-Speed SC ADB and Polyphase Subfilters With Autozeroing

The low-speed autozeroed SC ADBs are designed with the use of parallel and rotating-switching SC branches with charge-transfer-free property to obtain multi-unit delays [18], such as D1a and D2a for z^{-2} and z^{-6}, respectively, as shown in Fig. 4. Note that extra switches like *sw*1 and *sw*2 (or *sw*1' & *sw*2') in D2a are mandatory to break the resistive paths during the charge-holding phase, thus eliminating the signal-dependent clock-feedthrough and charge-injection errors. The sampling/holding capacitor is chosen at 0.48 pF as a compromise value obtained after considering different factors including the slew rate, gain bandwidth, and noise headroom.

The autozeroed polyphase subfilters (with $m = 0$ and 2 only for simplicity) and their individual accumulators are also presented in Fig. 4. The filter tap weights are implemented as direct capacitance ratios between the SC branches and the feedback/summing capacitor, either through in-phase direct charge coupling or out-phase charge transferring. To minimize the time-interleaved paths and relax the speed of the MUX, the polyphase subfilters $m = 0, 1$ and $m = 2, 3$ are especially designed to operate at different clock phases, A and B, respectively.

The unit capacitance values are chosen as 100 and 150 fF (considering several factors such as noise, matching, and speed), respectively, for subfilters $m = 0, 1$ and $m = 2, 3$, thus yielding the final adjusted maximum spread of 8, as shown in Table I.

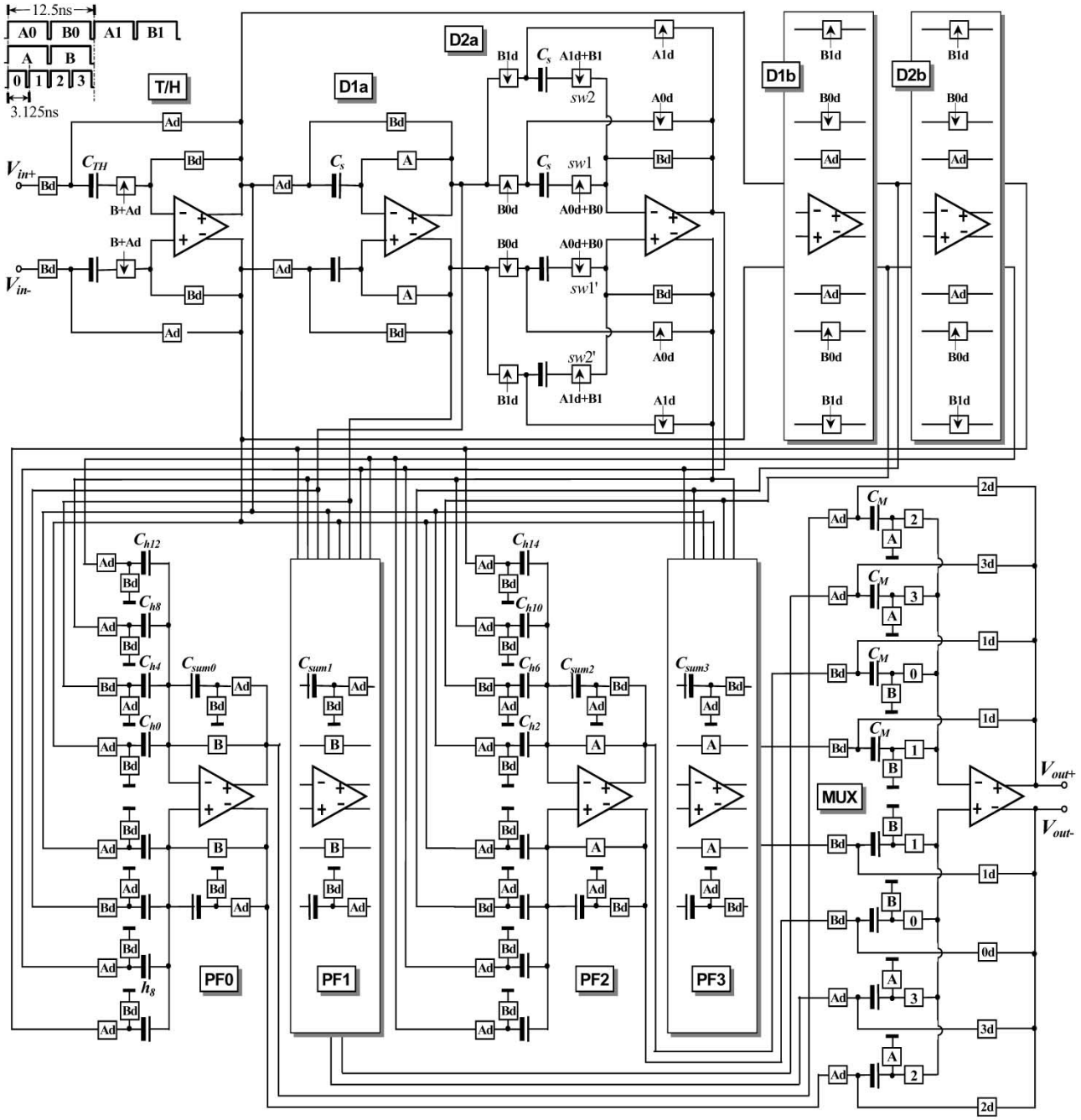

Fig. 4. Simplified SC filter schematic and clock phases.

A specific normalization scheme avoids the need for nonunit capacitance values in the feedback/summing capacitors, leading to better ratio matching.

B. High-Speed Output SC Multiplexer

The filter generates 320 MS/s interpolated outputs through the operation of an high-speed MUX that switches among the four polyphase subfilter outputs in a counterclockwise manner at 320 MHz, which imposes a settling time for the MUX opamp of 2.2 ns only after counting the nonoverlapping phase gap and the rising and falling time. Since the dc-offset of the MUX will impose mainly (in the overall response of the filter) a dc level shifting instead of pattern noise tones, the corresponding circuit shown in Fig. 4 is hence optimized without autozeroing for full output sampling period operation at maximum speed, thus minimizing the power consumption and improving linearity as well. The process of rotating-switching (that is also here charge-transfer free) boosts the operating speed to the maximum through the enlargement of the feedback factor and it also reduces further the parallel path gain and bandwidth mismatches together with the adoption of a double-sampled SC common-mode feedback (CMFB). In this case, the sampling/holding capacitor is chosen at 0.7 pF to yield an efficient tradeoff among noise, speed, and gain errors. Moreover, the process of charge-transfer free, mentioned before, reduces the output glitch effects which usually happen in SC circuits that employ high-output-impedance transconductance opamps.

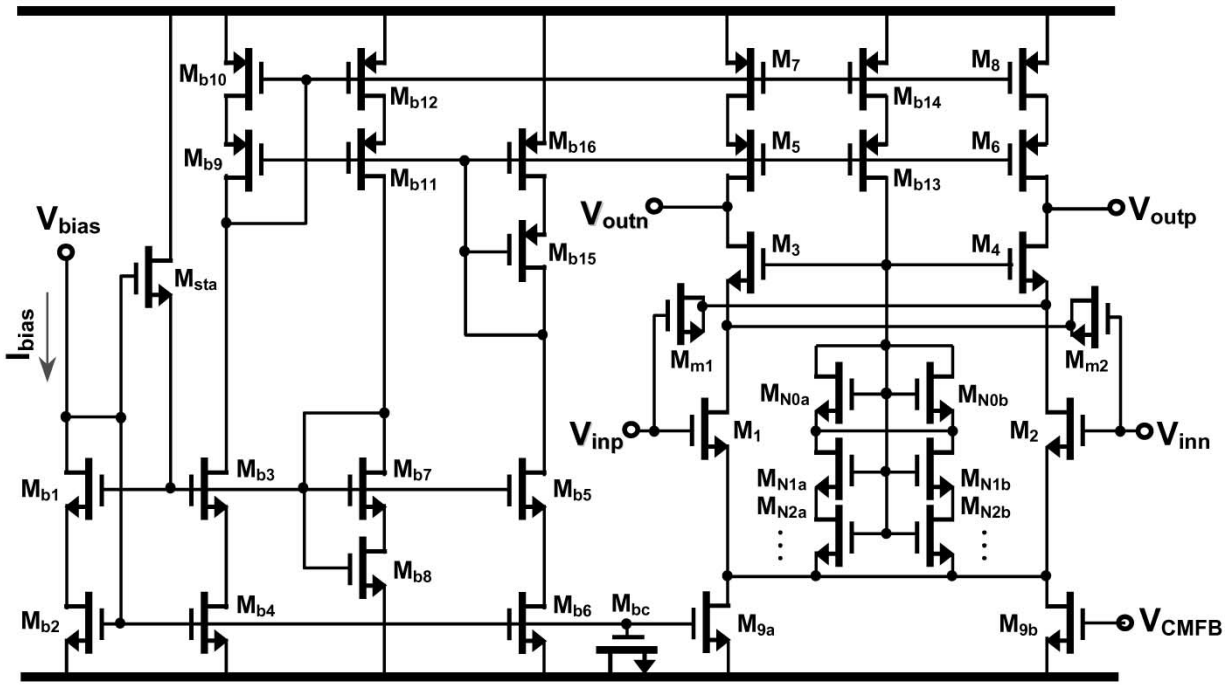

Fig. 5. Opamp schematic.

TABLE I
NORMALIZED CAPACITANCE VALUE (fF) FOR FIR TAP WEIGHT

PF0 (m=0)		PF1 (m=1)		PF2 (m=2)		PF3 (m=3)	
C_{h0}	192.2	C_{h1}	440.2	C_{h2}	242	$-C_{h3}$	171.1
$-C_{h4}$	442	$-C_{h5}$	155.7	C_{h6}	487.2	C_{h7}	911.3
C_{h8}	487.2	$-C_{h9}$	155.7	$-C_{h10}$	442	$-C_{h11}$	171.1
C_{h12}	242	C_{h13}	440.2	C_{h14}	192.2		
C_{sum0}	767.7	C_{sum1}	911.3	C_{sum2}	767.7	C_{sum3}	911.3
C_{unit0}	96	C_{unit1}	152	C_{unit2}	96	C_{unit3}	152

C. Opamps and Switches

The settling time of the opamps in the low-speed filter core is required to be less than 9.5 ns, while that in the high-speed MUX is lowered to 2.2 ns; on the other hand, in both cases the gains can be moderate, ranging from 1000 to 1500 without affecting the main circuit behavior. Hence, the single-stage telescopic-cascode opamp is used here due to its superior high-speed, low-power, and low-noise capability. To achieve the required output swing, with equal I/O common-mode levels at 0.95 V for 2.5-V supply, which is stabilized by dynamic SC CMFB and necessary due to the autozeroed reset nature, proper wide-swing and internal-cascode biasing circuitry is employed, as shown in the opamp schematic of Fig. 5. The nMOS capacitor ($M_{\rm bc}$) at the biasing line of the tail current source is only inserted at unused layout space for better common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR). Monte Carlo simulations performed with respect to process variations show that the fastest opamp achieves the following mean values: 67-dB dc gain ($\sigma = 1.3$ dB), 1.05-GHz unity-gain frequency ($\sigma = 57$ MHz) and 63° of phase margin ($\sigma = 0.9°$) with 2.5-pF loading. Also, the settling time is close to 1.6 ns with a 0.5-V voltage step, and the slew rate is 1.7 V/ns, leading to 12 mW of power dissipation.

The assignment of low common-mode level in the designed opamps is also imposed by the use of only nMOS switches to minimize routing and synchronization difficulty of the clock distribution in the overall circuit, which are mainly due to the multirate/multiphase arrangement, as well as the digital noise coupling from operation at high frequency. The sizes of the switches, ranging from 5 μm/0.3 μm to 53 μm/0.3 μm, are dimensioned distinctively according to their different capacitive loads.

D. Noise Allocations

Since the interpolating filter presents a bandpass response and its architecture uses the autozeroing technique, the flicker noise of the devices is negligible, which results in the thermal noise from switches and opamps being the dominant noise source in the circuit. Then, the total output noise of the differential SC ADB and polyphase subfilters can be approximated by [18]

$$\overline{v_{no,ADB}^2} = \frac{2kT}{C_s} + \left(\frac{2kTR_sC_s}{C_s + C_{PI\_d}}\right)\omega_{ugb\_d} + \frac{4}{3}\frac{kT}{g_{m1\_d}}\gamma_d\left(\frac{C_s + C_{PI\_d}}{C_s}\right)\omega_{ugb\_d} \quad (3)$$

and

$$\overline{v_{no,PF}^2} = \frac{2kT}{C_F}\left(1+\frac{\sum_{i=1}^{n} C_{hi}}{C_F}\right) + \left(\frac{2kT\sum_{i=1}^{n} R_i C_{hi}^2}{C_F(C_F+\sum_{i=1}^{n} C_{hi}+C_{PI\_PF})} + \frac{2kTR_FC_F}{C_F+\sum_{i=1}^{n} C_{hi}+C_{PI\_PF}}\right)\omega_{ugb\_PF} + \frac{4}{3}\frac{kT}{g_{m1\_PF}}\gamma_{PF}\left(\frac{C_F+\sum_{i=1}^{n} C_{hi}+C_{PI\_PF}}{C_F}\right)\omega_{ugb\_PF} \quad (4)$$

where C_s is the sampling/holding capacitor of each SC ADB, C_{hi} is the capacitor associated with the ith coefficient branch and C_F ($= C_{sumi}$ for simplicity) is the feedback/summing capacitor for subfilter, and R_s, R_i, and R_F are the corresponding total on-resistances of the switches, either in the summing or in the output phases. C_{PI} is the parasitic capacitance in the opamp input node, ω_{ugb} is the unity-gain bandwidth frequency, and g_{m1} is its transconductance, whereas γ represents the excess noise factor, which is as low as $\gamma = 1 + g_{m7}/g_{m1}$ in a telescopic opamp. In the case of the MUX, the noise contribution can be similarly calculated by (3).

From (3) and (4), the total output noise contains, first, the well-known sampling *kT/C* noise (first term), and second, the direct coupled noises generated during the output phase, with contributions from the switch on-resistance (second term) and the opamp input-referred thermal noise (third term), that are both band-limited by the opamp's bandwidth. The contribution of the second term here cannot be neglected due to the relatively large on-resistance (size limitation of switches) in such a high-frequency operation.

Thus, the total input-referred noise, within the lower input Nyquist band, can be estimated as

$$\overline{v_{IRN}^2} = B\cdot\overline{v_{no,ADB}^2} + \frac{\overline{v_{no,PF}^2}}{\left(\frac{\sum_{i=1}^{n} C_{hi}}{C_F}\right)^2} + \frac{\overline{v_{no,MUX}^2}}{\left(\frac{\sum_{i=1}^{n} C_{hi}}{C_F}\right)^2} \quad (5)$$

where B is the number of SC ADBs. Finally, the resulting total output noise within the output higher Nyquist band can be obtained by

$$\overline{v_{ORN}^2} = L\cdot\overline{v_{IRN}^2}\cdot ENBW \quad (6)$$

where $ENBW$ is the equivalent noise bandwidth of the overall filter. To achieve a value of SNR higher than 60 dB, the total output noise must be lower than 350 $\mu\mathrm{V_{rms}}$. The final values of noise allocations in the SC ADBs, polyphase subfilters, and output MUX are presented in Table II, together with the corresponding total noise obtained with the above formulas which also include the parameters extracted from simulations.

TABLE II
NOISE ALLOCATIONS ($f_{\mathrm{sop}} = 320$ MHz)

ADB	PF	MUX	Total
53.8 nV_{rms}^2	10.3 nV_{rms}^2	9.1 nV_{rms}^2	73 nV_{rms}^2 (271 μV_{rms})

E. I/O Circuitry

To emulate the actual S/H signals generated from the DDFS logic and DAC, a T/H SC stage with wide input signal bandwidth is designed with autozeroing and charge-transfer-free properties, to operate at the lower sampling rate of 80 MHz for testing purposes, as shown also in Fig. 4. The additional switches between the sampling capacitor and the opamp input were especially designed to eliminate undesired glitches imposed by the direct capacitive coupling from the input. An output driver including a level-shifter followed by a low-output impedance buffer is also used next to the output PAD to drive 50-Ω loads from the measurement equipment in high-frequency testing. For an accurate evaluation of the S/H characteristic of the output signals at 320 MS/s, this driver is designed to achieve a -3-dB bandwidth larger than 1 GHz and a total harmonic distortion (THD) lower than -65 dB.

F. Low Timing-Skew Multirate Clock Generator

The complexity of the multirate clock generator associated with the filter is quite high, comprising a total of 21 phases, originated from a single master clock, where eight rotate at 320 MHz and 13 at 80 MHz. To reduce the signal-dependent clock-feedthrough and charge-injection errors, the clock-delayed (bottom-plate sampling) technique has been used.

An important aspect that must be carefully considered in the design is the fixed systematic timing skew among time-interleaved phases imposed not only from substantial delay mismatches in the standard frequency divider, nonoverlapping clock generation circuit, and gate propagation delays, but also from unbalanced digital power supply noise. Due to the S/H nature of the input in analog interpolation, the timing-skew errors are negligible in the input sampling process, while instead they appear at the output S/H signals from the high-speed MUX. Thus, this timing-skew effect can be classified as a specific sampling mechanism defined as input-uniformly sampling with output-nonuniformly holding, or IU-ON(SH) [19], [20]. The spectrum expression of the signal with such practical nonuniformly holding effect can be derived as presented in [19], and on the other hand, the final SNR (power ratio between the signal and the modulated imaging sidebands) can be obtained with $2\pi f_{\mathrm{o}}\sigma_{rm}T \ll 1$ as [20]

$$\mathrm{SNR} = 20\log_{10}\left(\frac{1}{2\pi a\sigma_{rm}}\right) - 10\log_{10}\left(1-\frac{1}{M}\right) \quad (7)$$

where $a = f_{\mathrm{o}}/f_{\mathrm{samp}}$ is the normalized frequency of the sinusoid, σ_{rm} is the standard deviation of the timing skew (with pe-

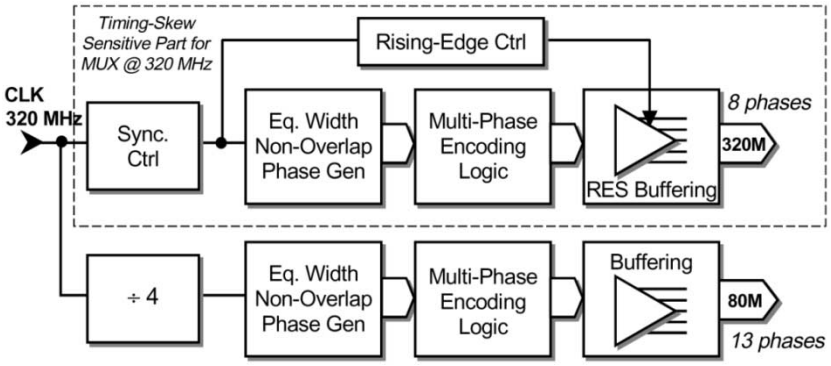

Fig. 6. Simplified structure for low timing-skew multirate clock generator.

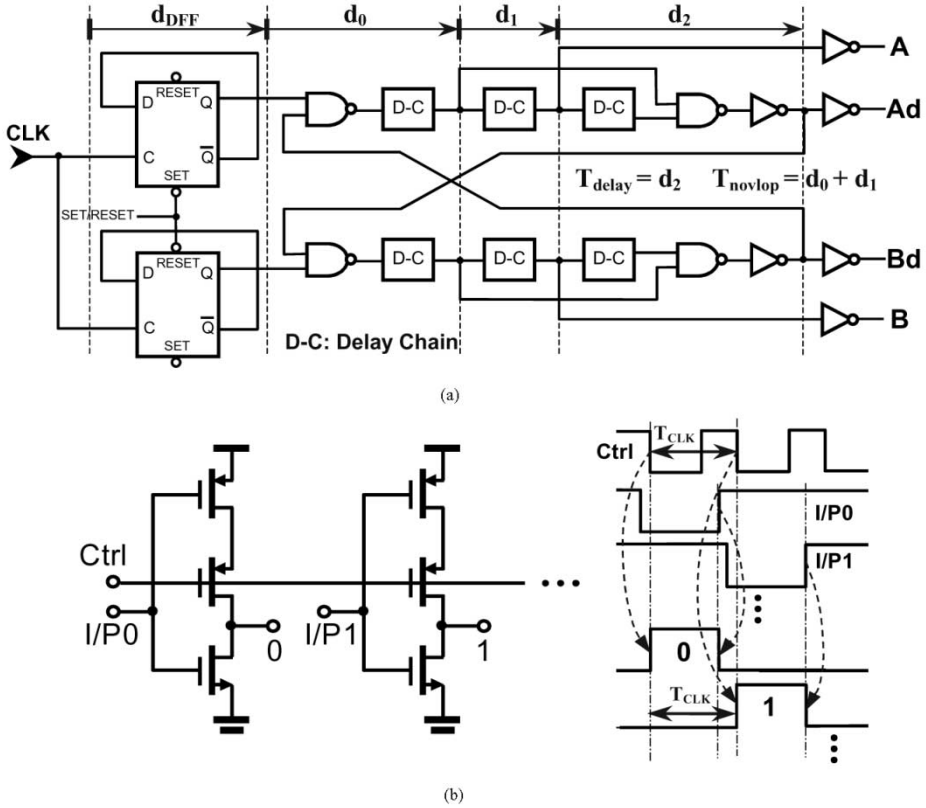

Fig. 7. (a) Equal-width nonoverlapping clock generation. (b) Rising-edge synchronization buffer array.

riod M) normalized to the sampling period (T). From this expression, we conclude also that the pure random clock jitter corresponds only to the first term, which is obtained when $M \rightarrow \infty$. Equation (7) proves also interestingly that the SNR for an IU-ON(SH) process is identical to the one obtained from digital spectra of traditional nonuniformly impulse sampling [21]. Hence, to achieve an SNR $>$ 60 dB the standard deviation of the timing skew must be well controlled within 5 ps. Such stringent requirements for the clock generation, which is structurally presented in Fig. 6, are especially achieved based on the following design controls.

1) *Systematic Mismatches Control—Equal Propagation Gate Delay:* The accumulated propagation gate delays for all interleaved phases are balanced by a careful logic design, e.g., all of them are triggered by the same edge of reference. This means that the nonoverlapping phase generator, shown in Fig. 7(a), provides ideally an equal width for A and B with a fixed timing delay of one master clock cycle. The layout parasitic effects are also considered in the design.
2) *Random Process Mismatches Control—Rising-Edge Synchronization:* To minimize the random process mismatches imposed by the logic gates in the skew-insensitive time-interleaved phase generation path, a specific rising-edge synchronization buffer array is also designed, as shown in Fig. 7(b) where the rising edges of phases 0 and 1 are only present at the falling edge of the same control clock, while their falling edges are independent of the control signal. This buffer array is located just before the last buffer that drive the clock

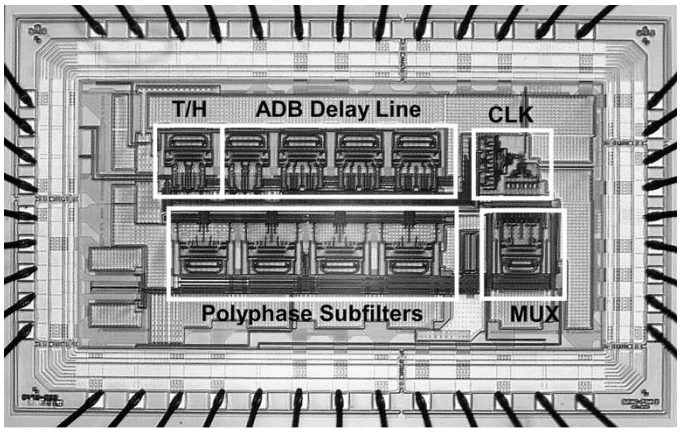

Fig. 8. Die microphotograph.

buses in the generation of eight output high-speed MUX phases, which implies that the random mismatch will ideally happen only in the last and largest buffer, meaning that it can indeed be neglected.

3) *dI/dt Supply Noise Mismatch Control—Separation of Digital $V_{\rm DD}$ Supplies:* The power supply design has included an arrangement of two-individual $V_{\rm DD}$ supplies with a shared common-ground and their correspondent on-chip decoupling for the low-speed (filter core) and the high-speed (MUX) clock generation. This is necessary to minimize the timing-skew errors that are enforced by the mismatches in the supply voltage variation (caused by dI/dt noise). Low-speed clock phases generate periodically dI/dt noise at a maximum value that is eight times greater than the output sampling period, which results in mismatches among the rising edges of the interleaved phases or equivalently periodic fixed timing skew. From the simulated results, such skew can be reduced, with the aforementioned technique, from a value higher than 100 ps in the worst case (that will completely degrade the system response) to a value close to a few picoseconds only.

G. Layout

The filter was integrated in 0.35-μm double-poly triple-metal CMOS technology and the chip microphotograph, with an active core area of 2 mm^2, is shown in Fig. 8. The design uses separated $V_{\rm DD}$ supply pins but shared common ground with on-chip decoupling for analog and digital parts to minimize the inductivity in the current return path for signal transfer, which usually leads to the highest current spikes in SC filters (the adoption of such technique allows up to 50% noise reduction as confirmed by simulation). Also, a strict symmetry and matching in sensitive circuit parts has been maintained together with a clean signal and substrate environment achieved by ample substrate contacts, as well as multidimensional shielding with minimized return current path impedance. Wide-sheet power supply lines are used to minimize the voltage drops across them and MOSFET capacitances fill the unused space to obtain a significant decoupling capacitance (larger than 200 pF) from the supplies to the ground, so that the peak power-supply noise can be controlled in the worst case simulation within a value of 200 mV.

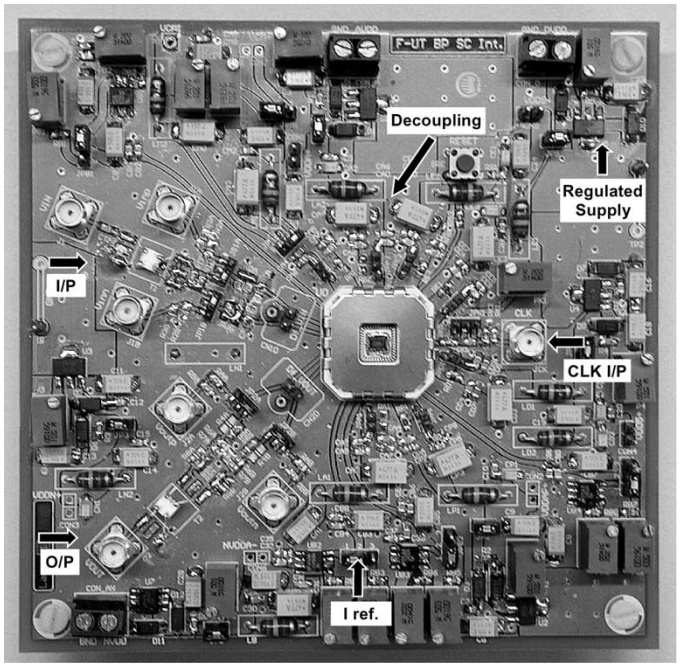

Fig. 9. Top view of four-layer testing board.

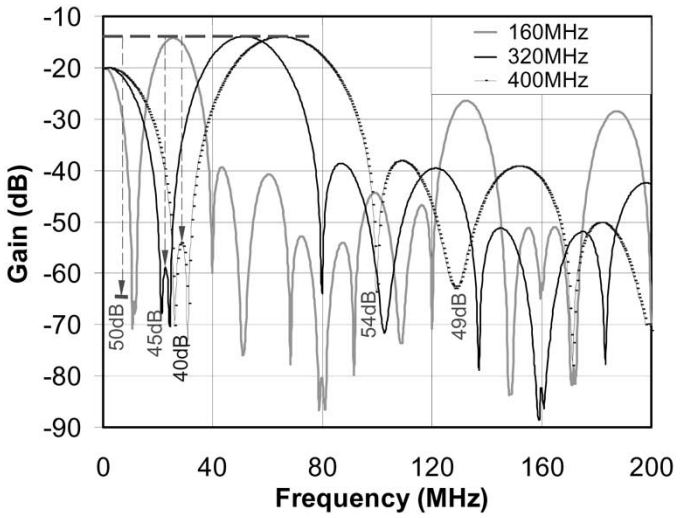

Fig. 10. Measured amplitude responses for different output sampling rates.

V. Experimental Results

Testing of the ten prototype chip samples, mounted in a ceramic quad flat pack (CQFP), was carried out at room temperature on a four-layer low EMC PCB (carefully designed) presented in Fig. 9, with 2.5-V supply for 160- and 320-MHz output sampling rates (further measurements were also taken at 400 MHz with 2.5-V analog and 3.3-V digital supplies).

The measured amplitude response in Fig. 10 shows that the minimum stop-band rejection is larger than 50/45/40 dB for 160/320/400 MHz output rates. Fig. 11 presents the ten samples' measured response at 320-MHz output rate, comparing it with the ideal response and the simulated worst case response. These results show that the prototype measurements meet well the initial specifications. For these ten samples, the passband ripple shows a value that is smaller than 0.6 dB (with 3σ at 0.02 dB)

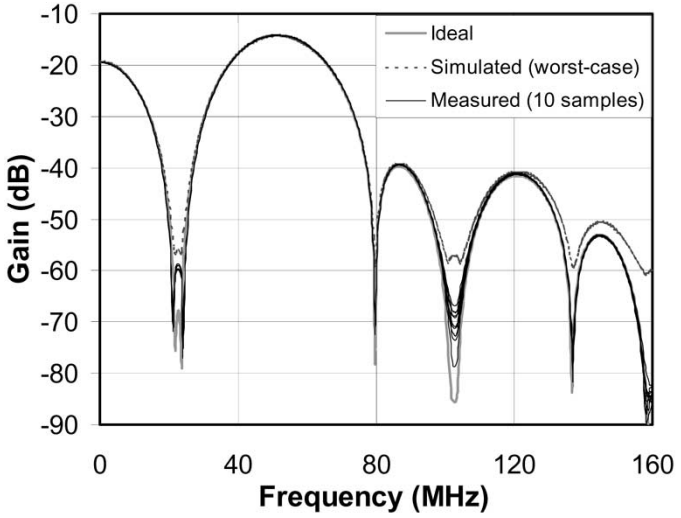

Fig. 11. Measured amplitude response for ten samples with $f_{\rm sop} = 320$ MHz.

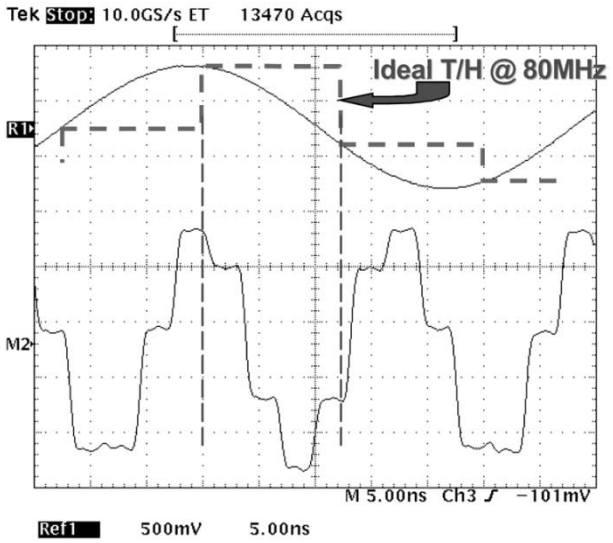

Fig. 12. Measured waveform of 58-MHz signal output with a 1-$V_{\rm p-p}$ 22-MHz input ($f_{\rm sop} = 320$ MHz).

and the variation in the stop-band attenuation complies with 3σ at only 0.45 dB, in the 22–24-MHz band.

To demonstrate the correct frequency up-translation process of the bandpass interpolating filter, the circuit waveforms of a 1-$V_{\rm p-p}$ 22-MHz input and the resulting 58-MHz output sampled at 320 MHz are presented in Fig. 12. In practice, the input sinusoidal signal is sampled by the T/H stage before the filter (and this internal node cannot be measured), thus the ideal T/H signal at 80 MHz is illustrated by the dotted line, clearly showing the correct fourfold sampling rate increase process.

Fig. 13 illustrates the measured 58-MHz interpolated output signal spectrum of the filter, where the delta markers 1, 2, and 3 are situated in the folded images of their third harmonics sampled either at 80 or 320 MHz, which are all less than -66 dBc, and the observed second harmonic is only as low as -78 dBc (due to the careful layout design), thus leading to a THD of -62 dB. The highest pattern noise at 80 MHz is close to -70 dBc, and the total pattern noise, measured within the Nyquist band with zero input, is only about 120 $\mu V_{\rm rms}$. The

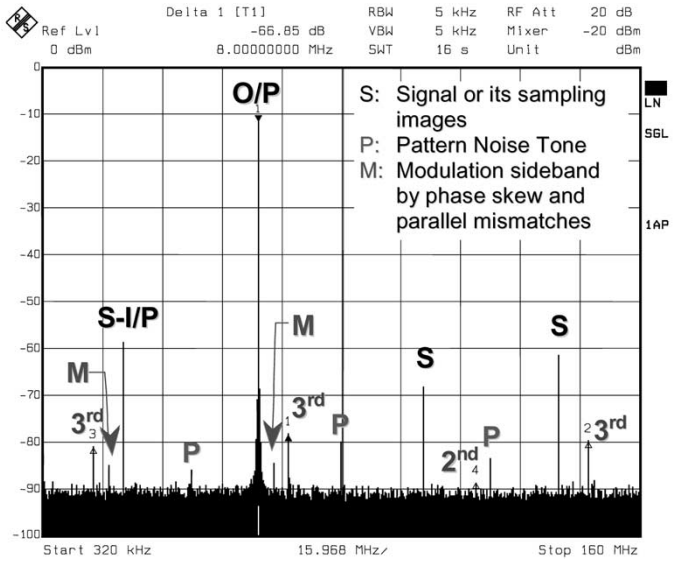

Fig. 13. Measured spectrum of 58 MHz signal output with a 1-$V_{\rm p-p}$ 22-MHz input ($f_{\rm sop} = 320$ MHz).

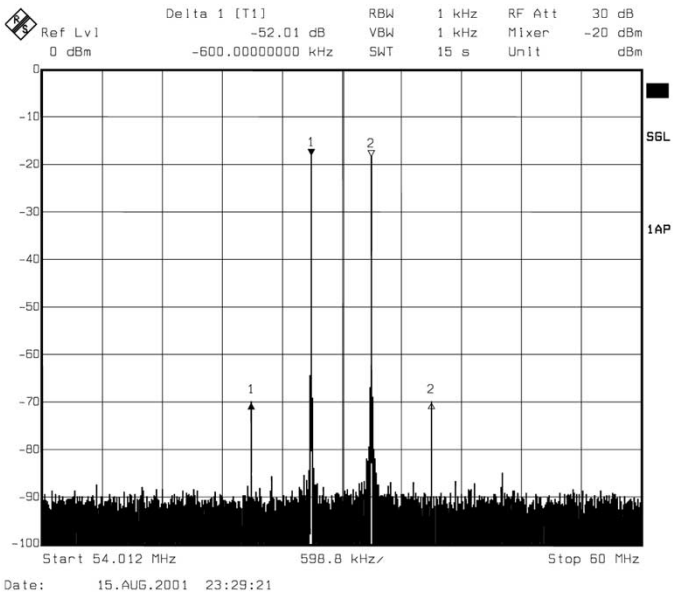

Fig. 14. Measured IM3 for two 0.5 $V_{\rm p-p}$ tones with 600 KHz separation ($f_{\rm sop} = 320$ MHz).

modulation sidebands at 18, 62, and 98 MHz originated by the phase timing skew and parallel gain mismatches are very well controlled, all being below -72 dBc.

Fig. 14 shows the measured in-band spectrum of outputs at 56.7 MHz and 57.3 MHz with the two respective input tones of 0.5 $V_{\rm p-p}$ at 22.7 MHz and 23.3 MHz, with a 320-MHz sampling rate resulting in a third-order inter-modulation distortion (IM3) of -52 dB.

Fig. 15 reports the IM3 and THD performance versus different input signal levels for three distinct output rates. For $f_s = 320$ MHz, 1% THD corresponds to one input at 2.1 $V_{\rm p-p}$ and 1% IM3 to two inputs at 0.85 $V_{\rm p-p}$. According to the measured output noise spectrum density shown in Fig. 16 with zero input (including the T/H and output driver that only contribute for additional degradation of the overall performance),

TABLE III
PERFORMANCE SUMMARY OF THE PROTOTYPE SC BANDPASS INTERPOLATING FILTER

Technology	0.35 μm CMOS		
Filter order	15-tap FIR Bandpass		
Output Sampling Rate	**400 MHz**	**320 MHz**	**160 MHz**
Input Sampling Rate	100 MHz	80 MHz	40 MHz
Passband f_{oL}- f_{oH}	70-72.5 MHz	56-58 MHz	28-29 MHz
Stopband Rejection	> 40 dB	> 45dB	> 50 dB
THD (1$V_{p\text{-}p}$ Output @ f_{oH})	-57 dB	-62 dB	-64 dB
IM3	-53 dB	-52 dB	-62 dB
Fixed-Pattern Noise Tones	< -65 dBc	< -70 dBc	< -70 dBc
Mismatch-Modulated Tones	<-70 dBc	<-72 dBc	<-77 dBc
Total Output Noise	265 μV_{rms}	280 μV_{rms}	262 μV_{rms}
Total Pattern Noise	240 μV_{rms}	120 μV_{rms}	120 μV_{rms}
SNDR (1$V_{p\text{-}p}$ Output @ f_{oH})	56 dB	61 dB	63 dB
Dynamic Range (1% THD)	68 dB	68.5 dB	69.4 dB
Dynamic Range (1% IM3)	62 dB	61 dB	64 dB
OIP3	22.5 dBm	23 dBm	26.4 dBm
CMRR (Output @ f_{oH})	53 dB	54.5 dB	56 dB
PSRR (Output @ f_{oH})	38 dB	32 dB	40 dB
Supply	2.5 V, 3.3 V(Dig.)	2.5 V	2.5 V
Analog Power	120 mW	120 mW	59 mW
Analog Power-per-zero	8.6 mW	8.6 mW	4.2 mW
Digital Power	37 mW	15.8 mW	7.8 mW
Total Power	157 mW	136 mW	67 mW
Active Core Area	2 mm^2 (BPF+T/H+CLK, 0.1 mm^2 for CLK)		

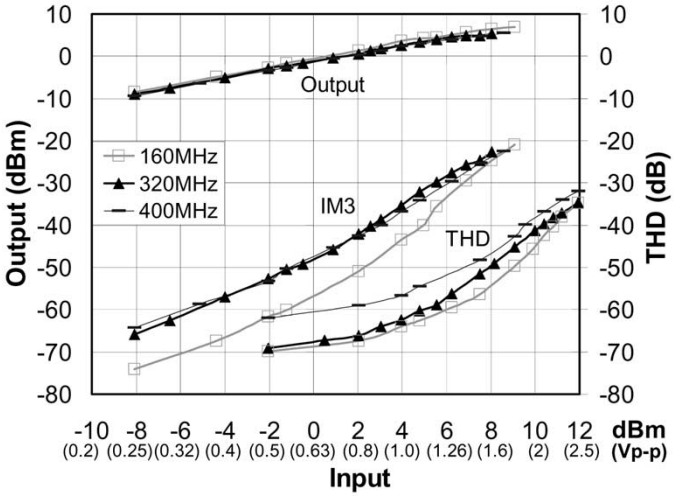

Fig. 15. Measured THD and IM3 versus input signal level for different output sampling rates.

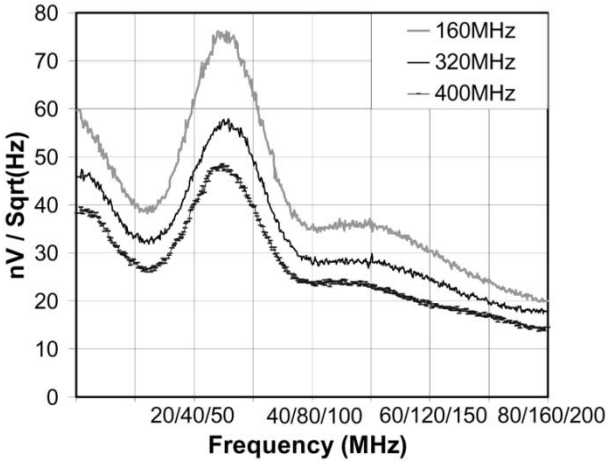

Fig. 16. Measured output noise spectrum density for different output sampling rates.

the total output noise within the Nyquist band is 280 μV_{rms} for the 320-MHz output sampling rate, thus resulting in a dynamic range of 68.5 dB for 1% THD and 61 dB for 1% IM3.

VI. CONCLUSION

This paper has presented the design and implementation of a very high-frequency multirate SC bandpass filter embedding, simultaneously, sampling rate increase and frequency up-translation in a monolithic 0.35-μm CMOS with 2.5-V supply. This filter successfully realized a 15-tap FIR system function, 57-MHz bandpass operation, and up-translation in the frequency of 2-MHz bandwidth signals, together with fourfold sampling rate increase to 320 MS/s at the output (with extended operation up to 400 MS/s) for DDFS systems. Novel system-level topologies and new design techniques adequate to this application have also been presented, e.g., a multi-notch FIR function, an improved multirate polyphase interpolation structure, as well as detailed high-speed SC circuit-level implementations, which are custom-designed taking into consideration most of the usual IC nonidealities

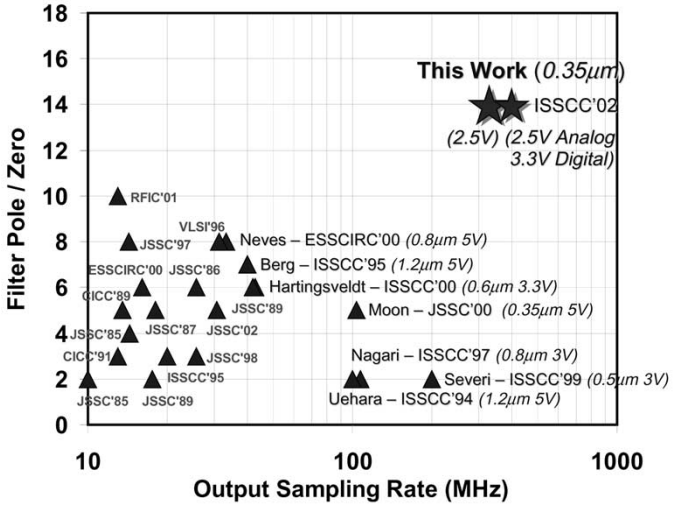

Fig. 17. Brief comparison of the state-of-the-art CMOS SC filters.

(speed, offset, noise, timing skew, and parallel mismatches). The filter performance, measured at different output sampling rates (the nominal 320 MHz, 160 MHz, and also 400 MHz), is summarized in Table III. The results, which are also presented in Fig. 17 with comparison to previously reported CMOS SC filters [1]–[7], show that the current design achieves the highest performance with higher output sampling rate, filter order, linearity, and dynamic range, while requiring the lowest supply voltage [18].

ACKNOWLEDGMENT

The authors would like to thank Chipidea Microelectronics, S.A., for the technical support, and the reviewers for their useful comments and suggestions.

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