Experimental results: A prototype oscillator was fabricated in the AMS 0.8 μm CMOS process. It used an active area of 0.20 mm^2. The frequency was tunable between 48 and 132 MHz, by adjusting bias current I_A. The current amplitude was adjusted to be $I_{ref}=I_A/5$. This way signal excursions remain always within the same portion of the nonlinear transfer curve of the OTAs. The resulting voltage amplitude at nodes V_1 and V_2 changed between 27 and 81 mV. Fig. 3*a* shows the measured dependence between oscillation frequency and bias current I_A. The measured phase shift error between voltages V_1 and V_2 (phase(V_1)-phase(V_2)-90°) is shown (with stars) in one of the traces in Fig. 3*b*. As can be seen, there was an error of less than 2° over the complete frequency tuning range. Also shown (with circles) in Fig. 3*b* is the phase noise present at voltage V_1 (or V_2), expressed in degrees. This phase noise was computed as follows. The node voltage was recorded with 0.2 ns sampling rate over a large number of periods. Zero crossings were computed and their standard deviation calculated. This standard deviation is what is shown in the second trace of Fig. 3*b*.

Conclusions: An OTA-C topology for implementing a quadrature oscillator in the range 50–130 MHz has been presented. The topology exploits symmetry to produce the two phases at 90° phase shift. The circuit also produces four extra current signals at phases 0°, 90°, 180°, 270° which are used in a high-speed current-mode MAX circuit to extract a quasi-instantaneous envelope of the oscillations, in the current domain. This envelope is used in a properly stabilised amplitude control loop to set the oscillating amplitude at 1/5 of the current excursion range of the main OTAs, to minimise distortion. The influence of transconductance phase shift of the OTAs is considered. A complete oscillator prototype has been fabricated and tested in the AMS 0.8 μm CMOS process. The quadrature oscillator shows a phase shift between its two output signals between 89.5° and 91.7° in the frequency range from 48 to 132 MHz. Phase noise has also been characterised.

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Two-step channel selection technique by programmable digital-double quadrature sampling for complex low-IF receivers

Pui-In Mak, Seng-Pan U and R.P. Martins

Presented is a novel two-step channel selection technique to be adopted in complex low-IF receivers for enhancing the performance and efficiency of the front-end PLL-frequency synthesiser (PLL-FS), which will be mainly implemented by a proposed programmable digital-double quadrature sampling (D-DQS) scheme. Thus, the weaknesses of the PLL-FS in very small step-size operations including long locking time and large phase noise are significantly reduced. Simulation results of the D-DQS scheme are provided to demonstrated the feasibility of such a technique.

Introduction: In complex low-IF receivers, the intermediate frequency (IF) can be set to half of the channel bandwidth value to relax the image rejection requirement, as the maximum power of the adjacent channel is much less than the other in-band channels in most wireless communications [1]. However, when an integer PLL-frequency synthesiser (PLL-FS) is employed for channel selection, a small step-size change in the local oscillator (LO) frequency is necessary. Such traditional scenario is shown in Fig. 1*a*, where the capture of the RF channels labelled as **A**, **B**, **C** and **D**, requires a step-size of the LO frequency equal to one channel bandwidth, and the total mandatory moving steps equal to the number of channels in the entire frequency band. The resulting major drawbacks are, the longer locking time and larger phase noise values, due to insufficient bandwidth for the loop filter and large division ratio of the frequency divider in the PLL-FS [2].

In this Letter, we propose a two-step channel selection technique that alleviates the problems mentioned above through the partition of channel selection from the front-end PLL-FS to the back-end programmable digital-double quadrature sampling (D-DQS) scheme [3]. Such new channel selection technique and simulation results of the D-DQS scheme are introduced in the following Sections.

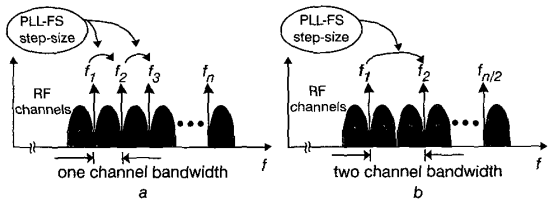

Fig. 1 *Channel selection by PLL-FS*
a Traditional method
b New proposed method

Proposed two-step channel selection technique:
Step 1: Dual-channel selection by PLL-FS: The first step of this new channel selection scheme is still performed by the PLL-FS in the front-end as shown in Fig. 1*b*, however the main difference relies on the fact that the PLL-FS only down-converts a pair of effective channels on the IF by selecting the LO frequency located between every two RF channels, e.g. channels **A** with **B** or channels **C** with **D** (the final selection between such pair of channels will be performed by the programmable D-DQS scheme in the second step). Based on this method, the block diagram of the new proposed receiver topology in shown in Fig. 2. The advantages of this topology are: (i) a higher frequency reference clock can be employed for the PLL-FS loop filter to significantly reduce the problems originated by small step-size operation, since the minimum step-size of the PLL-FS is now extended from one to two channels bandwidth; (ii) as the locking position of the LO is selected in between every two channels, the resulting moving steps of the LO frequency can be halved, which also simplifies the required division ratio of the frequency divider in the PLL-FS, thus allowing the reduction of phase noise; (iii) since the dual-channel is down-converted to a frequency range near to the baseband, the original required bandpass channel selection filters can be replaced by their lowpass counterparts. This illustrates the fact that such frequency down-conversion method can improve the PLL-FS performance and simultaneously simplify the whole receiver architecture without involving any extra-circuitry in the PLL-FS.

Step 2: Decision channel selection by programmable D-DQS: The D-DQS scheme is generally employed in the receiver back-end of the complex low-IF receiver for IF-to-baseband frequency down-conversion. Here, the programmability of D-DQS is explored in order to perform channel selection function between two adjacent channels only through a simple control. Following the channel selection from step 1, the operation of this programmable D-DQS is explained as follows: supposing that the PLL-FS has down-converted a pair of channels labelled **A** and **B** at the frequency bins $-f_{IF}$ and $+f_{IF}$ as shown in Fig. 3, (I), respectively, then the following steps will involve sampling and digitisation at the sampling frequency $f_s=4f_{IF}$. This value of f_s efficiently simplifies the following D-DQS because the multiplying values are only $\{-1, 0, 1\}$. Thus, no extra I/Q mismatch

exists and only a simple digital circuit plus a lookup table will be required.

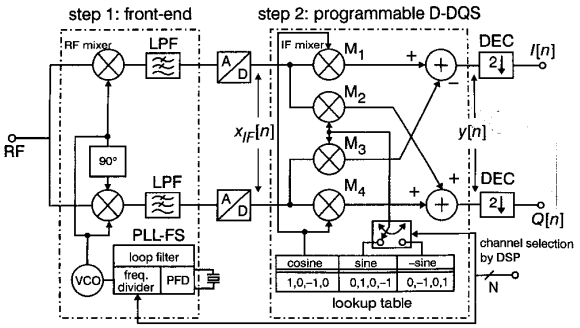

Fig. 2 *New proposed complex low-IF receiver topology*

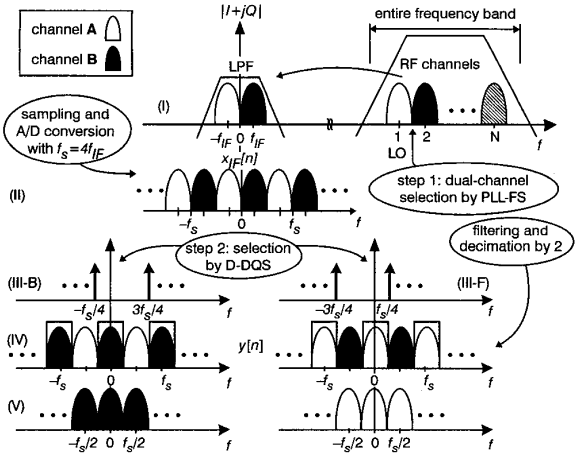

Fig. 3 *Spectra flows of proposed channel selection method*
III-F: forward-shifting; III-B: backward-shifting

After A/D conversion, as shown in Fig. 3, (I), the dual-channel at the IF with also the low-frequency noise $\varepsilon_{LF}[n]$ that generated from the RF-to-LO crosstalk is given by:

$$x_{IF}[n] = x_A[n]e^{-j(2\pi f_{IF}/f_s)n} + x_B[n]e^{j(2\pi f_{IF}/f_s)n} + \varepsilon_{LF}[n] \quad (1)$$

Switching the multiplying sequences in digital mixers $\mathbf{M_2}$ and $\mathbf{M_3}$ between $\sin[n\pi/2] = 0, 1, 0, -1$ and $-\sin[n\pi/2] = 0, -1, 0, 1$ for $n = 0, 1, 2, 3, \ldots$, is equivalent to multiplying complex exponential sequence $e^{jn\pi/2}$ or $e^{-jn\pi/2}$ to the input, thus programming the forward or backward frequency-shifting of $x_{IF}[n]$ for the acquisition of channel **A** or **B**, as shown in Fig. 3, (III-F) and Fig. 3, (III-B), respectively. For instance, in forward frequency-shifting, the resulting output will be

$$y[n] = x_A[n] + x_B[n]e^{jn\pi} + \varepsilon_{LF}[n] \cdot e^{jn\pi/2} \quad (2)$$

Therefore, channel **A** is now shifted to the baseband and low frequency noise together with channel **B** will be shifted to $f_s/4$ and $f_s/2$, respectively. The resulting output $y[n]$ after the D-DQS is then filtered by a digital decimation filter (DDF) to eliminate all the adjacent channels and low frequency noise as shown in Fig. 3, (IV). Finally, the I and Q data of $x_A[n]$ or $x_B[n]$ at a rate of $f_s/2$ can be obtained for demodulation as shown in Fig. 3, (V). This demonstrates that by applying the simple programmability to the D-DQS, the channel selection can be performed efficiently with also the simplified PLL-FS operation, which will only need to down-convert a pair of channels in the front-end (step I).

Simulation results: Simulation verification was conducted in the SIMULINK™. The simulation model included two 8-bit Nyquist rate A/D converters and a programmable D-DQS scheme. As shown in Fig. 4*a*, three test tones: channel **A** (located at $-f_{IF}$), channel **B** (at $+f_{IF}$) and zero-frequency component (or DC), are applied to the inputs. Such zero-frequency component is applied to test the low frequency noise or DC-offset sensitivity. Assuming that channel **A** is the desired one, the programmable D-DQS will be required to perform forward shifting in the DSP. The output power spectrum density (PSD) is shown in Fig. 4*b*, with the desired channel **A** obtained in the baseband while the zero-frequency component and channel **B** are shifted to $\pm nf_s/4$ and $\pm nf_s/2$, for $n = 1, 3, 5 \ldots$, respectively. A similar result is presented in Fig. 4*c* for backward-shifting.

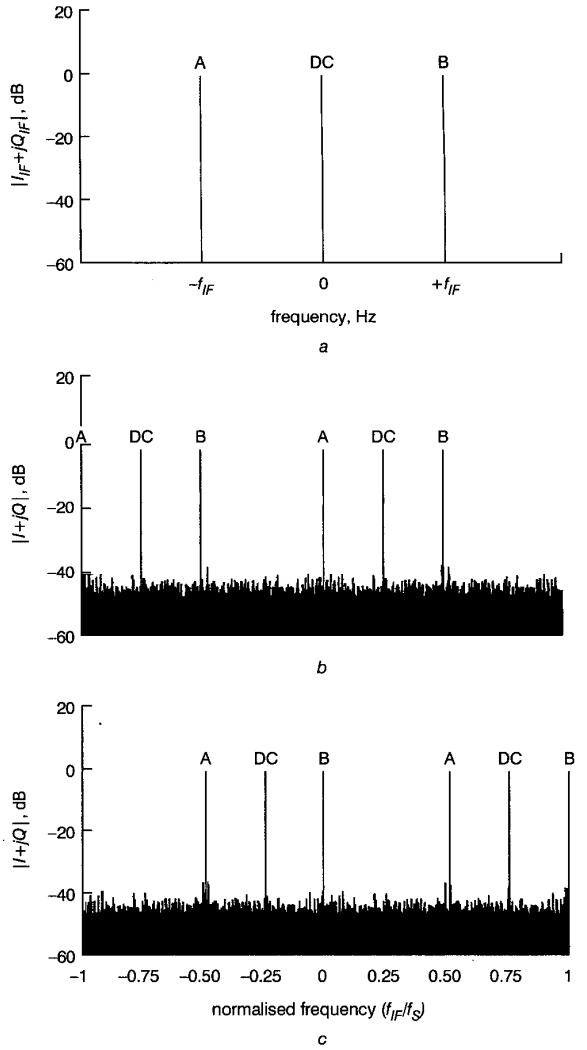

Fig. 4 *Simulated PSD of input, forward-shifted output, backward-shifted output*

a Input
b Forward-shifted output
c Backward-shifted output

Conclusion: A novel programmable D-DQS scheme in cooperation with a relaxed front-end PLL-FS has been presented to perform a two-step channel selection for complex low-IF receivers, without involving any extra I/Q mismatch. This technique, verified by system-level simulations, not only alleviates the problem of the PLL-FS in small step-size operation, but also simplifies the PLL-FS and the receiver architectures.

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Metal-plate 1 × 2 array antenna for 5.2/5.8 GHz WLAN operation

Fu-Ren Hsiao and Kin-Lu Wong

A novel metal-plate 1 × 2 array antenna constructed easily from a single metal plate and suited for WLAN operation in the 5.2/5.8 GHz bands (5150–5350/5725–5875 MHz) is presented. The metal-plate array antenna comprises two radiating elements series-fed by a 50 Ω microstrip line and excited in phase, leading to a high antenna gain level (>4.0 dBi) for frequencies across the 5.2/5.8 GHz WLAN bands.

Introduction: A new kind of antenna constructed by folding a single metal plate has been demonstrated recently [1]. This kind of metal-plate antenna is low cost in construction and is well suited for application as an internal antenna in wireless devices such as laptops, tablet computers, and personal digital assistants (PDAs). By applying this metal-plate construction technique, we present in this Letter a new metal-plate 1 × 2 array antenna, also constructed from a single metal plate and suited for wireless local area network (WLAN) operation in the 5.2/5.8 GHz bands (5150–5350/5725–5875 MHz). The proposed antenna comprises two radiating elements excited in phase, thus providing an enhanced antenna gain level for frequencies across the operating band. This characteristic is very attractive for practical applications, since it is usually required that the antenna gain for frequencies across the 5 GHz band be increased to provide a larger operating range for WLAN operation. This requirement is due to the fact that, given a constant power, the operating range decreases when the operating frequency increases.

Antenna design: Fig. 1*a* shows the proposed metal-plate array antenna, which in this study is easily constructed by folding a 0.3 mm-thick copper plate of dimensions about 20.9 × 65 mm^2 (see Fig. 1*b*). Note that there are four bending lines shown in Fig. 1*b*, and a slot is cut in the copper plate for separating the two radiating elements. The design dimensions shown in Figs. 1*a* and *b* were obtained with the aid of the Ansoft simulation software high frequency structure simulator (HFSS).

The proposed antenna comprises two (an upper and a lower) radiating elements, both series-fed by a 50 Ω microstrip line through the upper and lower feeding strips (size 4.5 × 7 mm^2). Note that the microstrip line has a width of 2.4 mm, mounted on the narrow ground plane of size 5 × 65 mm^2, and uses an air-layer substrate of thickness 0.5 mm. This air-substrate microstrip line has a structure similar to that used in [2], which requires no dielectric substrate and greatly reduces the construction cost of the antenna.

To excite the upper and lower radiating elements in phase, the two elements are oriented to face each other (i.e. the excited currents in the two elements will have opposite directions, suggesting a 180°-phase difference), and the distance between the two elements is set to 27 mm (distance between points A and B shown in Fig. 1), which is close to about a half-wavelength at 5500 MHz, the designed centre frequency. In this case the two radiating elements are excited in phase, thereby leading to a constructive array effect for gain enhancement.

Also note that the two radiating elements are connected to the ground plane through a U-shaped shorting wall and have a same length of 15 mm. Owing to the shorting, the two radiating elements will perform like a planar inverted-F antenna and operate as a quarter-wavelength structure. Thus, by adjusting the length of the two radiating elements (15 mm in this study, corresponding to about 0.25 wavelength at 5500 MHz), the centre operating frequency of the antenna can be controlled. By further adjusting the width (4 mm in this study) and height (5 mm to the ground plane) of the two radiating elements, a wide impedance bandwidth large enough for covering the 5.2/5.8 GHz bands for WLAN operation can be obtained.

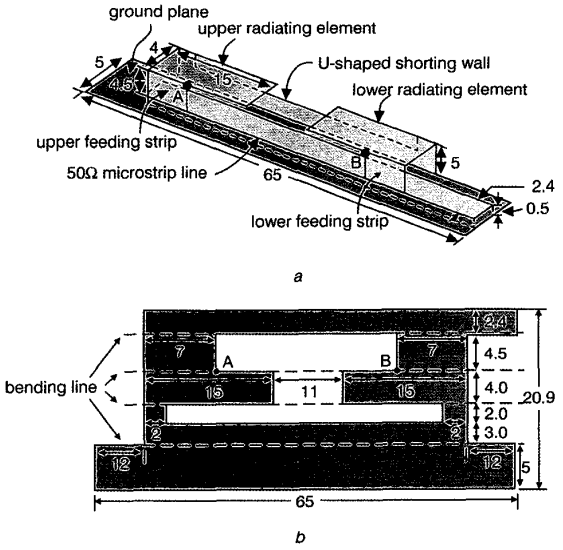

Fig. 1 *Geometry of proposed metal-plate 1 × 2 array antenna for WLAN operation in 5.2/5.8 GHz bands, and proposed antenna unfolded into planar metal plate*

a Proposed metal-plate array antenna
b Unfolded into planar metal plate

Results: Fig. 2 shows the measured and simulated return loss of the constructed prototype. The measured data agree with the simulated results, and a wide resonant mode centred at about 5.5 GHz is excited with good impedance matching. The obtained 10 dB return-loss impedance bandwidth reaches 885 MHz (4995–5880 MHz), covering the required bandwidth for WLAN operations in the 5.2/5.8 GHz bands.

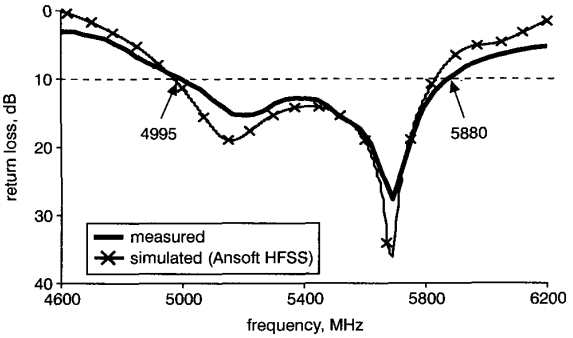

Fig. 2 *Measured and simulated return loss*

Fig. 3 shows the measured radiation patterns at 5500 MHz. Measurements at other operating frequencies across the 5.2/5.8 GHz bands were