A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems

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***Abstract*— A self-body-biasing technique is proposed for differential-drive cross-coupled (DDCC) rectifier, with its profound application in far-field RF energy-harvesting systems. The conventional source-to-body, and the proposed technique known as Lower DC Feeding (LDCF), were fabricated in the 130-nm CMOS and compared at the operation frequency of 500 MHz, 953 MHz and 2 GHz along with a corresponding load of 2 kΩ, 10 kΩ and 50 kΩ. The technique allows the PMOS transistors to operate with a dynamic threshold voltage (V_{th}) which improves the power conversion efficiency (PCE) when the rectifier is operating at a smaller received power. A 9.5% of improvement is achieved at the peak PCE when the rectifier is operating at 953 MHz, and driving a 10 kΩ load. A maximum PCE of 73.9% is measured at 2 GHz when driving a 2-kΩ load. The LDCF technique also offers a self-limiting capability for its output voltage, by reducing the PCE at larger received power. A limit-voltage level of 3.5 V is measured irrespective to the operating frequency and load. This capability aids the protection of the subsequent circuits in a wireless sensor from being overpowered.**

***Index Terms*— Body biasing, passive radio frequency identification (RFID), rectifier, RF-to-dc conversion, RF energy harvesting, wireless power transferring.**

I. Introduction

INTERNET Of Things (IoT) technology has recently gone through a significant evolution as the obsession in this field is in its ability to simultaneously connect and remotely control any physical objects. IoT usually incorporates RFID systems and other identification schemes [1]. Such small systems with wireless communication capability, enable automated object identification in numerous applications such as monitoring environment, tracking objects, contact-less identification and implantable medical devices (IMD) [2]–[4].

Unlike many other mobile devices, a battery is not appropriate for these applications since it requires routine maintenance, subjected to interruption in operation, and its replacement is an inevitable routine which incurs in additional cost. Moreover, integrating a battery consumes additional space which is undesirable for such systems [5].

An energy harvester extracts ambient or environmental energy to provide sufficient power for its applications. The harvesters are able to convert the energy emanating from vibration, sun, heat and other sources [6]–[9] to dc voltages. However, they suffer from a common constraint of being dependent on uncontrolled ambient sources. On the other hand, an RF energy harvesting (RFEH) system overcomes this constraint since radio frequency (RF) signals are the most pervasive ambient energy sources. In such systems, RF power can simply be delivered to the targeted applications when required using intentional radiators based on RF-powered network architecture such as wireless power transferring (WPT) techniques which enable the systems to be battery-less, low cost and maintenance free [10]. WPT techniques can be categorized into three groups which are far-field non-coupling, near-field non-resonant coupling, and near-field resonant coupling. A far-field non-coupling power transferring technique provides a longer communication distance which are mainly used in passive UHF RFID or MMID. However, it suffers from low power conversion efficiency (PCE). It captures incident RF signals and converts it into dc voltage through an antenna and a subsequent rectification device [11].

The dc voltage level at the rectifier output is considerably affected by both the threshold voltage and leakage current of integrated switching devices (diodes or MOS transistors). Several technical contributions and studies have been reported to either mitigate or completely suppress the MOS transistors threshold voltage of the rectifier [12]–[15]. Although the static threshold voltage cancellation technique improves the rectifier performance in forward-bias, the leakage current noticeably increases in reverse-bias resulting in PCE degradation.

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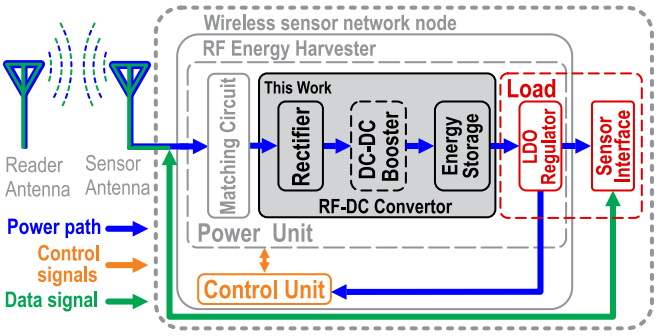


Fig. 1. Block diagram of a typical far-field RF energy harvesting (RFEH) system in a wireless sensor network.

Dynamic threshold voltage techniques have been proposed to improve the rectifier performance for Dickson-based charge-pump [16]. In [17], an additional circuit is used to control the threshold voltage. In [5], two adaptive threshold voltage compensation schemes have been proposed to diminish the leakage current in reverse bias and to reduce the threshold voltage in forward-bias without requiring triple-well transistors.

In [18], a differential-drive cross-coupled (DDCC) rectifier is proposed to reduce the threshold voltage and leakage current simultaneously. The structure has shown a considerable enhanced performance in terms of PCE. To the best of authors' knowledge, the DDCC rectifiers have shown considerable larger PCE when compared with conventional charge pump such as the Dickson topology [19]. Regardless of many reports on improving the rectifier performance, few works have studied the body biasing of MOS transistors integrated in the rectifier [17], [20]–[22] based on the Dickson charge-pump topology. In this work, a novel self-body biasing technique is presented for the DDCC topology without any extra circuits using local nodes, which allows PMOS transistors to have a scalable threshold voltage. Moreover, with this technique the rectifier operates with dynamic PCE which at lower received power implies improved PCE while at larger received power effectively decreases PCE and limits the rectifier output voltage.

This paper is organized as follows: a background review and a brief system operation is presented in Section II. A self-body biasing technique is presented along with detailed description in Section III. In Section IV measurement results and discussion are presented and finally the paper is concluded in Section V.

II. System Description and Threshold Voltage Effect

A typical block diagram of a far-field RFEH system is depicted in Fig. 1. It consists of two main parts which are the power and control unit where the power is generated in the power unit. The power path is depicted in Fig. 1. This unit is responsible to deliver the extracted power to the load and the control unit. The control signals, depicted in Fig. 1, are generated by the control unit to tune the power unit parameters in order to maximize or regulate the output power.

The RF signals emanating from a central hub or reader are collected and converted into signal voltages by an RF antenna. The extracted signal voltages can be modeled as an equivalent voltage source (V_S) and a source resistance (R_S). An impedance matching network is usually required to maximize the available power for the rectifier. The available power can be calculated as $V_S^2/(8R_S)$ when a proper matching network is considered [23].

In RFEH systems, the received power at the antenna is usually weak due to limited allowable power levels regulated by the FCC [24] and the degrading propagation loss [25], [26]. Recalling Friis transmission equation, the available power significantly drops with the increase in the distance between the source and the system. Considering multi-path fading [23], the received power faces even more attenuation.

An RF-to-dc converter, also known as rectifier, converts the received power to a dc voltage. Depending on the structure of the RFEH, the rectifier boosts the converted voltage level if it is adopted as a voltage multiplier. Otherwise, the extracted voltage is enhanced by a separate DC-DC voltage multiplier. For protection purposes, the generated voltage is limited by a voltage limiter. Finally the converted power charges the energy storage (usually a capacitor) which acts as a buffer in the system. The application and the structure of the load system determines whether the load can be directly supplied by the energy storage [27] or requires an additional voltage regulator [28] to reduce the output ripple.

As mentioned, threshold voltage or voltage drop of the switching devices (MOS transistor or diode) is the main setback for PCE degradation of the rectifier [5]. The PCE of a rectifier is the ratio of the delivered power at the load system to the received power at rectifier input [23].

A rectifier with lower threshold voltage MOS transistors or lower voltage drop diodes operates with lower received power levels and provides a larger output voltage level [21]. Reducing the threshold voltage statically in forward-bias results in an increase of the leakage current in reverse-bias. A DDCC rectifier [18] is able to cancel the threshold voltage by an active gate bias mechanism leading to reduction of the threshold voltage and leakage current in forward and reverse bias respectively. However, reducing the threshold voltage and leakage current is not always suitable for RFEH systems especially when the harvester is too close to the transmitter or RF source. Under this condition, the output voltage is expected to be limited to protect the succeeding circuitry from being driven with overpower.

A. Body Effect in the DDCC Rectifier

Body-source potential (V_{sb}) is directly related to the threshold voltage of a MOS transistor and often used to manipulate the threshold voltage through a method referred as dynamic voltage-threshold scaling (DVTS) technique [29]. in reference to the classic theory, the leakage current in the reverse bias mode can be determined as [30]:

$$I_{leakage} = I_0 . \left(\frac{W}{L}\right) . \left(e^{\frac{V_{gs} - V_{th}}{nV_T}}\right) . \left(1 - e^{\frac{-V_{ds}}{V_T}}\right) \quad (1)$$

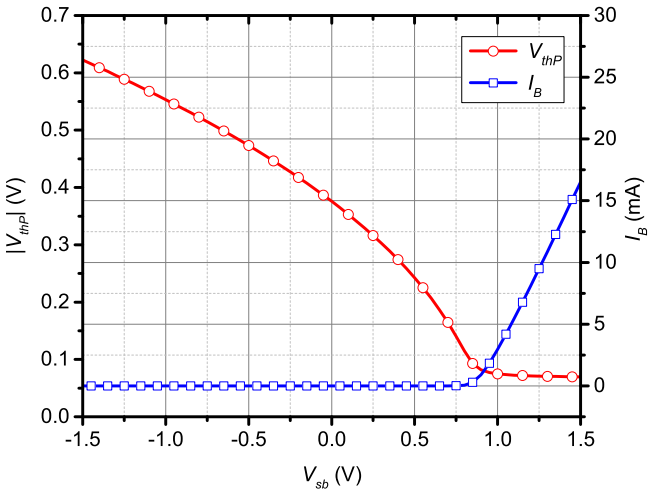


Fig. 2. Simulated threshold voltage and body current variation as a function of V_{sb} for PMOS transistor.

where I_0 is a process-dependent parameter, V_T is the thermal voltage and W/L is the aspect ratio of the transistors. The channel-length modulation effect is negligible for the operation frequency lower than C-band and further strengthen by the fabrication process in a standard 130 nm CMOS. For higher frequency bands operation and sub-micron CMOS technology, this effect becomes more conspicuous and should be taken into account.

Moreover, threshold voltage of a n-type or p-type MOS transistor in forward bias is expressed as [30]:

$$V_{thN} = V_{th0N} + \gamma \left(\sqrt{|2\Phi_F + V_{sb}|} - \sqrt{|2\Phi_F|} \right) \quad (2)$$

$$V_{thP} = V_{th0P} - \gamma \left(\sqrt{|2\Phi_F - V_{sb}|} - \sqrt{|2\Phi_F|} \right) \quad (3)$$

where V_{th0N} and V_{th0P} are the threshold voltages when V_{sb} is zero. γ is the body effect coefficient and $2\Phi_F$ is the surface potential coefficient. In reference to (2) and (3), threshold voltage can be only be dictated by V_{sb} since other parameters are much dependent upon the material properties of the CMOS process which are not easily adjustable unless the design is implemented in a customized process which bottlenecks in the fabrication cost.

In addition, a trade-off between threshold voltage and leakage current usually exists which limits the degree of freedom for threshold voltage reduction [see (1)]. Thanks to the inherent attributes of the DDCC rectifier, the leakage current is considerably restrained. Hence, it is feasible to reduce the threshold voltage to some extent by regulating V_{sb} without any major increase in the leakage current especially for PMOS transistors where the N-wells are isolated which allows the body to be freely biased. However, excessive threshold voltage reduction translates into PCE degradation which will be explained in Section IV. Also to be noted that, NMOS transistors are required to be implemented in a triple-well, also known as deep N-well (DNW), structure to allow the body to be independently biased.

Fig. 2 depicts the simulation result of V_{th} as a function of V_{sb} for a PMOS transistor while the drain-to-source voltage is set to -3.0 V and the width of transistor is set to 20 μm with 130 nm of length. The V_{th} curve shows gradual drop as V_{sb} increases till the PN junction between the source and the body turns "on" ($V_{sb} > 0.7$ V). Further increase does not affect V_{th}. Therefore, the body biasing of rectifier's PMOS transistors can be regulated in order to decrease the V_{th}.

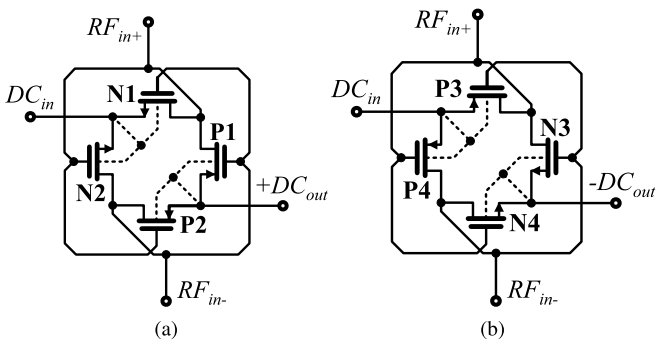


Fig. 3. Conventional source-to-body (SB) biasing structures for differential-drive cross-coupled (DDCC) rectifier. (a) Positive. (b) Negative rectifier.

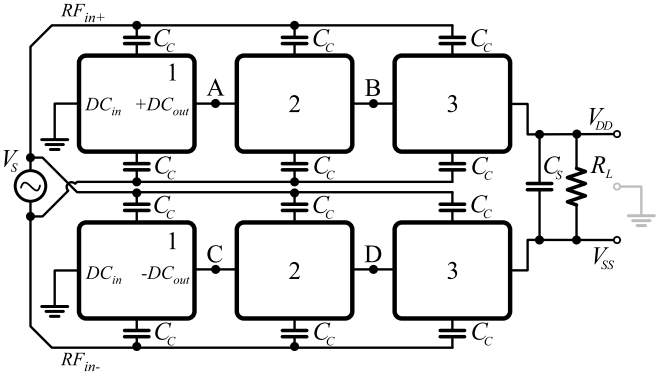


Fig. 4. A typical double-rail multi-stage DDCC rectifier configuration with 3 stages.

Fig. 3 illustrates circuit configuration of a DDCC rectifier. A symmetric rectifier as a dc power supply for wireless sensors increases the rectification efficiency and alleviates the non-linearity of input resistance while making the interface more efficient to the antenna. It also provides a condition for the succeeding analog circuits to be more flexible and efficient [31]. In Fig. 3, a two-cell rectifier is considered in which Fig. 3(a) (N1, N2, P1 and P2) and Fig. 3(b) (N3, N4, P3 and P4) are the positive and negative rectifiers respectively, which generate a symmetric dc voltage [32].

In a multi-stage DDCC rectifier, cells are stacked in series through the extracted dc path and connected in parallel via coupling capacitors (C_C) to the input terminals which feed the rectifier with RF signals (it is usually emulated by a sinusoidal voltage source). The number of stage is usually determined by the required output voltage and dependent on the harvester application. Fig. 4 depicts a double-rail three-stage DDCC rectifier driving a load (R_L). Smoothing capacitor (C_S) is usually connected in parallel with the load to mitigate the ripple at the output.

Conventionally, V_{sb} is set to 0 by connecting source to body to reduce the body effect as depicted in Fig. 3. This configuration drives the transistors to operate with a fixed V_{th} and keeps

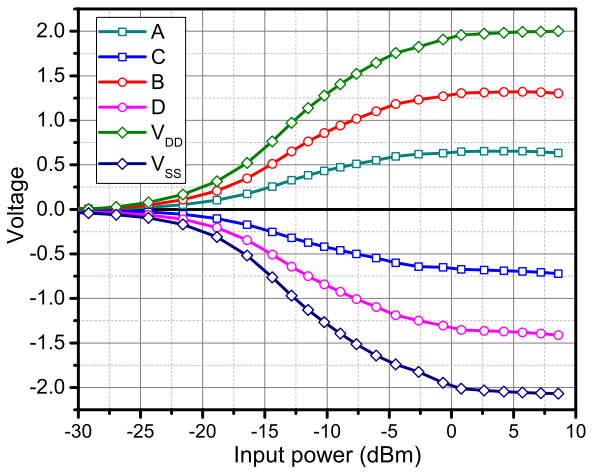


Fig. 5. Generated dc voltage in each cell versus input power in a rectifier using SB biasing technique at 953 MHz driving a 100 kΩ.

the leakage current relatively low. However, by examining the operation mechanism of the DDCC rectifier [18], a degree of freedom exists to reduce V_{th} by biasing transistors' body without any considerable increase in the leakage current since the gate of those transistors that are in the reverse bias are negatively biased leading to a controlled leakage.

III. Proposed Body-Biasing Configuration

As mentioned, transistors' body can be configured to moderately control V_{th}. The regulated V_{th} provides a condition for the rectifier to operate with dynamic efficiency. As concluded in Section II, V_{sb} should be configured with a positive dc voltage for the PMOS transistors in the DDCC rectifier to minimize the body effect especially for smaller received power. In other words, V_b is required to be biased by a lower dc voltage than V_s. In the DDCC rectifier structure, this dc voltage can be provided from each cell output. Fig. 5 depicts each cell output (A, B, C, D, V_{DD} and V_{SS} of Fig. 4) versus input power to drive a 100 kΩ load at 953 MHz operating frequency when source-to-body (SB) biasing technique is adopted. The generated dc voltage level in each cell varies by amount of input power as shown in Fig. 5. Due to the symmetric capability of the rectifier, both negative and positive dc voltages are provided. Therefore, the body of PMOS transistors should be connected to DC_{in} and DC_{out} for positive and negative rectifier rail respectively in order to be biased with a positive dc voltage.

Fig. 6 illustrates the circuit configuration of proposed body biasing scheme referred as lower dc feeding (LDCF) technique. In this configuration, the body of NMOS transistors are tied to source whereas PMOS transistors' body is connected to DC_{in} and DC_{out} in the positive and negative rectifier rail respectively. Therefore, NMOS transistors operate with non-scalable V_{th} since the V_{sb} is 0 while PMOS transistors operate with a scalable V_{th} since V_{sb} is no longer equal to zero.

Constructing a multi-stage rectifier based on Fig. 4 and adopting LDCF body biasing scheme allows PMOS transistors' body to be fed by the generated dc voltages. In the positive rectifier rail, the body of PMOS transistors are biased

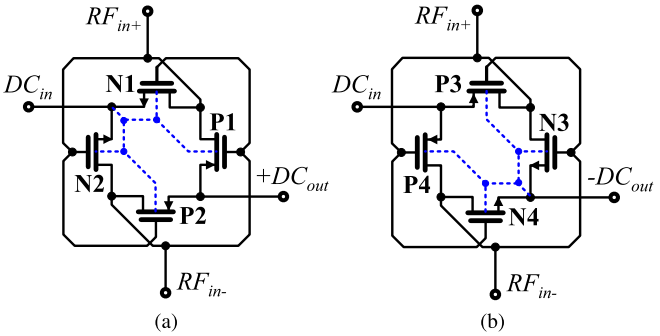


Fig. 6. Circuit configuration of proposed lower dc feeding (LDCF) body biasing technique for DDCC rectifier. (a) Positive. (b) Negative rectifier.

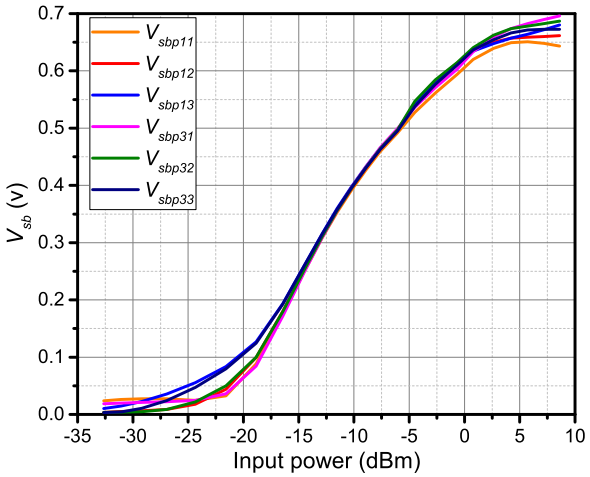


Fig. 7. V_{sb} of PMOS transistors as a function of input power driving a 100 kΩ load.

by the dc output of $(n-1)$ while they are fed by the output of $(n+1)$ for the negative rectifier rail where n represents the cell number in the Fig. 4. Hence, the effective value of V_{sb} is always positive since $V_s > V_b$ for all cells. Here, V_{sbpxn} can be defined where x denotes the PMOS number and n corresponds to the cell number. Therefore, in the positive and negative rectifier rail, body of two PMOS transistors in each cell are identically biased and

$$\left\{\begin{array}{lll} V_{sbp11} = V_{sbp21} & \& & V_{sbp31} = V_{sbp41} \\ V_{sbp12} = V_{sbp22} & \& & V_{sbp32} = V_{sbp42} \\ V_{sbp13} = V_{sbp23} & \& & V_{sbp33} = V_{sbp43} \end{array}\right\} \quad (4)$$

Fig. 7 depicts V_{sb} of all PMOS transistors in a double-rail three-stage rectifier using LDCF technique. The curves of V_{sb} are relatively equal over the range of input power between -35 and 5 dBm. It can be concluded that all bodies are almost equally biased with the same potential and smaller than the source. V_{sb} rises as input power increases leading to reduced V_{th}.

In DDCC rectifier structure, the gate-to-source capacitance (C_{gs}) of the transistors, which correlates with the aspect ratio, increases when the operation frequency is raised and causes the input parasitic capacitance C_{in} to become larger. Consequently, the transistors operate in weak inversion region

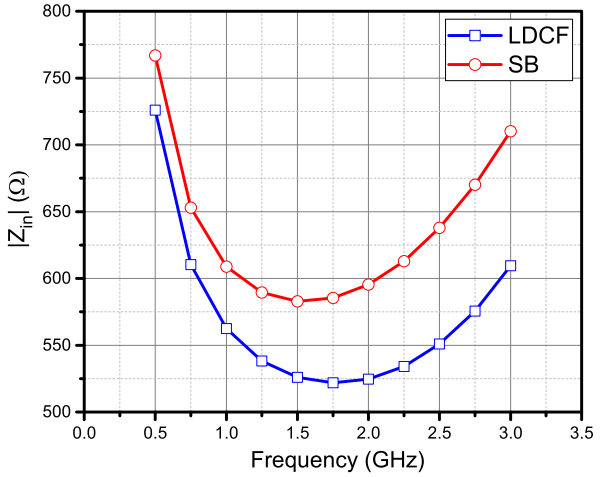


Fig. 8. Simulated input impedance $|Z_{in}|$ of the rectifiers as a function of frequency under a 10 kΩ load at −6 dBm.

due to the reduction in the differential voltage and an increase in input impedance caused by C_{in}, and resulting in PCE degradation [33]. Since the scope of this work is confined for the operating frequencies between 953 MHz and 2 GHz, the size of transistors has been set through multiple iterations in the simulation so that C_{in} moderately affects the PCE at the operation frequency between 953 MHz and 2 GHz. Fig. 8 depicts the simulation results of the input impedance ($|Z_{in}|$) of both LDCF and SB rectifier as function of operating frequency while driving a 10 kΩ load at −6 dBm of input power. $|Z_{in}|$ of the rectifiers decreases with an increase of frequency till it reaches to the minimum point (between 1.5 and 1.75 GHz). The rectifiers encounter larger $|Z_{in}|$ with further increase in frequency due to the increase in input reactance. Noted, the $|Z_{in}|$ of the LDCF rectifier is relatively smaller than the SB rectifier.

IV. Measurement Results and Discussion

A. Circuit and PCB Design

Both LDCF and SB biasing techniques have been implemented in two separate rectifiers with identical design specifications. The rectifiers were designed in a double-rail three-stage configuration with total transistor width of 25 μm and 40 μm for NMOS and PMOS, respectively. The length of 130 nm was chosen for both transistor types. This aspect ratio between NMOS and PMOS transistors approximates the ON-resistances be almost identical. Metal-Insulator-Metal (MIM) type was selected for coupling and smoothing capacitors. 600 fF MIM coupling capacitors (C_C) were deliberately implemented to exhibit a relatively less effect on the conversion efficiency. A 3.2 pF MIM smoothing capacitor (C_S) was selected in order to mitigate the output ripple. Table I lists the component's value. The component's value were obtained after multiple iterations so that they do not considerably degrade the PCE. The rectifiers have been fabricated in 130 nm CMOS technology. The die photograph of the fabricated chip is illustrated in Fig. 9(a) with a total chip area consumption of 0.954 mm^2 including the RF pads. However, an active area of 0.029 mm^2 was dedicated to each rectifier. Due to the negligible substrate loss, no de-embedding block is needed to be integrated to the chip. The RF pad in the design kit offers ESD protection capability which requires the pads to be biased by a dc voltage. All the RF pads were biased with 3 V and ground except the RF pads which are associated to V_{SS}s (output of negative rectifiers rail) signal were biased with −3 and 3 V to keep the original signals untouched. A FR4 PCB was implemented in order to realize a variable resistor to emulate the load system R_L and subsequently to evaluate the rectifiers under different load conditions.

TABLE I
Components Values of the LDCF and SB Rectifiers

Component	Value
C_C	600 fF
C_S	3.2 pF
Width n-type	25 μm
Width p-type	40 μm
Length N&PMOS	130 nm

B. Measurement Setups and Procedures

An on-wafer measurement technique was used to evaluate the rectifiers performance. Two differential probes were dedicated for the input and output. E8267D PSG was used along with a broadband balun in order to generate a differential signal and eventually to drive the rectifiers. The balun was characterized via E8364B PNA. The loss of the cables were also considered and measured using E4440A PSA. The total output dc voltage which is equal to $V_{DC} = V_{DD} - V_{SS}$ was measured using a digital multimeter. Fig. 9(b) shows a photo of the measurement setup. The rectifiers' PCE can be calculated as

$$PCE(\%) = \frac{P_{DC}}{P_{rcv}} \times 100 \tag{5}$$

where P_{rcv} is the received power at the input of the rectifiers and P_{DC} is the power delivered to the load system. For overall system optimization the antenna and the rectifier require an impedance matching circuit between them, but here we assume a perfect impedance matching. The performance of the rectifiers was evaluated by P_{rcv} which can be calculated as:

$$P_{rcv} = \left(P_{av} - P_{closs}\right).\left(1 - |\, S_{dd11}\,|^2 - |\, S_{cd11}\,|^2\right) \tag{6}$$

where

$$P_{av} = \left(P_S\right).\left(1 - |\, S_{ds21}\,|^2\right) \tag{7}$$

P_S is the power generated by PSG, S_{ds21} represents the insertion loss by the balun, P_{av} is the available power at the balun's output, P_{closs} denotes the power losses through the cables, while S_{dd11} and S_{cd11} are the rectifier's reflection coefficients for differential-to-differential and differential-to-common modes respectively. The reflection coefficients of the rectifiers and the insertion loss of the balun were obtained using transformation of the standard S-parameters matrix to mixed-mode S-parameters matrix [34], [35]. The calculated

TABLE II
TRANSFORMED MIXED-MODE SCATTERING PARAMETERS

Frequency (MHz)	Balun S_{ds21}	SB S_{dd11}	SB S_{cd11}	LCDF S_{dd11}	LCDF S_{cd11}
500	0.327-j0.628	0.245-j0.759	0.247+j0.009	0.236-j0.768	0.221-j0.022
953	-0.368-j0.601	0.361+j0561	-0.188+0j231	0.375+j0.566	-0.146+j0.218
2000	-0.208+j0.653	-0.563+j0.151	-0.181-j0.354	-0.592+j0.171	-0.18-j0.291

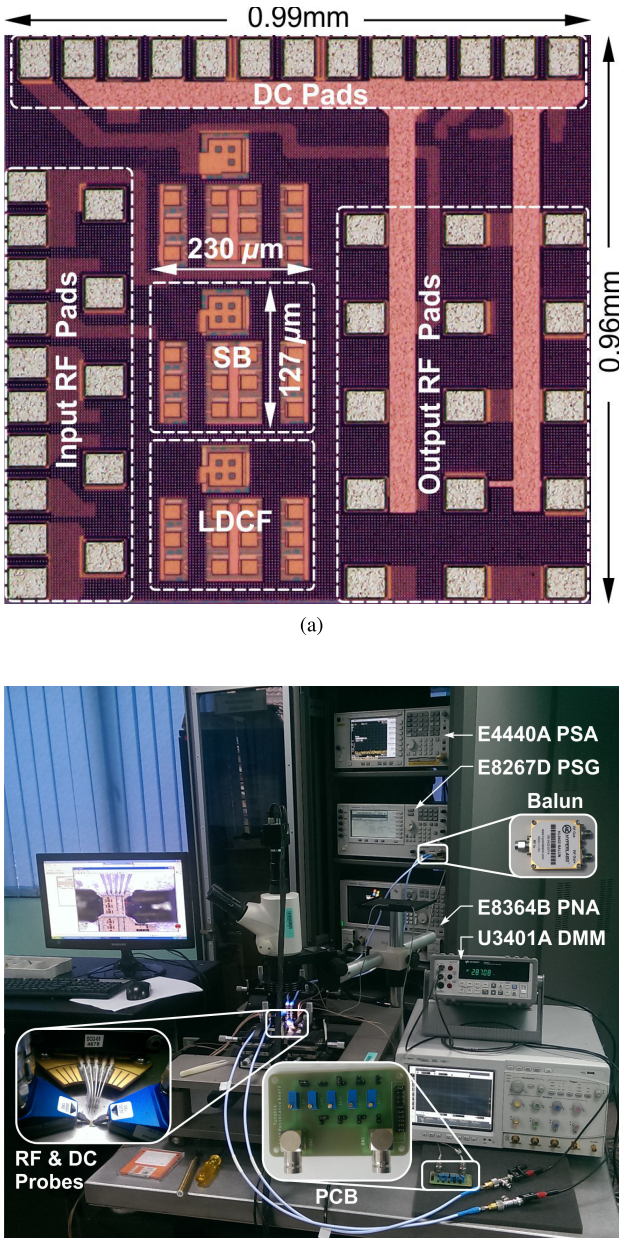


Fig. 9. (a) Photomicrograph of the fabricated rectifiers using the SB and LDCF body biasing techniques. (b) Photograph of probe station and the measurement setup.

mixed-mode S-parameters of the balun and the rectifiers at different frequencies are listed in Table II. DC power dissipation at the rectifier output (P_{DC}) can be obtained through the equation $P_{DC} = V_{DC}^2/R_L$.

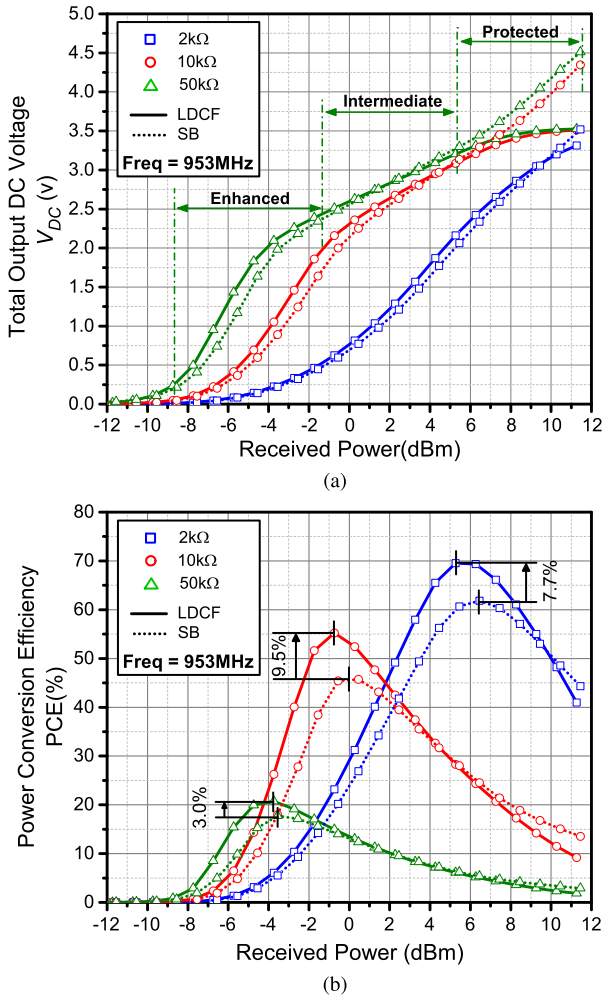


Fig. 10. Measured performance of LDCF and SB rectifiers while they are driving different load resistances. (a) V_{DC} and (b) PCE as function of P_{rcv} at 953 MHz.

C. Rectifier Performance

The performance of the rectifiers using LDCF and SB body biasing techniques are compared in Figs.10–13 under different loads and a variation of frequencies.

At the frequency 953 MHz, which is one of the most common operating frequencies for passive RFID systems and other identification schemes, the LDCF outperforms the SB biasing technique in lower received power region in terms of the generated V_{DC}. Fig.10(a) shows the V_{DC} of each rectifier as a function of P_{rcv} under 3 different loads as 2 kΩ, 10 kΩ and 50 kΩ. Both rectifiers behave almost similar in response to the P_{rcv} variations. V_{DC} rises as the P_{rcv} increases at different slopes. Increasing the load resistance improves the V_{DC} since

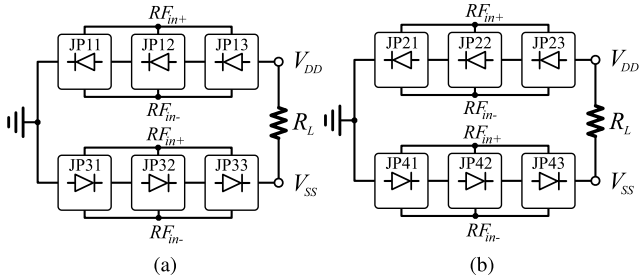
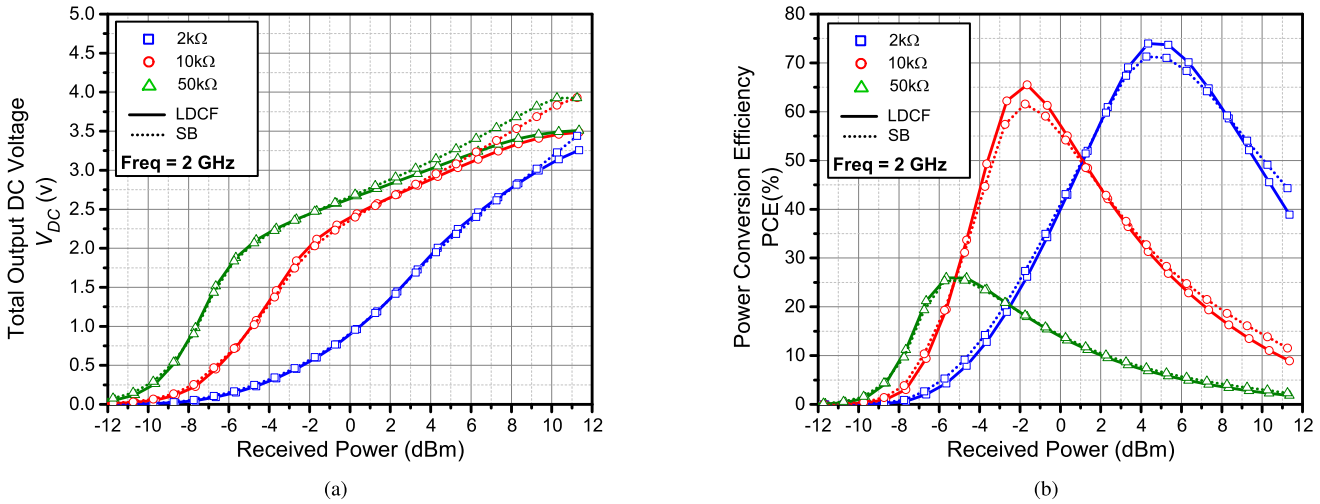


Fig. 11. Simplified LDCF model in the protected region. (a) Positive RF cycle. (b) Negative RF cycle.

a larger load draws less charge from the C_S leading to the storage of more dc voltage. For the rectifier adopting LDCF biasing technique, V_{DC} shows better performance compared to the rectifier with the conventional (SB) biasing technique. The operation of the LDCF rectifier can be categorized into 3 regions. For example, for 50 kΩ load resistance, when the P_{rcv} is between -9 and -1 dBm [Enhanced region in Fig. 10(a)], the rectifier generates larger V_{DC} and the curve shifted to the lower P_{rcv} compared to the SB rectifier. As the P_{rcv} increases and enters to the region between -1 dBm and 5 dBm [Intermediate region in Fig. 10(a)], both rectifiers' V_{DC} are almost equal in terms of magnitude. Further increase in P_{rcv}, raises the V_{DC} for the SB rectifier while the V_{DC} of the LDCF rectifier becomes saturated after 5 dBm [Protected region in Fig. 10(a)] and the V_{DC} does not exceed 3.5 V. The V_{DC} in the far-field RFEH systems hardly reaches up to 5.0 V with a small load [4], [18], [23]. Such systems are usually supplied with a dc voltage around 1.2 V up to 1.8 V. A LDO voltage regulator is commonly used to stabilize the dc voltage fed by the rectifier, regulating towards the circuitry in the system. The level of 3.5 V is a sufficient dc voltage headroom which allows the LDO to operate properly.

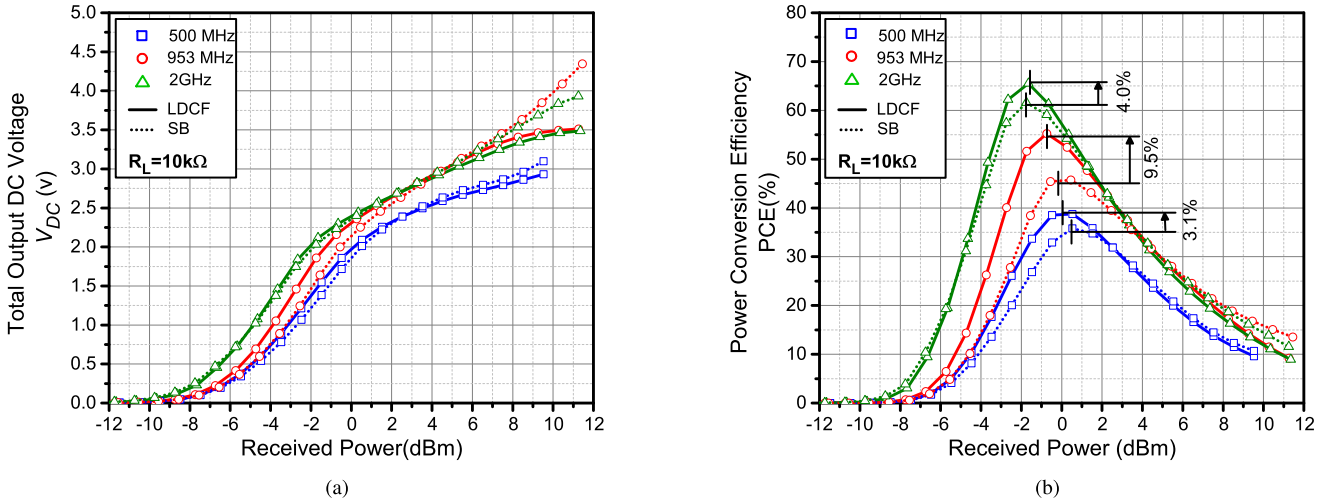
To be more precise, the rectifier using LDCF technique improves the V_{DC} for smaller P_{rcv} since the V_{th} of PMOS transistors in the structure has been mitigated by biasing the V_{sb} with a positive dc voltage in the enhanced region. The V_{sb} of PMOS transistors increase as P_{rcv} increases which causes the source-body PN junction starts to turn "on", and leads to source-body leakage current. In the intermediate region, the source-body leakage neutralizes the V_{th} mitigation and the LDCF rectifier performance becomes almost similar to the SB rectifier. In the protected region, V_{sb} of the PMOS transistors in the LDCF rectifier reaches to 0.7 V (see Fig. 7 for power >5 dBm) which induces the PN junction between the source and the body of the PMOS transistors completely turn "on" and shorts the input and output DC in both positive and negative rectifier cells with a voltage drop through the junction (see connections of the source and the body of P1-4 in Fig. 6). Hence, the voltage difference between the DC_{in} and DC_{out} of each rectifier cell becomes almost equal to the voltage drop of the junction. Since the structure is in a double-rail three-stage configuration, each rail encounters 3 voltage drops with respect to the ground for each RF cycle. The LDCF rectifier in the protected region can be simplified with a model depicted in Fig. 11 in which JPxn denotes the PN junction between the source and the body of PMOS transistor x in stage n. As a result, V_{DC} in the protected region is almost equal to 6 voltage drops which is theoretically expected to be 4.2 V. However, due to the undesirable parasitic effects, the voltage is limited at a lower level at the output of the LDCF rectifier. The turning "on" of PN junction is a gradual process which starts in the intermediate region and is completed in the protected region. From the behavior of the LDCF depicted in Fig. 10(a), it can be concluded that the process of turning "on" is completed when the V_{DC} does not further increase with increase in P_{rcv} which is at 3.5 V. This behavior can be accounted as an advantage since a voltage limiter is usually required in a far-field RFEH system to protect the succeeding circuitry when it is too close to the RF source. Fig. 10(b) illustrates the PCE of both rectifiers as a function of received power under 3 different load resistances at 953 MHz. The PCE increases with P_{rcv} until it reaches its peak and starts to drop with further increase in P_{rcv}. These fluctuations are caused by the leakage current of the transistors. According to the operation mechanism of the DDCC rectifier [18], for each RF cycle two transistors are "on" and the other two transistors are "off". For example, in the positive RF cycle, P1 and N2 in the positive rectifier rail are "on". The drain-gate voltage of the "off" transistors, N1 and P2, increases with larger P_{rcv} and forces the "off" transistors to turn "on". As a result, the current flows in the reverse direction and dissipates the power leading to less charge to be stored in the C_s. PCE increases for lower P_{rcv} region with an increase of load resistance while it degrades considerably at higher P_{rcv} region. The maximum PCE significantly decreases with larger load as well. The rectifiers under a larger load resistance generate a larger dc voltage which again forces the two transistors (N1 and P2 for the positive RF cycle and N2 and P1 for the negative RF cycle) to turn "on" with higher P_{rcv} which are supposed to be in "off" state while at lower P_{rcv}, less dc voltage is generated and the leakage current is suppressed. On the other hand, a smaller load resistance draws larger current at lower P_{rcv} while provides larger maximum PCE at higher P_{rcv} region compared to the larger load resistances.

As depicted in Fig. 10(b), the rectifier with LDCF biasing technique operates with superior PCE at lower P_{rcv} region and inferior at higher P_{rcv} region. In a typical rectifier, the leakage current is mainly due to the source-to-drain leakage of NMOS and PMOS transistors which are suppressed by negatively biasing the gates in the reverse bias condition for the DDCC structure. However, another leakage affects the DDCC rectifier using LDCF technique which is associated with the PN-junction between the source and the body of the PMOS transistors. As P_{rcv} increases, the V_{th} of PMOS transistors decreases which also reduces the power loss and increases the PCE, compared to the SB rectifier, since the V_{th} reduction still does not cause the PN-junction to turn "on". Further increase in P_{rcv} causes excessive reduction in the V_{th} so that the PMOS transistors become highly vulnerable to the reverse bias leakage, and the negative biasing of the gates will no longer be effective to suppress the reverse leakage current. In addition, the PN-junction between the source and the body of PMOS transistors turns "on", and causes the current to leak even in the forward bias. Hence, the summation of leakage



(a) (b)

Fig. 12. Measured performance of LDCF and SB rectifiers while they are driving different load resistances. (a) V_{DC} and (b) PCE as function of P_{rcv} at 2 GHz.



(a) (b)

Fig. 13. Measured performance of LDCF and SB rectifiers at different operating frequencies while driving a 10 kΩ load resistance. (a) V_{DC} and (b) PCE as function of P_{rcv}.

in the forward and reverse bias becomes noticeable and the PCE considerably drops with steeper slope compared to the SB rectifier. This also explains the reasoning that the rectifier behaves like a voltage limiter. The LDCF biasing technique improves the maximum PCE as well. Under 2 kΩ, 10 kΩ and 50 kΩ load resistances, the improvements are 3.0%, 9.5% and 7.7% respectively compared to the rectifier with SB biasing. The maximum PCE at this operating frequency for the LDCF rectifier are measured to be 69.5% at 5.26 dBm, 55.2% at −0.73 dBm and 20.7% at −3.73 dBm while driving a 2 kΩ, 10 kΩ and 50 kΩ respectively.

The LDCF rectifier performance at 2 GHz operating frequency is compared to the SB rectifier in Fig. 12. The operation of LDCF rectifier at this frequency differs as depicted in Fig. 12(a). The output V_{DC} of the rectifiers rises almost equally as P_{rcv} increases while the LDCF rectifier still keeps its self-limiting characteristic and does not allow the V_{DC} to exceed 3.5 V. At lower P_{rcv}, the SB rectifier operates with better PCE to some extent [see Fig. 12(b)] but as P_{rcv} increases, the PCE of the LDCF rectifier becomes larger until it reaches to the maximum peak. Subsequently, the response rolls off with steeper slope leading to self-limiting at the output for higher P_{rcv}. The maximum PCE for the rectifier using LDCF technique under 2 kΩ, 10 kΩ and 50 kΩ are 73.9% at 4.34 dBm, 65.5% at −1.65 dBm and 25.9% at −5.65 dBm respectively. Comparing the simulated and measured maximum PCE, the former is only higher by 17% at 953 MHz with R_L of 10 kΩ. Due to the structure of LDCF rectifier, a voltage difference between the source and the body of PMOS transistors always exist causing considerable parasitic capacitance C_{sb} which is suppressed in the SB rectifier as the source and the body of the PMOS transistors are shorted. The effect of C_{sb} is negligible for lower frequencies but C_{sb} increases with an increase of frequency and causes the LDCF technique to become less effective in improving the PCE. This is the reason the LDCF rectifier is comparatively less effective at 2 GHz. However, the LDCF still exhibits higher maximum PCE compared to the SB rectifier.

TABLE III
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART

	This Work LDCF	This Work SB	[23] TCAS-I'14[1]	[36] TCAS-I'15	[5] TCAS-I'15
Technology	**130 nm**	130 nm	180 nm	180 nm	130 nm
Topology	**DDCC**	DDCC	DDCC	Dickson-based	Dickson-based
Frequency	**953 MHz**	953 MHz	900 MHz	433 MHz & 925 MHz	902-928MHz
Load (R_L)	**2 kΩ**	2 kΩ	2 kΩ	-	1 MΩ
PCE	**69.5%**	61.8%	75%	<50%	32%
Input	**5.2 dBm**	6.4 dBm	-7 dBm	-15 dBm	-15 dBm
Max V_{DC}	**3.5 V**	3.9 V	2.0 V	-	5.0 V
Number of stage	**3 double rail**	3 double rail	1	-	12
Output Self-Limiting Capability	**Yes**	No	No	No	No
Output Symmetric Capability	**Yes**	Yes	No	No	No

[1]The performance of the integrated rectifier is reported based on simulation results.

The frequency response analysis for a DDCC rectifier when the rectifier adopts the LDCF self-body biasing technique can be done for a specified condition. The performance of the rectifier strongly depends on the driving load and the operating frequency. One way to deliver a relatively an acceptable analysis is to select a specified load and analyze the rectifier in terms of the frequency response. A 10 kΩ load was selected and the performance of the rectifiers have been analyzed with respect to the P_{rcv} at three different frequencies and the measurement results are depicted in Fig. 13. Increasing the frequency from 500 MHz to 2 GHz improves the performance of both LDCF and SB rectifiers. For the LDCF rectifier the measured V_{DC} is slightly improved compared to the SB rectifier at smaller P_{rcv} region [see Fig. 13(a)]. Fig. 13(b) illustrates PCE of the rectifiers. As a perfect matching condition is assumed for the measurement, for the performance analysis it can be referred to the input impedance of the rectifiers for selected frequencies which is depicted in Fig. 8 in which both rectifiers exhibit a fall and rise between 500 MHz and 3 GHz with a minimum point at approximately 1.75 GHz for the selected power and load. The input impedance is mainly under influence of the input reactance which is predominated by the parasitic capacitances of the transistors in both rectifiers. Maximum PCE is observed at the frequency where the rectifiers input impedance is minimum which explains why the increasing in the frequency from 500 MHz to 2 GHz improves the PCE in Fig. 13(b). However, a PCE comparison indicates that the LDCF achieves the maximum improvement of 9.5% at 953 MHz which was the preferred frequency for the optimization of design parameters in this work. In addition, the LDCF rectifier improves the PCE by 3.1% and 4% at 500 MHz and 2 GHz respectively.

As a crucial measurement parameter, V_{DC} of 15 different samples of the fabricated LDCF rectifier has been measured at two frequencies of 953 MHz and 2 GHz while driving a 10 kΩ load. The corresponding received power at 953 MHz and 2.0 GHz were calculated as 3.26 dBm and 3.34 dBm respectively. The results were fairly consistent as depicted in the Fig. 14.

The performance summary of the rectifiers in this work is listed in Table III and fairly compared with the state-of-the-art reported architecture [5], [23] and [36]. The LDCF rectifier in this work outperforms other works in terms of maximum efficiency while driving a heavy or smaller load with an inherent limitation capability which non of the listed work offers. The simulated PCE reported in [23] is larger than measured PCE of the LDCF rectifier since in this work a double-rail three-stage rectifier is adopted in order to generate a symmetric dc voltage at the output. Hence, The LDCF rectifier faces more PCE degradation compared to single-rail single-stage architecture in [23]. However, the maximum V_{DC} of the LDCF rectifier is comparatively larger.

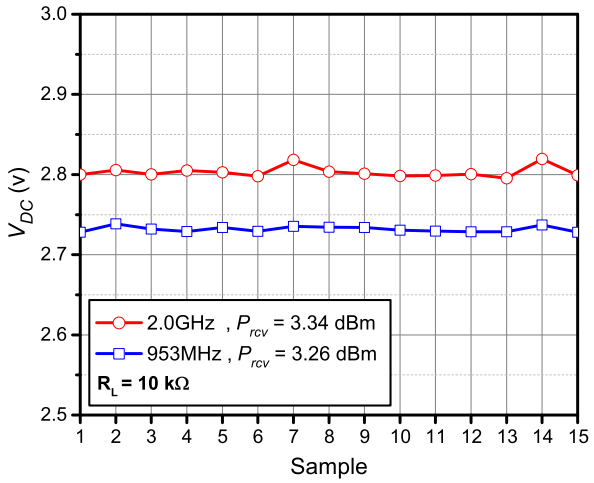


Fig. 14. Output DC voltage V_{DC} measured with 15 different samples of the fabricated LDCF rectifier.

V. CONCLUSION

A novel self-body-biasing technique, known as LDCF, was proposed and compared with the conventional body-biasing technique for DDCC rectifier used in far-field RF energy-harvesting systems. The technique enables the integrated PMOS transistors in the rectifier to operate with a scalable V_{th} leading to an improvement of the output V_{DC} and PCE at smaller received power. The technique also allows V_{DC} saturation and PCE reduction at larger received power

which can be considered as a self-limitation capability to protect the succeeding circuits in a wireless sensor from being overpowered.

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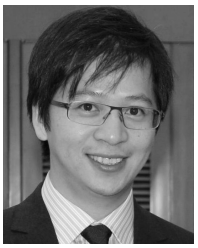

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Rui P. Martins (M'88–SM'99–F'08), born in April 30, 1957, received the B.S. (5-years), M.S., and Ph.D. degrees, as well as the Habilitation for Full-Professor in electrical engineering and computers, from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively. He has been with the Department of Electrical and Computer Engineering (DECE) / IST, TU of Lisbon, since October 1980. Since 1992, he has been on leave from IST, TU of Lisbon (now University of Lisbon, since 2013), and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor since August 2013. In FST he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed (in 2013), as Vice-Rector (Research) until August 31, 2018. Within the scope of his teaching and research activities he has taught 21 bachelor and master courses and has supervised (or cosupervised) 40 theses, Ph.D. (19) and Master's (21). He has coauthored 6 books and 9 book chapters (refereed); and 18 Patents, USA (16) and Taiwan (2); 355 papers, in scientific journals (104) and in conference proceedings (251); as well as another 55 academic works, in a total of 443 publications. He was a cofounder of Chipidea Microelectronics (Macao) [now Synopsys] in 2001/2002, and created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory of UM, elevated in January 2011 to State Key Laboratory of China (the 1st in Engineering in Macao), being its Founding Director (http://www.amsv.umac.mo/). Prof. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005, and of the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/ Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of the IEEE Circuits And Systems Society (CASS)]. He was the General Chair of 2008 IEEE Asia-Pacific Conference on CAS– APCCAS 2008, and was the Vice-President for the Region 10 (Asia, Australia, the Pacific) of IEEE CAS Society (2009-2011). Since then, he was Vice-President (World) Regional Activities and Membership of IEEE CAS Society (2012-2013), and Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (2010-2013), nominated Best Associate Editor of TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS for 2012 to 2013. Plus, he was a member of the IEEE CASS Fellow Evaluation Committee (2013 and 2014), and the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—Director of the IEEE. He was the General Chair of Asia South Pacific Design Automation Conference ASP-DAC2016. He is currently a Nominations Committee Member of IEEE CASS. He was also the recipient of 2 government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese academician living in Asia.