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MIXED SIGNAL LETTER

LC-VCOs using spiral inductors with single- and dual-layer patterned floating shields: a comparative study

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Abstract This letter studies and compares class-B VCOs using spiral inductors with the proposed dual-layer patterned floating shield (DL-PFS) and conventional single-layer patterned floating shield (SL-PFS). The proposed DL-PFS technique utilizes two lowest metal layers to effectively reduce the capacitive induced current to the substrate in an on-chip spiral inductor, thereby boosts its Q-factor by 40% when compared with the conventional SL-PFS approach. We fabricated, as a proof of concept, the class-B LC-VCOs using the DL-PFS and SL-PFS in 0.13 μm CMOS. Operating at 10 GHz, the VCO with the DL-PFS inductor measures a 3.6 dB phase noise (PN) improvement at the same power consumption of 2.12 mW. Specifically, the VCO with DL-PFS inductor is tunable from 9.3-to-10.1 GHz and measured PN at 10 GHz is −132.5 dBc/Hz at 10 MHz offset while consuming 2.12 mW at the lowest 0.6 V supply. The achieved figure-of-merit (187.4 dBc/Hz@1 MHz offset) compares favorably with the recent state-of-the-art.

Keywords Inductor · Patterned floating shield · Substrate · CMOS · VCO

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1 Introduction

Phase noise performance of the voltage controlled oscillators (VCOs) is often degraded by the limited Q-factor due to non-zero resistivity of the metal trace, skin/current crowding effect and substrate loss from electromagnetic (EM) coupling [1]. Although proper geometrical design, exploiting thick top metal, can alleviate the first two issues mentioned above, respectively, but EM loss is still a major concern especially at high operating frequency.

Patterned ground shield (PGS) implemented using polysilicon was firstly used to block the electric field from penetrating the silicon substrate [2]. However, it requires a near ideal ground which is difficult to achieve due to finite conductivity and parasitic inductance of the metals connecting to substrate ground, or noise coupled between close-by circuits. To circumvent these, patterned floating shield (PFS) using metal strips has been demonstrated with better shielding performance when compared with PGS [3], since the reflection loss for near field electric sources requires shield with higher conductivity.

This letter demonstrates an improved dual-layer PFS (DL-PFS) by optimally utilizing two lowest metal layers, exhibiting a significant improvement in the Q factor. Although the dual-layer patterned floating shield has been studied in [4], it lacks of experimental proof and specific design strategies for the floating shield. Thus, Sect. 2 describes the design considerations for the DL-PFS. Section 3 exhibits the experimental characterization of the performances of the class-B VCOs using DL-PFS and SL-PFS inductors, proving the improvement of the inductor Q-factor. Finally, Sect. 4 draws the conclusion.

2 Proposed dual-layer PFS (DL-PFS)

Conventionally, in the design of the single-layer PFS (SL-PFS) the metal slits are perpendicular to the current flow in the inductor [3] as shown in Fig. 1. This, as Fig. 2 shows, terminates the induced current flowing tangentially to the surface of the substrate in X and Y directions. However, this approach is only effective for square inductors, but not for the commonly used octagonal spiral inductors, as there are both X and Y directed currents induced on the substrate along the diagonal sides. In other words, the current on the substrate flows radially out from the inductor turns, indicating an electrically induced current [5].

Figure 3 shows the proposed DL-PFS, where we utilize Metal-1 and Metal-2 to ensure minimized coupling between the inductor at the top metal. The shield is also

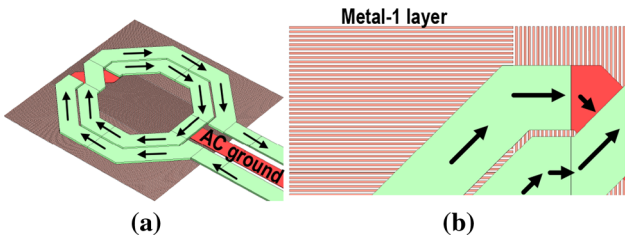

Fig. 1 **a** Spiral inductor with conventional SL-PFS using metal-1, and **b** zoom-in view of the PFS

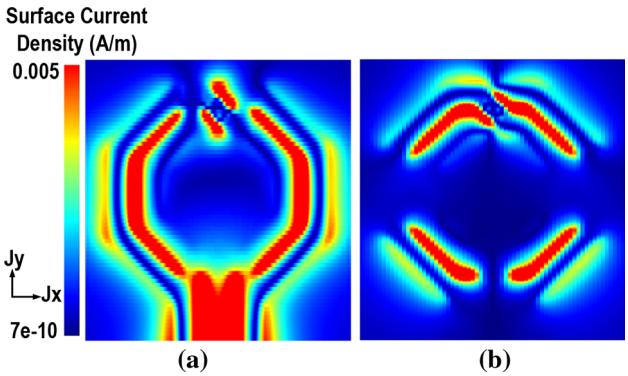

Fig. 2 Simulated surface current density induced on the substrate in: **a** X direction, and **b** Y direction

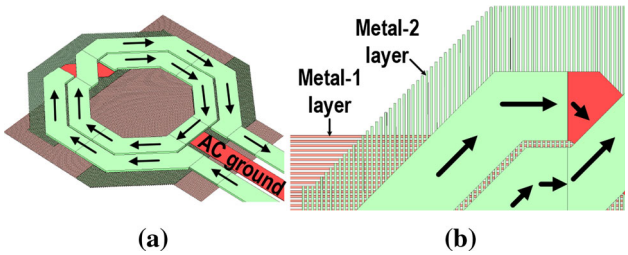

Fig. 3 **a** Proposed DL-PFS underneath the spiral inductor, and **b** zoom-in view of DL-PFS

significantly thinner than the skin depth to guarantee the shielding effectiveness against the electric field by means of reflection. Several issues should be considered in the selection of the width and the gap. First, it is crucial to ensure that the inductance of the metal strips is lower than the inductor being shielded, hence leading to a desired smaller width and gap. However, as shown in [2] and [5], we observe a negligible improvement in the Q factor and the degradation in the self-resonance frequency (f_{SR}) as the width and gap decrease beyond 1 μm. Therefore, the width and gap are deliberately selected as 1 μm. We positioned metal-1 horizontally to reduce the induced current in the X-direction tangential to the substrate, and metal-2 vertically to reduce the induced current in the Y-direction, where it is dominant underneath along the diagonal path of the inductor.

Figure 4 shows the surface current density on the substrate of the unshielded inductor, and on the inductor with SL-PFS and DL-PFS from the Sonnet EM simulation. Due to the absence of vertical metal slits along the diagonal path, the current induced on the substrate for the inductor with SL-PFS is still significant [Fig. 4(b)]. However, induced substrate current is greatly suppressed by DL-PFS [Fig. 4(c)], reflecting a huge improvement in the Q factor as shown in Fig. 5, in which DL-PFS achieves a peak Q of 38. The Q factor of the inductor with DL-PFS is 40% higher when compared to the SL-PFS at 10 GHz. For the same area, inductance is also increased as a result from the proposed DL-PFS. In addition, by comparing SL-PFS and diagonal SL-PFS, we also observed no difference in the Q factor as shown in Fig. 6. Table 1 summarizes the technology parameters used and the performance parameters of the inductors at 10 GHz.

3 Measurement results

We implemented and fabricated in 0.13-μm 1P8 M CMOS with 3.3 μm-thick-top metal, as a proof of concept, the unshielded, SL-PFS and DL-PFS inductor in a class-B

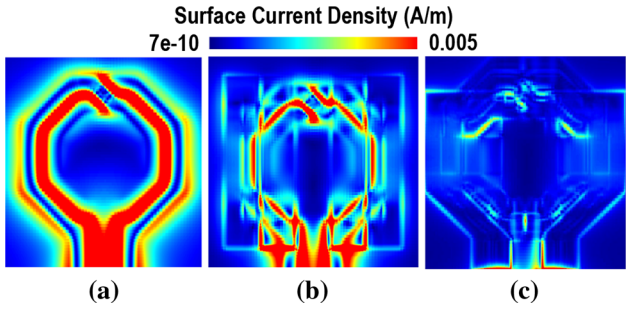

Fig. 4 Magnitude of the surface current density induced on the substrate at 10 GHz for **a** non-shielded inductor, **b** conventional SL-PFS, and **c** proposed DL-PFS

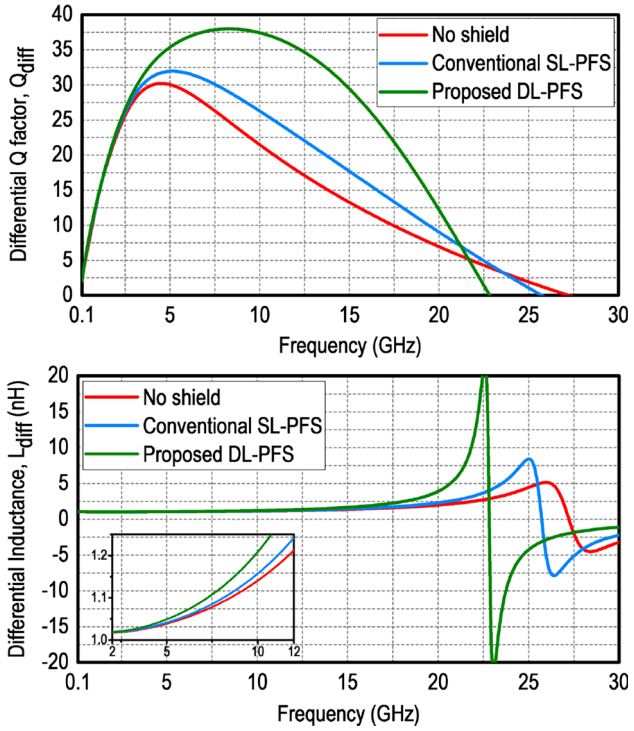

Fig. 5 Simulated Q factor (*top*) and inductance (*bottom*) of the inductors without shields, with conventional SL-PFS and proposed DL-PFS

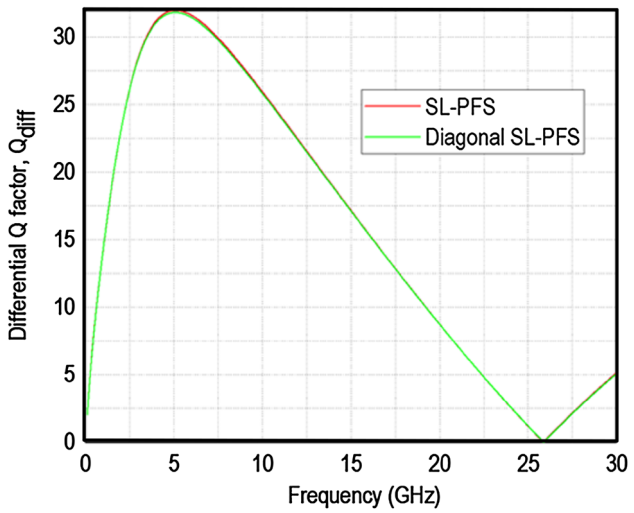

Fig. 6 Q factor comparison between SL-PFS and diagonal SL-PFS

VCO with a tail current source, occupying 0.2 mm^2 of core area for each VCO. Each inductor has 140 μm inner diameter with 25 μm trace width, separated by 3 μm gap. The VCOs are supplied with a minimum of 0.6 V, since $V_{DD(min)} = V_{TH} + V_{DS(tail)}$, assuming $V_{TH} \cong 400$ mV and $V_{DS(tail)} = 0.5V_{TH}$ to guarantee the tail transistor to operate in saturation region. Figures 7 and 8 show the schematic of the VCO and the photomicrograph of the chip respectively where it is tunable from 9.3-to-10.1 GHz.

Figure 9 depicts the measured phase noise (PN) of the three VCOs with a 10 GHz carrier at 2.12 mW. The DL-PFS inductor shows 3.6 dB improvement in PN at 10 MHz-offset when compared with the SL-PFS. This is in agreement with the PN expression in $1/f^2$ region [6] according to the impulse-sensitivity function (ISF),

Table 1 Summary of technology parameters and performance parameters at 10 GHz

Substrate resistivity (Ω cm)			10
Width of the trace (μm)			25
Inner diameter (μm)			140
Trace gap (μm)			3
Metal thickness (μm)			3.3
Inductor type	Non-shielded	SL-PFS	DL-PFS
Inductance (nH)	~1.13	~1.15	~1.2
Q	~21.5	~26.9	~37.5
Self-resonant frequency (GHz)	~27	~26	~22.6

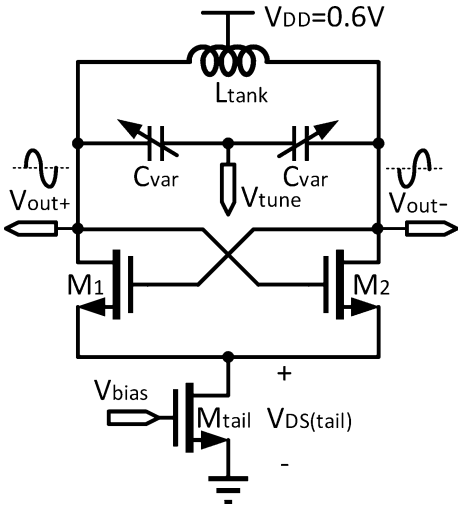

Fig. 7 Schematic of the class-B VCO

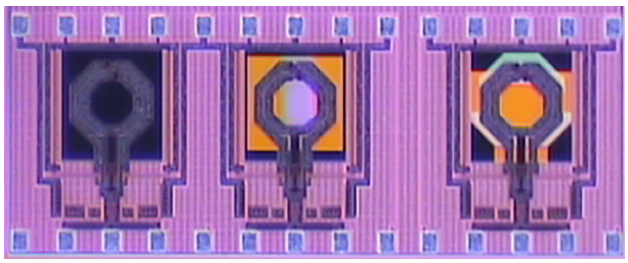

Fig. 8 Photomicrograph of the VCOs with non-shielded inductor (*left*), conventional SL-PFS (*middle*) and proposed DL-PFS (*right*)

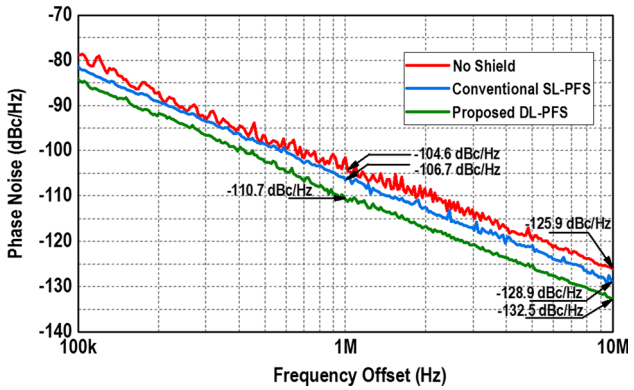

Fig. 9 Measured PN versus frequency offset at 10 GHz carrier

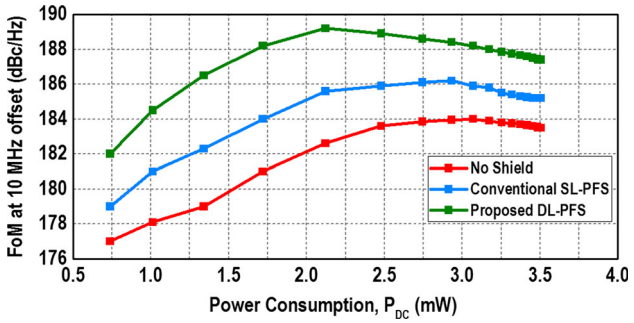

Fig. 10 Measured FoM against power consumption

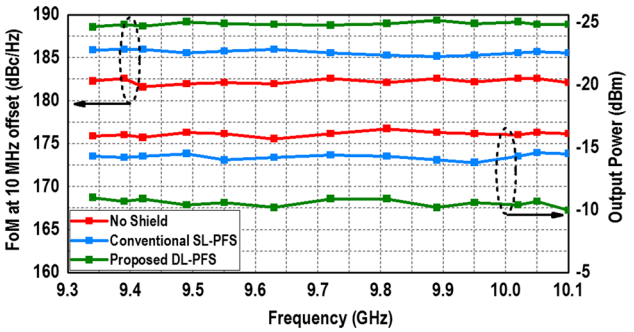

Fig. 11 Measured FoM and output power against frequency

$$\mathcal{L}(\Delta f) = 10\log\left[\frac{kT}{Q^2}\cdot\frac{\Gamma_{T,rms}^2+\gamma\Gamma_{M,rms}^2+\gamma\Gamma_{tail,rms}^2 g_{mT}R_P}{I_{RF}V_{RF}}\cdot\left(\frac{f_0}{\Delta f}\right)^2\right] \quad (1)$$

where Q is the tank's quality factor, $\Gamma_{T,rms}^2$, $\Gamma_{M,rms}^2$, $\Gamma_{tail,rms}^2$ are the rms ISF associated with the tank loss, MOS cross-coupled pair and tail transistor respectively, γ is the MOS channel noise factor, V_{RF} and I_{RF} are the rms values of voltage and current across the LC tank. For a sinusoidal oscillation, $\Gamma_{T,rms}^2 = \Gamma_{M,rms}^2 = 1/2$, $\Gamma_{tail,rms}^2 = 0.085$ for class-B VCO with a conduction angle of $\pi/2$. Based on (1), 40% improvement in the inductor Q factor yields 4.38 dB

Table 2 Performance benchmark with the state-of-the-art VCOs

Topology	This work			[8]	[9]	[10]	[11]
	Inductor w/DL-PFS	Inductor w/SL-PFS	Non-shielded inductor	Current reuse Colpitts	Hybrid class AB/B	Current reuse hybrid class B/C	Class-B NMOS top biased
Power (mW) @ supply (V)	2.12@0.6 V†	2.93@0.6 V†	3.07@0.6 V†	2.1@1.2 V	2.4@0.75 V	2.2@1.2 V	3@1.2 V
Frequency (GHz)	10	10	10	9.41	12.7	11.17	7.9
Tuning range (GHz)	9.3–10.1 (8.25%)	9.31–10.16 (8.73%)	9.33–10.2 (8.91%)	8.57–10.21 (17.4%)	10.1–13.15 (25.6%)	10.15–11.17 (9.57%)	7.5–10.6 (31%)
PN @ 1/10 MHz (dBc/Hz)	−110.7/−132.5	−108.1/−130.9	−105.9/−128.9	−110.6/−130.6*	−104.5/−124.5*	−107.7/−127.7*	−105/−125*
FoM @ 1/10 MHz (dBc/Hz)	187.4/189.2	183.4/186.2	181/184	186.9/186.9	182.8/182.8	185.2/185.2	178.2/178.2
Core area (mm^2)	0.2			0.45**	0.59**	0.07	0.33
Technology	0.13 μm CMOS			0.13 μm CMOS	0.18 μm CMOS	65 nm CMOS	65 nm CMOS

$FoM = -PN + 20\log(f_0/\Delta f) - 10\log(P_{DC}/1mW)$

* Normalized from PN at 1 MHz offset

** Area including pads

† Corresponds to the boundary between current and voltage limited regime

lower PN assuming tank loss is dominated by the inductor. Specifically, the factor $1/Q^2$ contributes 2.92 dB, and the remaining improvement is due to the increased output swing, since $V_{RF} = I_{RF} \cdot R_P$ where R_P is the parallel tank resistance approximated by 2π fLQ. Subsequently, at 10-MHz offset, the VCO with DL-PFS inductor achieves a maximum FoM of 189.2 dBc/Hz at 2.12 mW, while the maximum FoM of the VCO with SL-PFS decays to 186.2 dBc/Hz at the increased P_{DC} of 2.93 mW, as Fig. 10 illustrates. Besides that, flicker noise caused by Groszkowski's effect, which is the imbalanced condition in tank reactive energy is also minimized, since a shift in low frequency $\Delta f \pm f_o$ caused by higher current n th harmonics flowing into capacitive path will be restored to f_o, as higher inductor Q has a stronger tendency to counteract the imbalance in tank reactive energy, where Groszkowski's effect is defined as [7]

$$\frac{\Delta f}{f_o} = -\frac{1}{Q^2}\sum_{n=2}^{\infty}\frac{n^2}{n^2-1}\cdot\left(\frac{I_{fn}}{I_{fo}}\right)^2 \quad (2)$$

With the maximum FoM achieved through the biasing of the VCO, at the boundary between the voltage- and current-limited regime, the 27.6% reduction in P_{DC} to obtain that maximum also proves that R_P and thus the inductor Q of the VCO with DL-PFS inductor are $\sim 1.38\times$ larger than those of the VCO with SL-PFS, which is close to the EM simulation results (1.4×). Figure 11 presents the measured FoM at 10 MHz offset and the output power across the frequency tuning range. The variation of FoM and output power is less than 0.6 dBc/Hz and 1 dB, respectively.

Benchmarking with a VCO containing a SL-PFS inductor (Table 1), shows that the VCO with the proposed DL-PFS inductor achieves a 3 dB improvement of the maximum FoM. Likewise, our VCO with the proposed DL-PFS inductor also reaches the highest FoM when compared with the recently reported low-power VCOs in Table 2.

4 Conclusion

This letter reported a DL-PFS technique to reduce the substrate loss of the on-chip spiral inductor by optimally utilizing two of the lowest metal strips. DL-PFS achieved a 40% Q factor improvement when compared with the conventional SL-PFS. The inductor with DL-PFS applied in a class-B VCO and fabricated in 0.13 μm CMOS, achieves a 3-dB improvement of the maximum FoM and reduces power consumption by 27.6%. The measured PN is 132.5 dBc/Hz at 10 MHz offset with a 10 GHz carrier while dissipating 2.12 mW. The resulting FoM compares favorably with the state-of-the-art.

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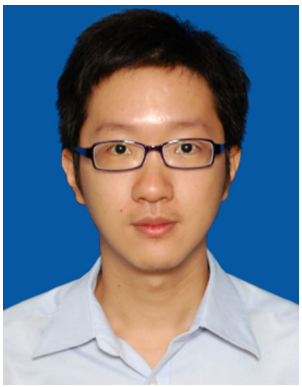

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