

A Single-Chip Solar Energy Harvesting IC Using Integrated Photodiodes for Biomedical Implant Applications

Zhiyuan Chen, Man-Kay Law, *Senior Member, IEEE*, Pui-In Mak, *Senior Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

Abstract—In this paper, an ultra-compact single-chip solar energy harvesting IC using on-chip solar cell for biomedical implant applications is presented. By employing an on-chip charge pump with parallel connected photodiodes, a $3.5\times$ efficiency improvement can be achieved when compared with the conventional stacked photodiode approach to boost the harvested voltage while preserving a single-chip solution. A photodiode-assisted dual startup circuit (PDSC) is also proposed to improve the area efficiency and increase the startup speed by 77%. By employing an auxiliary charge pump (AQP) using zero threshold voltage (ZVT) devices in parallel with the main charge pump, a low startup voltage of 0.25 V is obtained while minimizing the reversion loss. A $4 V_{in}$ gate drive voltage is utilized to reduce the conduction loss. Systematic charge pump and solar cell area optimization is also introduced to improve the energy harvesting efficiency. The proposed system is implemented in a standard $0.18\text{-}\mu\text{m}$ CMOS technology and occupies an active area of 1.54 mm^2 . Measurement results show that the on-chip charge pump can achieve a maximum efficiency of 67%. With an incident power of 1.22 mW/cm^2 from a halogen light source, the proposed energy harvesting IC can deliver an output power of $1.65\text{ }\mu\text{W}$ at 64% charge pump efficiency. The chip prototype is also verified using *in-vitro* experiment.

Index Terms—Auxiliary charge pump, charge pump/solar cell area optimization, photodiode-assisted dual startup circuit, single-chip solar energy harvesting.

I. INTRODUCTION

THE emerging eHealthcare system is patient-driven, where patients can continuously monitor their own health status even at home. Their physiological data, such as breathing, electrocardiogram (ECG), heart beat, glucose level and so on, can be sent back to dedicated medical data servers wirelessly

for further analysis. Existing research on implantable/wearable systems include retinal prosthesis [1], intraocular pressure monitoring [2], wearable ECG [3], and many others. In order to achieve minimal invasiveness for implantable devices, such systems should be miniaturized as much as possible, leading to a stringent size and energy bottleneck. As a result, energy harvesting becomes a favorable alternative to achieve system autonomy or even battery replacement in various implantable systems.

Solar energy harvesting has been recently demonstrated as a viable solution in applications including intraocular pressure monitoring [2] and subdermal implant applications [4]. In [5] and [6], the feasibility of powering CMOS circuitry using different types of photodiodes built on the substrate in standard CMOS is demonstrated. By integrating the CMOS circuitry and solar energy harvester on the same chip, the associated difficulty during the system assembly can be much relaxed, improving the system reliability and reducing the cost. However, the low voltage generated by integrated photodiodes (typically ranging from 0.3 V to 0.5 V) can result in significant circuit performance degradation. Even though a complete sensor read-out circuit directly powered by on-chip solar cells in the same substrate is demonstrated in [4], the achieved sensing accuracy is limited. Various attempts to passively boost the voltage generated by integrated photodiodes have been reported. In [7], the property of Silicon-on-Insulator (SOI) is exploited to serially connect photodiodes with separate substrates, but with the tradeoff of increased cost. In [8] and [9], different approaches to stack photodiodes in a standard CMOS process are studied. Nevertheless, due to the single substrate limitation, the total photosensitive area cannot be optimized, sacrificing the overall energy harvesting efficiency.

Instead of passively stacking integrated photodiodes, a more efficient approach is to employ DC-DC converters to boost the low voltage generated. Even though an inductor-based boost converter solution can be employed to boost up the voltage harvested by on-chip solar cells as demonstrated in [10], the requirement for large off-chip components can jeopardize its applicability in implantable applications. To solve this problem, charge pumps using integrated capacitors while preserving ultra-low voltage operations can be employed. In [11], a solar energy harvesting charge pump with a startup voltage of 0.27 V is introduced. However, the ZVT switches and the non-uniform gate drive voltages can lead to increased reversion

Manuscript received November 26, 2015; revised February 12, 2016 and April 8, 2016; accepted April 8, 2016. Date of publication August 1, 2016; date of current version January 26, 2017. This work was supported by the Macau Science and Technology Development Fund (FDCT) under Project 015/2012/A1, and the Research Committee of University of Macau (MYRG100-FST13-LMK). This paper was recommended by Associate Editor M. Sahin.

Z. Chen and P.-I. Mak are with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China.

M.-K. Law is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China (e-mail: mklaw@umac.mo).

R. P. Martins is with the State Key Lab of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China, on leave from Instituto Superior Técnico/Universidade de Lisboa, 1049-001 Lisboa, Portugal.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TBCAS.2016.2553152

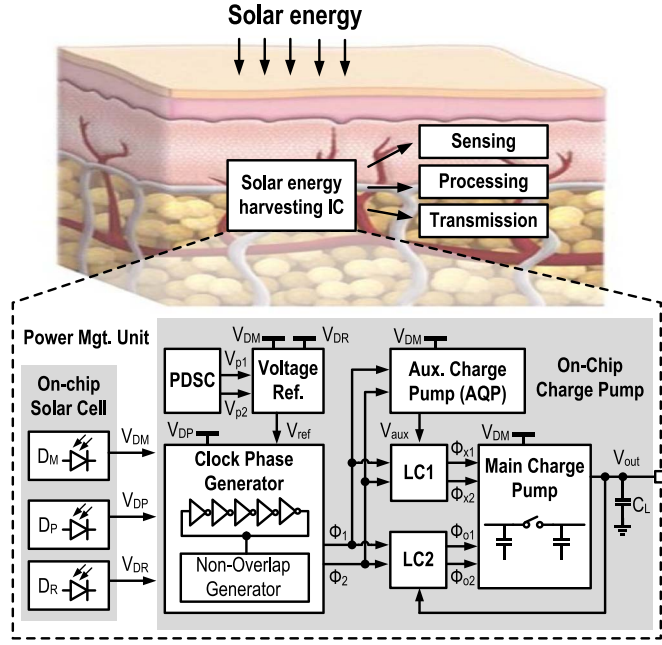


Fig. 1. System overview of the proposed single chip solar energy harvesting system in subdermal implant applications.

and conduction losses, sacrificing the efficiency. In [12], an ultra-low input voltage energy harvesting charge pump that can operate down to 0.15 V using dynamic body biasing is proposed. But it requires 6 off-chip capacitors that can lead to significant packaging complexity and overhead. In [13], a complete die-stacked sensing platform using integrated solar energy harvesting is reported. Nevertheless, the feasibility and co-optimization of a single-chip solar energy harvesting solution, that can boost the harvested voltage while achieving a high efficiency suitable for implantable applications, is yet to be demonstrated.

In this paper, we propose a single-chip solar energy harvesting system using a 3-stage integrated charge pump with on-chip photodiodes. An output power in the μW level is targeted for subdermal implant applications, where the key challenge is to achieve high energy efficiency at ultra-low power levels and in a small volume [14]. By preserving a single-chip solution, a complete highly efficient energy harvesting system with a high output voltage as well as an ultra-compact form factor can be accomplished while fulfilling the system dynamic range requirement [15].

II. SYSTEM ARCHITECTURE

Fig. 1 shows the application scenario of a typical subdermal implant, which is responsible for harvesting the incoming solar energy, retrieving the physiological data from miniaturized sensors, processing the collected data and transmitting the acquired information wirelessly. This work focuses on the power management unit, where on-chip charge pump and integrated photodiodes are utilized to provide an ultra-compact highly efficient energy harvesting solution.

The proposed single-chip solar energy harvesting system is comprised of an on-chip solar cell, a voltage reference with a

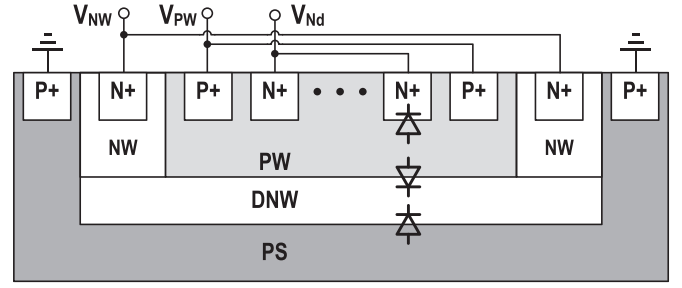


Fig. 2. Illustrative diagram showing the PN junctions available in a standard triple-well CMOS process.

TABLE I
MEASURED PHOTODIODE PERFORMANCE WITH PARALLEL AND STACK CONNECTIONS UNDER AN INCIDENT POWER OF 1.13 mW/mm² FROM A HALOGEN LIGHT SOURCE

Parameter	Diode Type			Connection	
	N+/PW	PW/DNW	DNW/PS	Parallel	Stacked
I_{sc} (pA/ μm^2)	74.3	69.6	433	577	74.7
V_{oc} (V)	0.55	0.527	0.526	0.53	1.05
Max. Eff. (%)	2.8	2.6	16.7	21.9	5.9

I_{sc} : Short-Circuit Current V_{oc} : Open-Circuit Voltage

photodiode-assisted dual startup circuit (PDSC), a clock phase generator, an auxiliary charge pump (AQP), two level converters (LCs) and a main charge pump. The solar cell harvests the incoming solar energy and provides power to the other building blocks as well as to the load. To prevent noise coupling between modules, the solar cell is divided into three sub-blocks D_M , D_P , and D_R to provide energy to the main/auxiliary charge pump, clock phase generator and voltage reference, respectively. The voltage reference generates a reference voltage V_{ref} for biasing the clock phase generator. PDSC is proposed to improve the voltage reference startup time while imposing minimum overhead. The clock phase generator provides a two-phase non-overlapping clock Φ_1 and Φ_2 to the AQP and LCs using a 5-stage ring oscillator with body-biasing optimized for on-chip solar energy harvesting. Instead of implementing the main charge pump with zero threshold devices as in [11], an AQP is utilized to generate an auxiliary supply voltage V_{aux} to LC1 to ensure a low startup voltage while minimizing the reversion loss. High swing clock phases Φ_{x1}/Φ_{x2} and Φ_{o1}/Φ_{o2} are utilized for improved conduction loss in the main charge pump. Descriptions of individual building blocks are outlined as follows.

A. On-Chip Photodiode

Fig. 2 shows the PN junctions available for serving as on-chip photodiodes in a standard triple-well CMOS process, including: (i) N+/PW; (ii) PW/DNW; and (iii) DNW/PS. In order to characterize the photodiode performance using the selected 0.18- μm CMOS process, test structures are fabricated and measured under direct illumination using a halogen light source with an incident power of 1.13 mW/mm². The corresponding measurement results are shown in Table I. It can be observed

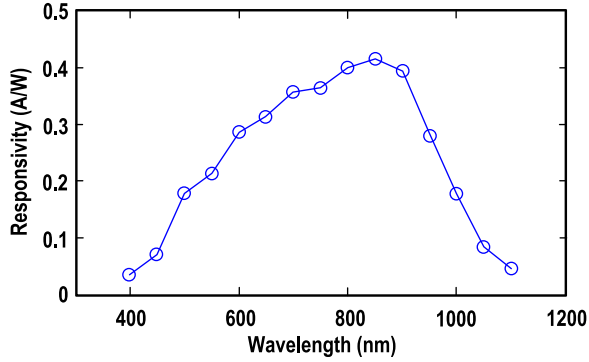


Fig. 3. Measured responsivity of the proposed parallel photodiode configuration.

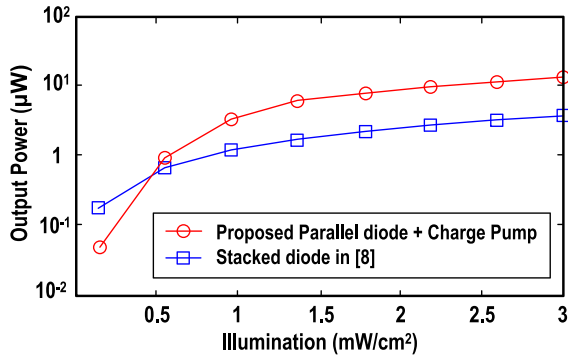


Fig. 4. Simulation results showing the achieved output power of the proposed photodiode with charge pump and the stacked photodiode approach in [8] under the same area budget.

that the normalized short-circuit current density from DNW/PS is almost 6 times larger than that obtained from N+/PW and PW/NW, which is consistent with [9]. As a consequence, unlike [4] that shorts DNW/PS for generating a positive output voltage, the DNW/PS photodiode is utilized to improve the energy harvesting efficiency at the expense of an extra inversion stage. Apart from that, the harvested low voltage should be further boosted for system use. Even though passive stacking on photodiodes as in [8] (by shorting the PW/DNW photodiode) can be employed to increase the output voltage, the incurred efficiency loss due to the shorting of PW/DNW and the mismatch between N+/PW and DNW/PS can be significant as shown in Table I. To address the above issues while improving the energy harvesting efficiency and maintaining a compact solution, we propose to utilize all the available on-chip photodiodes through parallel connections and subsequently boost the harvested voltage using an on-chip charge pump built on the same substrate.

Fig. 3 shows the measured responsivity of the proposed parallel photodiode configuration. The maximum responsivity is achieved at a wavelength of 850 nm. Fig. 4 shows the simulated results of the proposed parallel photodiode together with our designed on-chip charge pump as well as the solar energy harvesting system using stacked photodiodes from [8] with the same technology and active area of 1.54 mm². The incident power is expected to be within 3 mW/cm² for harvesting power in the order of few μW. It can be observed that almost 3.5× more output power can be extracted using our proposed ap-

proach with an incident power of approximately 1.22 mW/cm². The loss in efficiency at very low illumination levels is mainly due to the overhead of the on-chip charge pump as expected.

B. Voltage Reference

The voltage reference serves as an important module to generate the required biasing and wake up the entire system. As the open-circuit voltage generated by on-chip photodiodes is small, the voltage reference should be designed to operate at a low supply voltage. In this work, we implemented the voltage reference based on [16], which can achieve ultra-low voltage/power operation and is therefore suitable to be powered using on-chip photodiodes with nA power consumption. However, the slow startup problem due to the use of a conventional startup circuit under a low supply voltage still remains unresolved. Apart from that, the large energy surge during the startup period can lead to system instability or even startup failure for the proposed system where the available energy can be limited. To resolve the above issues, PDSC is proposed to ensure a robust startup process with minimal overhead while improving the startup time.

Fig. 5(b) shows the proposed voltage reference with PDSC. The voltage reference operation can be found in [16]. The PDSC is composed of a light induced startup signal V_R , and two photodelay generators (PDG_{1,2}) for controlling M_{st1} and M_{st2} , respectively. The schematic of the PDG is shown in Fig. 5(a). To improve the startup time, locally self-stacked photodiodes are utilized to generate a local high voltage to reduce the switch on-resistance for improved startup speed while imposing minimal overhead. The capacitor C_x is utilized to generate different delays from the two PDGs during the startup sequence. V_R is employed to discharge C_x of the two PDGs to prevent possible startup failure during a fast incident power transient. As mentioned before, the startup circuit consumes a transient power which can be much larger than the nominal power consumption of the voltage reference during the startup period. This can limit the startup speed or even lead to startup failure. Instead of increasing the size of D_R to cater for the extra energy required during system startup, PDG₂ is employed to temporarily connect D_R and D_M to support the extra energy required during the startup process, improving the system area efficiency.

Fig. 5(c) shows the illustrative timing diagram of a typical startup sequence. In the beginning of the startup period, the incoming solar energy triggers V_R , and two pulses V_{p1} and V_{p2} with different pulse widths are generated by PDG_{1,2}, respectively. D_M is connected to D_R through M_{st2} to provide the extra startup energy, and is disconnected at the end of V_{p2} . Fig. 6(a) shows the transient simulation results of the voltage reference using the conventional startup as in [16] and our proposed PDSC with an incident power of 1.22 mW/cm², and the startup time comparison is shown in Fig. 6(b). It can be concluded that a startup time improvement by 77% with an incident power of 1.22 mW/cm² can be achieved. Notice that the peaking of V_{ref} , which is contributed by the large shoot-through current during the startup process, can be alleviated by optimizing the sizing of M_{st1} while ensuring robust startup operation under process variations.

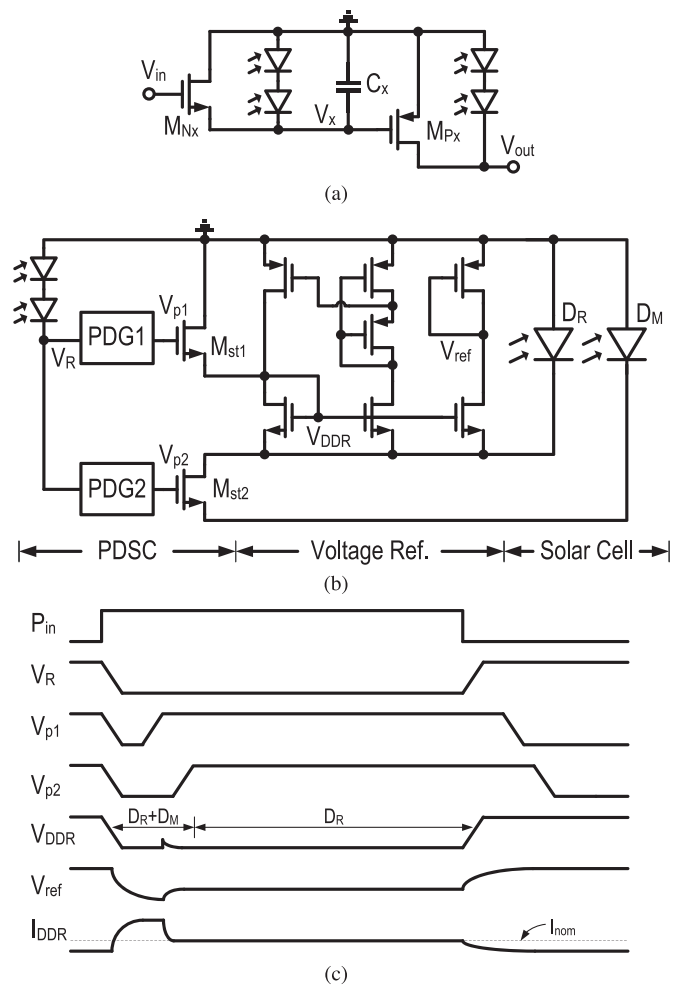


Fig. 5. Simplified schematic showing (a) the photo-delay generator (PDG), (b) the proposed voltage reference with PDSC, and (c) the corresponding timing diagram.

C. Clock Phase Generator

The on-chip charge pump should operate at a frequency in the order of MHz to reduce the output impedance as a result of the limited size of the flying capacitors. Nevertheless, due to the low voltage generated by the on-chip solar cell, the operating frequency of the ring oscillator and the non-overlap clock generator can be sacrificed. As a result, forward biasing both the PMOS and NMOS body [17] is utilized to increase the operating frequency. Fig. 7 shows the simulated efficiency of the on-chip energy harvesting charge pump both with and without body biasing at different illumination levels. It can be observed that body biasing can significantly increase in efficiency by up to 5% at low light conditions, while resulting in only an approximate 0.5% efficiency reduction at high illumination levels due to parasitic loss.

D. On-Chip Charge Pump

Conventionally, bootstrapping and ZVT switches are utilized for solar energy harvesting applications due to the low input voltage V_{in} . This will inevitably lead to significant reversion

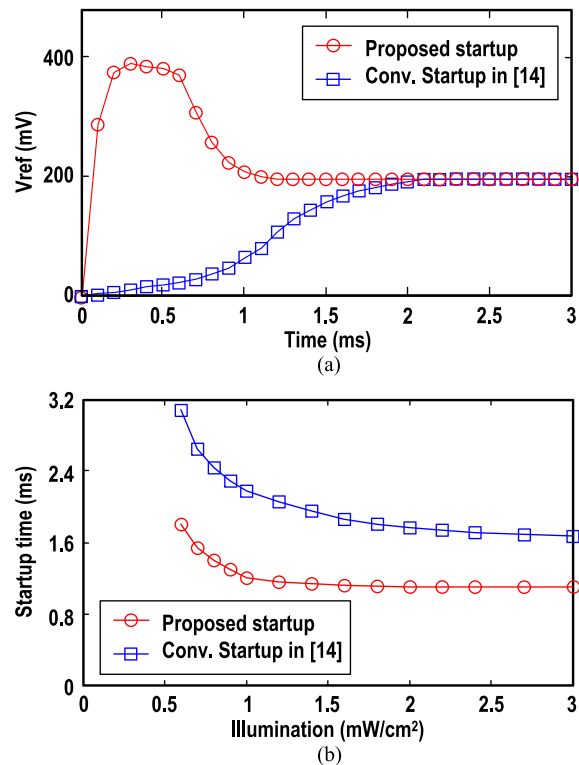


Fig. 6. Simulation results of the voltage reference showing (a) the transient waveform of the proposed PDSC and the conventional startup in [16] at an incident power of 1.22 mW/cm^2 , and (b) the startup time comparison under different illumination levels.

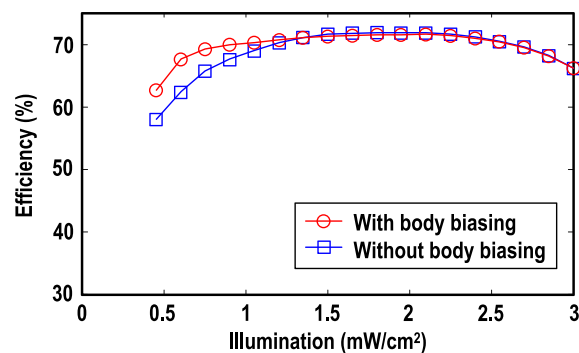


Fig. 7. Simulation results of the proposed charge pump with and without using body biasing for the clock phase generator.

loss due to the increased leakage as in [11], sacrificing the overall efficiency. The non-uniform gate drive voltages in [11] can also increase the conduction loss. Fig. 8(a) and (b) shows the simplified schematics of the proposed auxiliary and main charge pump based on the linear charge pump topology, respectively. In order to minimize the reversion loss while maintaining a low startup voltage, ZVT switches [shown as shaded in Fig. 8(a)] are only utilized in the AQP. The AQP, which is preceded by an inversion stage and followed by two boosting stages, generates an output voltage V_{aux} at $3V_{in}$ to obtain a pair of high swing clock $\Phi_{x1,2}$ through LC1 for controlling the cold start switches in the main charge pump, to charge up V_{out} . V_{out} is then utilized to power up LC2 to generate $\Phi_{o1,2}$ for driving

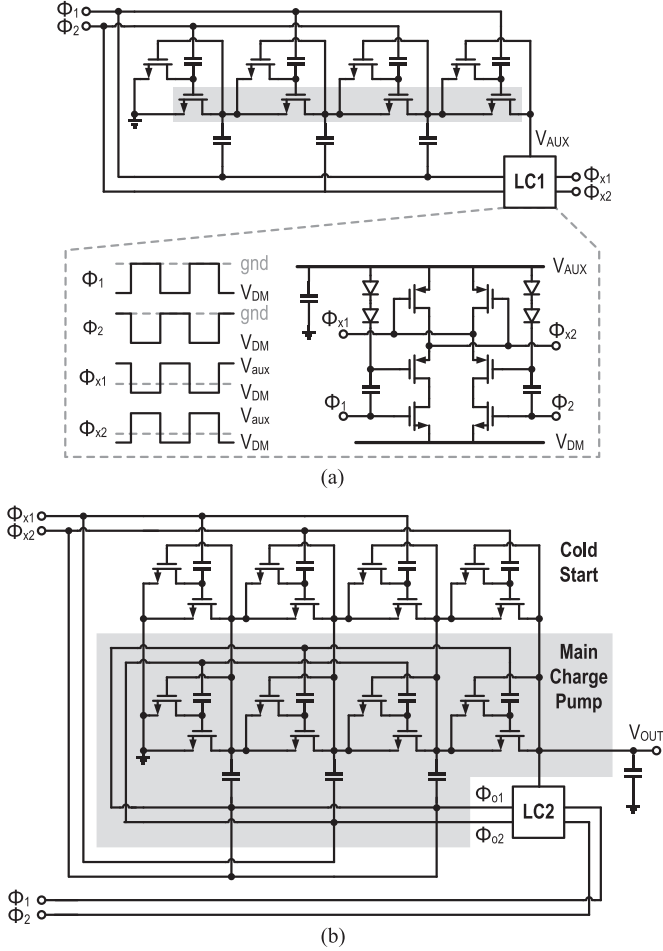


Fig. 8. Simplified schematic showing the (a) AQP and LC, and (b) main charge pump with cold start switches in parallel.

the main switches and work cooperatively with $\Phi_{x1,2}$ in the steady state to further improve the efficiency. The main charge pump switches are controlled with a $4V_{in}$ gate drive voltage to reduce the conduction loss. The structure of LC1 (LC2 is similar) is shown in Fig. 8(a). To balance the pull up/down speed of the LC, the turn on voltage of the pull up PMOS is buffered by a 50 fF capacitor. Notice that the AQP is also turned on during normal operations to improve the heavy load efficiency.

III. SYSTEM ANALYSIS AND OPTIMIZATION

To maximize the energy harvesting efficiency of the on-chip solar cell, all the available photodiodes are utilized and connected in parallel, as discussed in Section II-A. A 3-stage linear charge pump (one inversion stage + two boosting stages) is utilized to convert the negative voltage into a high output voltage.

A. Switching Loss Optimization

For a N -stage linear charge pump within an input voltage V_{in} (i.e., the harvested voltage from on-chip photodiodes in the

proposed system), the corresponding output voltage V_{out} can be approximated as

$$V_{out} = N \left(V_{in} \frac{C_{fly}}{C_{fly} + C_P} - R_{eq,on} I_{out} \right) \quad (1)$$

where C_{fly} is the flying capacitance, C_P is the parasitic capacitance, $R_{eq,on}$ is the equivalent switch on-resistance, and I_{out} is the load, respectively. The equivalent on-resistance of a switch can be approximated as [18]

$$R_{eq,on} = \sqrt{\sum R_{on}^2 + \frac{1}{f C_{fly}}^2} \quad (2)$$

where R_{on} is the on-resistance of a switch and f is the frequency. To achieve a high charge pump efficiency, $R_{eq,on}$ should be much smaller than R_L to minimize conduction loss, where R_L is the equivalent load resistance. For a micro-power charge pump, the reversion loss, which is characterized by the switch off-resistance R_{off} , can become significant and hence cannot be neglected. As a result, both the switch on- and off-resistance should be optimized, leading to

$$R_{off} \gg R_L \gg R_{eq,on}. \quad (3)$$

From [19], when the drain-source voltage V_{ds} is much smaller than the overdrive voltage $V_{gs} - V_{th}$, where V_{gs} is the gate-source voltage and V_{th} is its threshold voltage, respectively. R_{on} can be expressed as

$$R_{on} = \frac{1}{\mu C_{ox} \left(\frac{W}{L} \right) (V_{gs} - V_{th})} \quad (4)$$

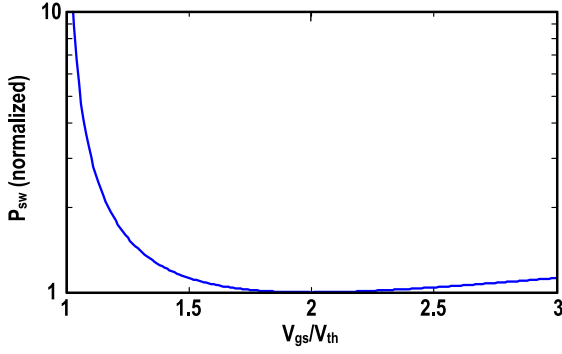
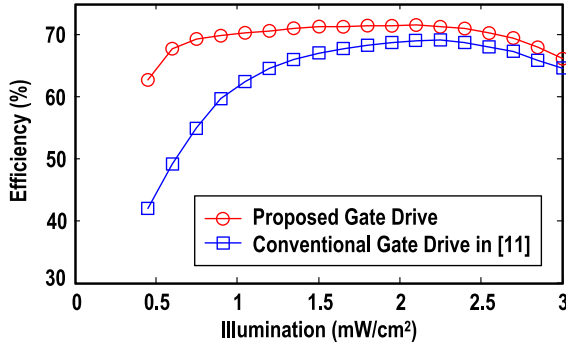
μ is the electron mobility, C_{ox} is the unit oxide capacitance and W/L is the aspect ratio. Similarly, when V_{ds} is much larger than $4V_T$ (V_T is the thermal voltage) when the switch is turned off, R_{off} can be expressed as

$$R_{off} = \frac{V_{ds}}{S e \frac{V_{gs} - V_{th}}{m V_T}} \quad (5)$$

where S is a proportional factor. From (4) and (5), it can be observed that a lower V_{th} reduces R_{off} more rapidly than R_{on} . As a result, the charge pump efficiency is sacrificed especially when R_L is large, rendering the use of low V_{th} devices or body biasing technique [17] as the charge pump switches unsuitable. Even though the switching body biasing technique [12] can extend the ratio between R_{on} and R_{off} , the increase in design overhead under a variable input condition for micro-power energy harvesting applications can be undesirable. Comparatively, a better solution should be to increase the switch driving voltage V_{gs} .

To determine the optimal switch driving voltage V_{gs} , we first determine the associated switching power loss (P_{sw}) of a charge pump, expressed as

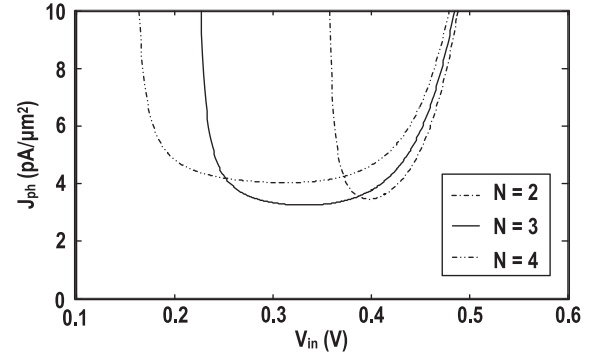
$$P_{sw} = \frac{N}{2} f C_0 \sum W_i L_i V_{gs,i}^2 \quad (6)$$

Fig. 9. Normalized switching loss P_{sw} versus different V_{gs}/V_{th} ratios.Fig. 10. Simulation results showing the efficiency of the proposed $4V_{in}$ gate drive and the conventional approach in [11].

where n is the number of stage for the charge pump, f is the switching frequency, C_0 is the gate capacitance per unit area, and W_i , L_i and $V_{gs,i}$ are the switch width, switch length and gate driving voltage of the i -th switch, respectively. Due to the limited C_{fly} , a high switching frequency f is required to suppress the series loss. This will inevitably increase the gate switching loss P_{sw} which can be significant for micro-power energy harvesting. As shown in (4) and (5), R_{on} varies significantly when V_{gs} is close to V_{th} . As a result, an increase in switch driving voltage V_{gs} should be ensured instead of enlarging the switch width W when the input voltage is low. From (4) and (6), it can be observed that an increase in V_{gs} can reduce the loss through R_{on} while increasing P_{sw} . By substituting (4) into (6), the optimal V_{gs} can be deduced as

$$V_{gs} = 2V_{th}. \quad (7)$$

Fig. 9 shows the charge pump efficiency with respect to different ratios of V_{gs}/V_{th} in a standard $0.18 \mu\text{m}$ CMOS process. It can be observed that the minimum normalized P_{sw} is achieved when $V_{gs} \sim 2V_{th}$ as expected. With a V_{th} of approximately 0.49 V (without body effect) and an expected worst case photodiode voltage of roughly 0.3 V , V_{gs} is therefore designed to be $4V_{in}$. Fig. 10 shows the simulated efficiency by using the proposed AQP with the proposed $4V_{in}$ gate drive and the one in [11] using the same area budget. It can be observed that our proposed scheme can achieve better efficiency over the targeted illumination power levels.

Fig. 11. Optimization of the photocurrent density versus photodiode voltage V_{in} using numerical method.

B. Solar Cell Area Optimization

To optimize the area of the proposed single-chip solar energy harvesting system, both the solar cell and the charge pump should be considered. As stated in [11], the charge pump current consumption I_{cp} can be expressed as

$$I_{cp} = I_{out} \left(N + \alpha \frac{N^2 V_{in}}{N V_{in} - V_{out}} \right) \quad (8)$$

where α is the ratio between the bottom plate parasitic and the nominal capacitance of the on-chip capacitor. The on-chip photodiode should be able to provide this charge pump current together with its intrinsic loss, and can be defined as

$$I_{ph} = I_S e^{\frac{V_{in}}{\eta V_T}} + I_{cp} \quad (9)$$

where η and I_S are the non-ideality factor and the saturation current of the on-chip photodiode, respectively. To minimize the area of the on-chip solar cell, the photocurrent density J_{ph} for driving a particular charge pump load I_{out} should be minimized. The total capacitance C_{total} for a N -stage linear charge pump can be expressed as

$$C_{total} = \frac{I_{out}}{f} \frac{N^2}{N V_{in} - V_{out}}. \quad (10)$$

For a total chip area A_{total} , the photocurrent is defined as

$$I_{ph} = \left(A_{total} - \frac{C_{total}}{C_0} \right) J_{ph} \quad (11)$$

where C_0 is the capacitance per unit area of the on-chip capacitor. By using (8)–(11), the optimized J_{ph} under different N and V_{in} can be obtained numerically, as shown in Fig. 11. It can be observed that the minimum J_{ph} of $3.3 \text{ pA}/\mu\text{m}^2$ can be achieved with $N = 3$. The optimized C_{total} can be deduced to be approximately 15% of A_{total} .

IV. MEASUREMENT RESULTS

The complete single-chip solar energy harvesting system is designed and fabricated in a standard $0.18\text{-}\mu\text{m}$ CMOS process. Fig. 12 shows the corresponding chip micrograph with key building blocks indicated. The on-chip photodiode, main flying capacitors, auxiliary flying capacitors and voltage reference

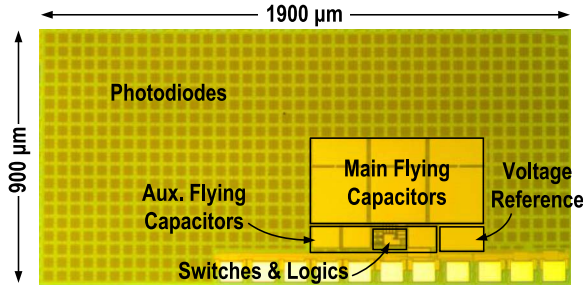


Fig. 12. Chip micrograph of the proposed single-chip solar energy harvesting IC with test pads for verifications only.

TABLE II
POWER DISTRIBUTION OF THE PROPOSED SYSTEM
WITH AN INCIDENT POWER OF 1.22 mW/cm²

	Simulated	Measured
Power Harvested	2.6 μ W	2.58 μ W
Power Consumed		
Ring Oscillator	3.3 nW	523 nW
Clock Phase generator	38.2 nW	
Voltage reference	0.9 nW	
Level converters	439 nW	
Power Delivered	1.8 μ W	1.65 μ W

occupy 1.3, 0.2, 0.04, and 0.02 mm², respectively. The total area is 1.54 mm² (excluding test pads which are utilized for verifications of different building blocks only). The charge pump to solar cell area ratio is approximately 18%, which is kept to be close to the value deduced in Section III-B. Storage capacitors are constructed underneath the flying (MIM) capacitors to save area. Circuits are shielded from incoming light using metal shielding on top.

The chip prototype is characterized with the halogen light source (Newport model no. 66885) using a light guide. The incident power is measured using the Newport Power Meter model 2936-C. Table II summarizes the simulated and measured power of the chip prototype under an incident power of 1.22 mW/cm². The harvested power is measured by using equivalent loads under the same illumination condition. The difference between the simulated and measured results is mainly due to process variations as verified by the corner models provided by the foundry. With a harvested power of 2.58 μ W, a measured output power of 1.65 μ W can be achieved. Fig. 13 shows the measured efficiency with respect to I_{out} under different illuminations (from 0.6 to 2.43 mW/cm²). The on-chip clock frequency is fixed at 800 kHz. It can be seen that the proposed system achieves a maximum efficiency of 67% at $P_{in} = 0.6$ mW/cm², which is close to the simulated value. At higher illumination levels, the maximum efficiency slightly drops as a result of the reduction in the photodiode efficiency due to increased chip temperature during the measurement. Fig. 14 shows the measured transient waveform of the charge pump start up sequence with a loading of 10 M Ω (oscilloscope probe loading). The auxiliary charge pump controls the cold start switches to charge the loading capacitor when incoming light power is available. When V_{out} exceeds the predefined threshold, the main charge pump starts to operate. The voltage

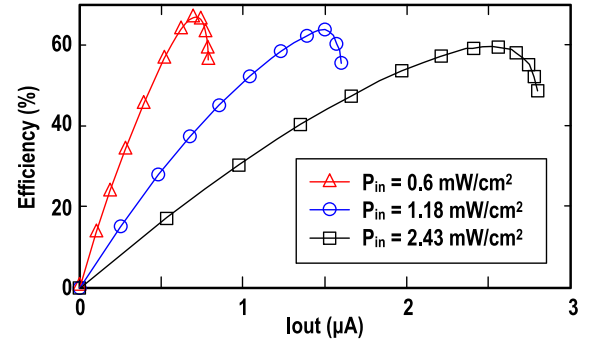


Fig. 13. Measured efficiency under different incident power levels.

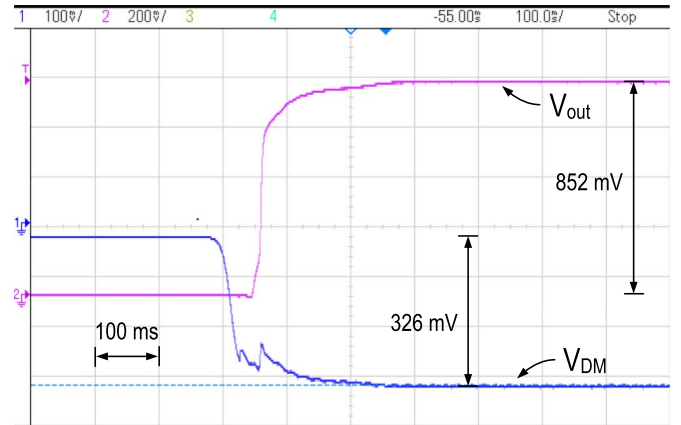


Fig. 14. Measured system startup waveform with an incident power of 0.6 mW/cm².

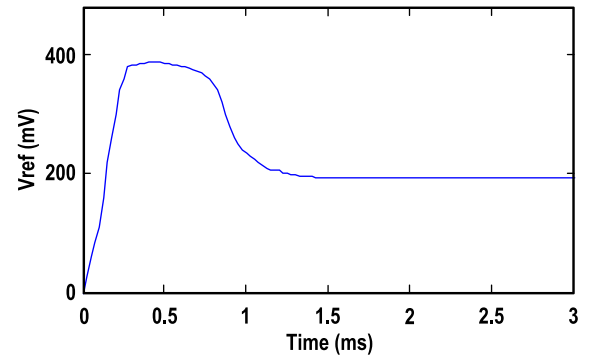


Fig. 15. Measured V_{ref} during startup with an incident power of 1.22 mW/cm².

droop at V_{DM} is due to the disconnection between D_R and D_M during the PDSC operation. An output voltage of 852 mV is achieved when the photodiode voltage V_{DM} is 326 mV. Fig. 15 shows the measured V_{ref} during the system startup with an incident power of 1.22 mW/cm², and the result is consistent with the simulated one. Fig. 16 shows the test setup for *in-vitro* system verification. A piece of pork skin with fat and muscle (1 mm + 2 mm + 1.5 mm) is utilized to mimic the situation for subdermal implant applications. It can be concluded that the proposed energy harvesting IC can successfully harvest the incoming solar energy. With an output power close to 1.6 μ W, the measured source power is roughly 110 mW/cm², corresponding to an incident power loss of approximately 20 dB.

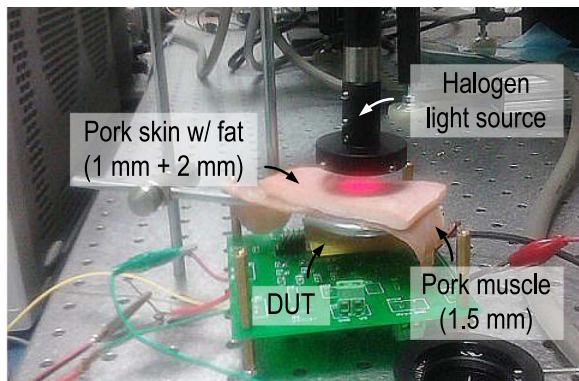


Fig. 16. *In-vitro* measurement setup using a pork skin + fat + muscle (1 mm + 2 mm + 1.5 mm).

TABLE III
PERFORMANCE COMPARISON WITH EXISTING INTEGRATED CHARGE PUMPS FOR ENERGY HARVESTING

	JSSC'13 [13]	TCAS-IP'11 [11]	JSSC'15 [12]	This work
Process (μm)	0.18	0.13	0.13	0.18
Charge pump area (mm^2)	0.95	0.42	0.066	0.24
Capacitors	On-chip	On-chip	Off-chip	On-chip
Solar cell	External 1.62 mm^2	External 1.21 mm^2	–	Integrated 1.3mm^2
Extra pads and packaging cost	Yes	Yes	Yes	No
No. of stages	6	3	3	3*
freq. (kHz)	335	800	250	800
Gate Drive	$3V_{in}$	$2 \sim 3V_{in}$	$2 \sim 3V_{in}$	$4V_{in}$
Min. V_{in} (V)	–	0.27	0.15	0.25
Max. Eff. (%) @ V_{in} (V)	26.9 [^]	61@0.35 ^{†‡}	62@0.3 ^{†‡}	67@0.31[§]

* One inversion + two boosting stages

[^] Overall energy harvesting efficiency

[†] Extracted from the corresponding literature

[‡] Without regulation

[§] Corresponding to $P_{in} = 0.6$ mW/cm²

Table III compares the performance of our work with state-of-the-art energy harvesting systems using on-chip charge pumps. Our work realizes a single-chip solar energy harvesting solution without the overhead of extra pads and packaging cost. The on-chip charge pump achieves the highest efficiency of 67% at low incident power levels (with an input voltage close to 0.3 V) which is expected in subdermal implant applications. Even though [12] can achieve a low input voltage down to 0.15 V, the requirement of 6 off-chip capacitors can induce significant overhead both in size and cost. The proposed PDSC also enables a fast voltage reference startup time of 1.4 ms with an incident power of 1.22 mW/cm², corresponding to a 77% improvement when compared to the conventional startup circuit. Table IV summarizes the performance comparison with existing single-chip solar energy harvesting solutions. It can be observed that our work results in the highest energy harvesting efficiency ($\sim 3.5\times$ improvement when compared with [8])

TABLE IV
PERFORMANCE COMPARISON WITH EXISTING SINGLE-CHIP SOLAR ENERGY HARVESTING SOLUTIONS

	TED'12 [8]	TVLSI'11 [6]	This work
Process (μm)	0.35	0.35	0.18
Light source	White LED	Green laser (532 nm)	Halogen lamp
Incident light intensity	31 klx	34.2 μW	1.13 mW/mm ²
Area	0.69* mm^2 1.38 [^] mm^2	338 μm^2	1.3 + 0.24 mm^2
V_{oc} (V)	0.52*	0.533	0.53
I_{sc} (μA)	17.5*	680	750
P_{out} (μW)	7.14*	225	322
Eff. (%)	9.5* [‡]	24	21.9*
Voltage boosting	Stacked	–	On-chip charge pump
$V_{out,boosted}$ (V)	0.97 ^{^†}	–	1.08[§]
$Eff_{boosted}$ (%)	3.5 [^]	–	12.1[§]

* Single photodiode configuration only

[^] Two-photodiode stacked configuration

[†] Estimated using the open-circuit voltage

[‡] Extracted using a luminous efficacy of 285 lm/W

[§] Corresponding to $P_{in} = 1.22$ mW/cm²

while generating a boosted output voltage for system use. Simulation result shows that close-loop regulation using pulse skipping modulation similar to [11] can be achieved with a controller power overhead of 69.7 nW. The ultra-compact form factor and high efficiency at a low input voltage demonstrates that our proposed system is especially suitable for subdermal implant applications.

V. CONCLUSION

In this paper, an ultra-compact single-chip solar energy harvesting IC using on-chip photodiodes is introduced. The proposed system employs an on-chip charge pump to extract energy from an integrated photodiode and to generate a high output voltage while preserving a single substrate solution. Based on the photodiode measurement results, the proposed system achieves a $3.5\times$ improvement in energy harvesting efficiency when compared to the conventional stacked photodiode for boosting the harvested voltage with no external components. The proposed PDSC achieves a 77% startup speed improvement when compared with the conventional startup circuit. The charge pump reversion and conduction loss are improved by employing an auxiliary charge pump (AQP) and a $4V_{in}$ gate drive voltage, respectively. Systematic charge pump and solar cell area optimization is also introduced to improve the energy harvesting efficiency. Our proposed solar energy harvesting system achieves high efficiency without extra pads and packaging cost, making it suitable for low-cost ultra-compact robust subdermal implant applications. The future work includes the development of a reconfigurable charge pump with close loop maximum power point tracking (MPPT) capability.

REFERENCES

- [1] M. Monge, M. Raj, M. H. Nazari, H. C. Chang, Y. Zhao, J. D. Weiland, M. S. Humayun, Y. C. Tai, and A. Emami, "A fully intraocular high-density self-calibrating epiretinal prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 747–760, Dec. 2013.
- [2] G. Chen, H. Ghaed, R. Haque, M. Wiecekowski, Y. Kim, G. Kim, D. Fick, D. Kim, M. Seok, K. Wise, D. Blaauw, and D. Sylvester, "A cubic-millimeter energy-autonomous wireless intraocular pressure monitor," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 310–312.
- [3] Z. Zhang and Y. Lian, "A 300-mV 220-nW event-driven ADC with real-time QRS detection for wearable ECG sensors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 6, pp. 834–843, Dec. 2014.
- [4] S. Ayazian, V. A. Akhavan, E. Soenen, and A. Hassibi, "A photovoltaic-driven and energy-autonomous CMOS implantable sensor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 336–343, Aug. 2012.
- [5] Y. Amira and M. Ehara, "On-chip solar battery structure for CMOS LSI," *IEICE Electron. Exp.*, vol. 13, no. 13, pp. 287–291, Jul. 2006.
- [6] N. Guilar, A. Chen, T. Kleeburg, and R. Amirtharajah, "Integrated Solar Energy Harvesting and Storage," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 5, pp. 627–632, Feb. 2011.
- [7] M. A. Marwick and A. G. Andreou, "Photo-battery fabricated in silicon on sapphire CMOS," *IEEE Electron Device Lett.*, vol. 44, no. 12, pp. 766–767, Jun. 2010.
- [8] F. Horiguchi, "Integration of series-connected on-chip solar battery in a triple-well CMOS LSI," *IEEE Trans. Electron Devices*, vol. 59, no. 6, pp. 1580–1584, Jun. 2012.
- [9] M. K. Law and A. Bermak, "High-voltage generation with stacked photodiodes in standard CMOS process," *IEEE Electron Device Lett.*, vol. 31, no. 12, Dec. 2010.
- [10] S. Ghosh, H. T. Wang, and W. D. Leon-Salas, "A circuit for energy harvesting using on-chip solar cells," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4658–4671, Sep. 2014.
- [11] Y. Shih and B. P. Otis, "An inductor-less DC-DC converter for energy harvesting with a 1.2- μ W bandgap-referenced output controller," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, Dec. 2011.
- [12] J. Kim, P. K. T. Mok, and C. Kim, "A 0.15 V input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement," *IEEE J. Solid-State Circuits*, pp. 414–425, Feb. 2015.
- [13] Y. Lee, S. Bang, I. Lee, Y. Kim, G. Kim, M. H. Ghaed, P. Pannuto, P. Dutta, D. Sylvester, and D. Blaauw, "A modular 1 mm³ die-stacked sensing platform with low power I^2C inter-die communication and multimodal energy harvesting," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 229–243, Jan. 2013.
- [14] A. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," *Ann. Rev. Biomed. Eng.*, vol. 10, no. 1, pp. 247–274, 2008.
- [15] Z. Safarian and H. Hashemi, "Capacitance-sharing, dual output, compact, switched-capacitor DC-DC converter for low-power biomedical implants," *IET Electron. Lett.*, vol. 50, no. 23, pp. 1673–1675, Nov. 2014.
- [16] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V temperature-compensated subthreshold CMOS voltage reference," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, Feb. 2011.
- [17] P. Chen, K. Ishida, X. Zhang, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "0.18-V input charge pump with forward body biasing in startup circuit using 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2010, pp. 1–4.
- [18] M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," Ph.D. dissertation, Dept. Elect. Eng. and Comput. Sci., Univ. California, Berkeley, CA, USA, 2009.
- [19] D. Ma and R. Bondade, *Reconfigurable Switch-Capacitor Power Converters: Principles and Designs for Self-Powered Microsystems*. New York, NY, USA: Springer, 2013.



Zhiyuan Chen received the B.Sc. and M.Sc. degrees from the University of Macau (UM), Macao, China, in 2011 and 2013, respectively.

Currently, he is working toward the Ph.D. degree at UM State-Key Laboratory of Analog and Mixed-Signal VLSI and Faculty of Science and Technology—ECE. His research interests are solar and piezoelectric energy harvesting systems.



Man-Kay Law (M'11–SM'16) received the B.Sc. degree in computer engineering and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST), Kowloon, Hong Kong, in 2006 and 2011, respectively.

In February 2011, he joined HKUST as a Visiting Assistant Professor. Currently, he is an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, Faculty of Science and Technology, University of Macau, Macao. His research interests are on the development of ultra-low power circuits and integrated energy harvesting techniques for wireless sensing and biomedical applications. He developed an ultra-low power fully integrated CMOS temperature sensor for passive UHF RFID tag for commercialization together with Zhejiang Advanced Manufacturing Institute of HKUST (ZAMI). He has authored or coauthored more than 60 technical papers and holds three U.S. patents, and one Chinese patent.

Dr. Law was a member of the Organizing Committee of ASQED (2016), and the Technical Program/Review Committee of PrimeAsia (2011), ASQED (2012–13), ISCAS (2012–15), BioCAS (2012–15), and ISIC (2014). He is a member of the IEEE CAS committee on Sensory Systems as well as Biomedical Circuits and Systems. He was a corecipient of the ASQED Best Paper Award (2013), A-SSCC Distinguished Design Award (2015) and ASPDAC Best Design Award (2016). He also received the Macao Science and Technology Invention Award (2nd Class) by Macau Government—FDCT (2014).



Pui-In Mak (S'00–M'08–SM'11) received the Ph.D. degree from the University of Macau (UM), Macao, China, in 2006.

Currently, he is an Associate Professor at the UM Faculty of Science and Technology—ECE, and Associate Director (Research) at the UM State Key Laboratory of Analog and Mixed-Signal VLSI. His research interests are on analog and radio-frequency (RF) circuits and systems for wireless, biomedical and physical chemistry applications. His group contributed seven state-of-the-art chips at ISSCC: wideband receivers (2011, 2014, 2015), micro-power amplifiers (2012, 2014) and ultra-low-power receivers (2013, 2014). The team also pioneered the world-first Intelligent Digital Microfluidic Technology (iDMF) with micro-Nuclear Magnetic Resonance (μ NMR) and Polymerase Chain Reaction (PCR) capabilities. He has coauthored three books: *Analog-Baseband Architectures and Circuits for Multistandard and Low-Voltage Wireless Transceivers* (Springer, 2007), *High-/Mixed-Voltage Analog and RF Circuit Techniques for Nanoscale CMOS* (Springer, 2012), and *Ultra-Low-Power and Ultra-Low-Cost Short-Range Wireless Receivers in Nanoscale CMOS* (Springer, 2015).

Prof. Mak (co)-received the DAC/ISSCC Student Paper Award (2005); CASS Outstanding Young Author Award (2010); SSSC Pre-Doctoral Achievement Awards, 2014 and 2015; the National Scientific and Technological Progress Award (2011), and the Best Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (2012–2013). In 2005, he was decorated with the Honorary Title of Value for scientific merits by the Macau Government. His involvements with IEEE are: Editorial Board Member of IEEE Press (2014–2016); IEEE Distinguished Lecturer (2014–2015); Member of Board-of-Governors of IEEE Circuits and Systems Society (2009–2011); Senior Editor of IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (2014–2015); Guest Editor of IEEE RFIC Virtual Journal (2014); Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I (2010–2011, 2014–2015) and II (2010–2013). He is the TPC Vice Co-Chair of ASP-DAC 2016.



Rui P. Martins (M'88–SM'99–F'08) was born on April 30, 1957. He received the Bachelor (five-year degree), Masters, and Ph.D. degrees as well as the Habilitation for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), Technical University of Lisbon (TU of Lisbon), Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

Since October 1980, he has been with the Department of Electrical and Computer Engineering (DECE)/IST, TU of Lisbon. Since 1992, he has been on leave from IST, TU of Lisbon (since 2013, the University of Lisbon), and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor since August 2013. In FST he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since 1997. Since September 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed (in 2013), as Vice-Rector (Research) until August 2018. Within the scope of his teaching and research activities he has taught 21 bachelor and master courses and has supervised (or cosupervised) 38 theses, Ph.D. degrees (17), and Masters degrees (21). He has coauthored six books and five book chapters; 16 Patents, USA (14) and Taiwan (2); 320 papers in scientific journals (82) and in conference proceedings (238); as well as 61 other academic works in a total of 408 publications. He was a cofounder of Chipidea Microelectronics (Macao) [now Synopsys] in 2001–2002, and, in 2003, created the Analog and Mixed-Signal VLSI Research Laboratory of UM, elevated in January 2011 to State Key Laboratory of China (the first in Engineering in Macao), being its Founding Director.

Dr. Martins was the Founding Chairman of IEEE Macau Section (2003–2005), and IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) (2005–2008) [2009 World Chapter of the Year of IEEE CASS]. He was the General Chair of 2008 IEEE Asia-Pacific Conference on CAS—APCCAS (2008), and was the Vice President for Region 10 (Asia, Australia, and the Pacific) of IEEE CAS Society (2009–2011). Since then, he was Vice President (World) Regional Activities and Membership of IEEE CAS Society (2012–2013), and Associate Editor of IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS (2010–2013), nominated Best Associate Editor of T-CAS II for 2012 to 2013. In addition, he was a member of the IEEE CASS Fellow Evaluation Committee (2013 and 2014), and the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—Director of the IEEE. He is now the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC (2016). He was the recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010, he was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.