Metastablility in SAR ADCs

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Abstract—The fundamental limitation of Nyquist analog-to-digital converter (ADC) architectures toward high speed is metastability. It refers to the inability of a latched comparator to produce a valid decision in a certain available time. This issue is usually severe in high-speed successive approximation register (SAR) ADCs due to their serial conversion scheme, which includes the regeneration and the reset process of the comparator in a feedback loop, thus significantly reducing the available time for the regeneration. Our analysis considers the probability of metastability errors as a function of their magnitude and is customized for a timer-based asynchronous SAR ADC (with loop time-out). The resulting framework can also quantify the metastability in a synchronous architecture, and we provide a numerical comparison. To validate the analysis, measurement results of an 8-bit 130-MS/s SAR ADC in 90-nm CMOS are provided.

Index Terms—Analog-to-digital converter (ADC), comparator, metastability, successive approximation register (SAR).

I. Introduction

METASTABILITY is an error phenomenon whose characteristics are difficult to predict, since they depend on the applied input and the circuit implementations. The resulting impairment is usually not quantified in the form of signal-to-noise ratio in data converters because the rate of its occurrence is relatively low. Instead, the error is characterized as a probability (P_E) or mean time to error. In addition, the magnitude of the generated error depends on the circuit architecture and implementation [1]. Examples of mixed-signal applications requiring low error rate include digitizing oscilloscopes and wireline communication systems, where the error probability must be on the order of $10^{-15}-10^{-17}$ [2]. In high-speed analog-to-digital converter (ADC) designs, the penalty for reducing the error rate can imply considerable circuitry complexity and higher power consumption and die area [3]; thus, the study on the tradeoffs and error characteristics of metastability in different architectures becomes important.

Due to technology scaling, the speed of a single-channel SAR ADC can go well above several hundred megahertz [4], [5]. Since the successive approximation (SA) operation is based on the decisions of the comparator, it experiences metastability issues at high speed with less time available for the regeneration. The asynchronous SA loop [6] is typically adopted for high-speed design, and the timer-based asynchronous loop employed in [7] comes with similar advantages over a fully synchronous design. In this brief, we analyze the timer-based asynchronous (TB-ASYN) SAR ADC. The resulting equations can be also used to predict the metastability behavior of a synchronous design.

This brief is organized as follows. We first discuss the design tradeoffs and error characteristics for synchronous (SYN), asynchronous (ASYN), and TB-ASYN SAR ADCs. The basics of metastability and the associated power tradeoffs in SAR ADCs are then reviewed in Section II. Section III analyzes different metastability error mechanisms. A model for error prediction is given in Sections IV and V. Finally, the measurement results are discussed in Section VI.

II. Background on Metastability and Tradeoffs in the SAR ADC

A. Synchronous and Asynchronous Versus Timer-Based Asynchronous

For a properly designed N-bit SAR ADC without redundancy, there is only one single critical comparison where the comparator input is within ± 1 least significant bit (LSB), and the other $(N-1)$ decisions are more relaxed with a larger input. Thus, in conventional ASYN SAR ADCs [6], additional time is made available for the critical comparisons by allocating time away from the easier ones through detection logic at the comparator's outputs. On the other hand, SYN SAR ADCs have all cycles set by the worst case timing for a hard comparison. Hence, less time is available for the critical decision. The available time for the most critical comparison, i.e., $T_{\text{comp},g}$, of the ASYN and SYN SAR ADCs can be expressed as

$$T_{\text{comp},g,\text{asSAR}} = T_S - T_{\text{SAM}} - T_O - T_{\text{comp,easy\_tot}} \tag{1}$$

$$T_{\text{comp},g,\text{sySAR}} = T_S - T_{\text{SAM}} - T_O - T_{\text{comp,hard}} \cdot (N-1) \tag{2}$$

where $T_{\text{comp,easy\_tot}}$ is the total required time for all easy comparisons, $T_{\text{comp,hard}}$ is the worst case time for the hard comparison, T_S is the sampling period, T_{SAM} is the sampling time, and T_O is the total time for the logic propagation and

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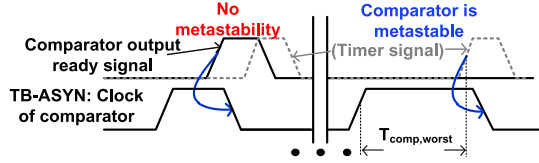Digital Object Identifier 10.1109/TCSII.2016.2554798

Fig. 1.   Timing diagram of the TB-ASYN SAR ADC.

digital-to-analog converter (DAC) settling in all SA cycles. Since the total time for easy comparisons is shorter than $(N-1)$ times the hard comparison, a lower error probability can be achieved with longer $T_{\mathrm{comp},g}$ in ASYN SAR ADCs.

A variant of the ASYN approach with an added timer was proposed in [7], as shown in Fig. 1. It does not only asynchronously detect the activity from the comparator but also runs a timer that forces the SAR ADC to proceed to the next cycle if the length of the worst case cycle exceeds a prescribed maximum time $(T_{\mathrm{comp,worst}})$. It means that the asynchronous logic controls the timing of the SA loop during the easy comparisons (same as the ASYN SAR ADC), whereas the timer may interject during very difficult decisions. In the design in [7], the timer does not override the bit decision logic, but just controls the reset of the comparator (thus avoiding race conditions). This approach benefits from a longer available time for the hard comparison (similar to the conventional ASYN SAR ADC), where $T_{\mathrm{comp},g}$ in this type of ADC is now equal to $T_{\mathrm{comp,worst}}$.

The analyses conducted in the next sections are applicable to the TB-ASYN SAR ADC (such as [7]) and to the SYN SAR ADC, where both types have a fixed maximum available time for the critical comparison. However, it is worth noting that the former one has lower error probability due to longer available time for the critical comparison.

B. Fundamentals

In order to avoid metastability, the comparator's output must reach a valid logic level V_{valid} before a given time $T_{\mathrm{comp},g}$ for a desired input difference. Assuming that the signal is uniformly distributed across the input range of the comparator, the probability of a metastable event is [1] (considering no preamplifier)

$$P_E = \frac{V_{\mathrm{valid}}}{A_{\mathrm{eff}} V_d} \exp\left(-\frac{T_{\mathrm{comp},g}}{\tau_{\mathrm{reg}}}\right) \qquad (3)$$

where V_d is the full-scale input voltage range of the comparator, τ_{reg} is the regeneration time constant, and A_{eff} is the gain between the initial voltage at the regeneration nodes when the cross-coupled inverters are turned on, as well as the input signal. $T_{\mathrm{comp},g}$ is the available time for the most critical comparison, which is different in the synchronous and asynchronous versions, as expressed in (1) and (2).

C. Power Tradeoff

In SAR ADCs without redundancy, there exists only one comparison per cycle that experiences the most critical metastable condition. In order to show the design tradeoff against the power consumption, an analysis is conducted next. For simplicity, A_{eff}, V_d, and V_{valid} are now normalized to unity in (3). As $P_E = V_{d,\mathrm{min}}/V_{\mathrm{LSB}}$ (where V_{LSB} is the LSB of the ADC and is equal to $1/2^N$, N is the bit resolution, and $V_{d,\mathrm{min}}$ is the minimum input voltage with which the comparator can
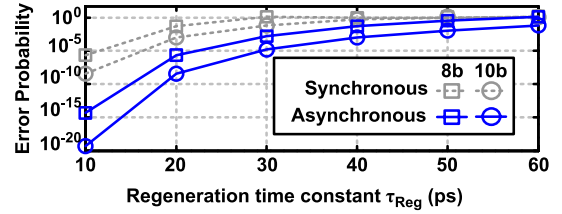

Fig. 2.   Error probability versus regeneration time constant of the comparator in the SAR ADC.

regenerate a valid decision), the error probability with a certain regeneration time constant τ_{reg} is then simplified to

$$P_E = 2^N \cdot \exp\left(-\frac{T_{\mathrm{comp},g}}{\tau_{\mathrm{reg}}}\right). \qquad (4)$$

Based on (4), the regeneration time constant versus the error probability is plotted in Fig. 2 under the following assumptions: 1) the sampling frequency is 100 MHz; and 2) 30% is for sampling, and 70% is for DAC, logic settling, and comparison. As in (4), the error probability has an exponential relationship over the time constant. When increasing the bit resolution, a steep tradeoff is experienced due to the simultaneous growth in the number of SA cycles in the SYN SAR ADC. Furthermore, as more time is available for the critical comparison in the asynchronous version, the error probability is significantly lower. The shown result is based on simulations of a typical 8- to 10-bit design in 65-nm CMOS technology, in which the total time of the easy comparisons occupies around half of the entire available time for decision, as also indicated in [6].

In order to reduce the time constant for a fixed technology, it is necessary to increase the width of the transistors at the regenerative nodes. However, as the self-loading capacitance also grows proportionally with the transconductance, the speed improvement experiences diminishing returns. This can be quantified by the following equation, which models the regeneration time constant with respect to the width-scaling factor S_w of the comparator:

$$\tau_{\mathrm{reg}} \propto \tau_{\mathrm{int}}\left(1 + \frac{\alpha}{S_w}\right). \qquad (5)$$

Here, α represents the ratio between external and internal capacitance, and τ_{int} is the regeneration time constant with the internal load. The case of $S_W = 1$ corresponds to a minimum sizing of the transistor in the latch. Accordingly, the error probability P_E has a tradeoff over power, which is expressed by

$$P_E \propto \exp\left(-\frac{1}{(\alpha/S_{\mathrm{power}} + 1)} \cdot \frac{T_{\mathrm{comp},g}}{\tau_{\mathrm{int}}}\right) \qquad (6)$$

as the power grows proportionally with S_w ($S_{\mathrm{power}} \propto S_w$), and the designs where the metastability matters naturally operate at large values of S_w, such as 5 or higher [8]. Fig. 3 depicts explicitly the trend of P_E versus the S_{power} of the latch for $\alpha = 0.5$, $T_{\mathrm{comp},g}/\tau_{\mathrm{int}} = 12.5$, and $S_{\mathrm{power}} > 4$. The aforementioned behavioral model is also compared with *Spice* transistor-level simulations. In the simulation, the size (width) of the transistors in the comparator is scaled from the minimum by the corresponding scaling factor S_{power}, and their time constants are extracted and plugged in (6) to plot the curve in Fig. 3. Both estimation and simulation results show that there is a relatively small improvement if the size of the regeneration transistors increases, particularly for a large value of S_w. The
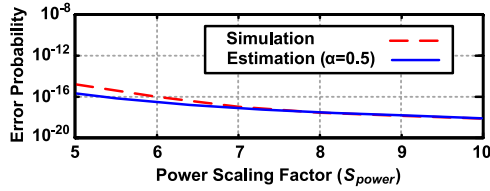
Fig. 3. Error probability [from (6)] versus power scaling factor (S_{power}); estimation and simulation results with S_{power}.
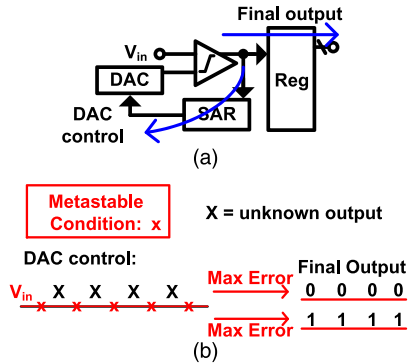

Fig. 4. (a) Conventional SAR block diagram. (b) Metastable error characteristics in the SAR ADC.

improvement of P_E eventually stays almost constant, and extra power is wasted, which implies that increasing the size gives diminishing returns for the error rate reduction as we approach the technology limits.

III. ERROR CHARACTERISTIC IN SAR ARCHITECTURES

Fig. 4(a) shows the conventional architecture of a SAR ADC (single-ended), which consists of a DAC, SA logic, a comparator, and a register. One of the possible metastable scenarios in the SAR ADC is depicted in Fig. 4(b). When the input difference is much lower than the decision threshold of the comparator, its output is at an undefined level. As this invalid logic level is not able to fully trigger the switches and make the DAC settle to the final value within the given time frame, the residue could turn out to be around zero in the subsequent successive comparisons in the worst case scenario. Since the resulting codes in every bit are unpredictable, the maximum possible error can be at the half-scale.

The other possible error caused by the metastability of the comparator is due to inconsistent decisions between decoding, SA logic, and DAC switching. When the comparator is in a metastable condition, the outputs are interpreted with an undefined level. Due to a nonmatched implementation of the SA feedback logic and register circuitries, the final logic decisions of these two blocks may differ, which can cause a catastrophic error. Although this mechanism may lead to a large error, its occurrence can be greatly suppressed by proper design schemes such as in [7]. Therefore, the former error has a dominating effect, and only that will be analyzed in the following sections in detail.

IV. CIRCUIT MODEL FOR ERROR CHARACTERIZATION

The model setup is based on [9] and the operation of the prototype [7] introduced in Section VI, which has the following characteristics: 1) top-plate sampling; 2) VCM-based switching
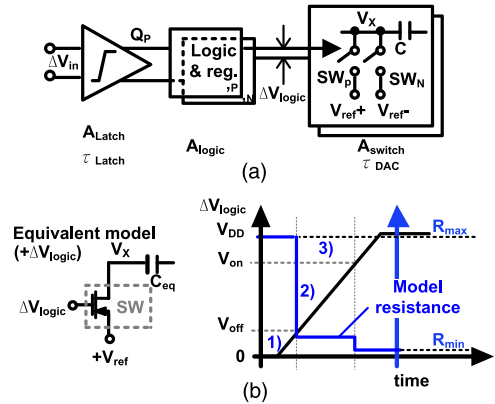

Fig. 5. (a) Model setup of signal path from the input to the DAC control. (b) Equivalent single-ended piecewise linear approximation model of the DAC settling.

[10]; and 3) settling of the comparator, logic, and DAC happening simultaneously within a bit conversion time. Furthermore, a piecewise linear approximation model [9] is adopted to simplify the settling behavior of the DAC switches.

As the SA switching in each cycle depends on the decision of the previous comparison, the signal path from the metastable comparator to the bottom-plate switches of the DAC can be illustrated as in Fig. 5(a). Considering the case where the comparator is in metastable state, then an undefined logic level is at the output (Q_P) and applies to the subsequent logic block. Under this condition, both switches $(SW_P$ and $SW_N)$ for positive and negative references turn on simultaneously and form a short-circuit current between the two references. In order to simplify the model for analysis, the following assumptions are made: 1) the reference voltages are symmetric around midsupply $(|V_{\mathrm{ref}+}| - V_{DD}/2 = V_{DD}/2 - |V_{\mathrm{ref}-}|)$; 2) the pMOS and nMOS transistors of the bottom-plate switches and the logic circuit draw the same amount of current when their gate voltage is at $V_{DD}/2$; and 3) three states are defined based on different values of $\Delta V_{\mathrm{logic}}$ and assuming that $V_{\mathrm{ref}}\pm$ are equal to V_{DD} and ground, respectively. Fig. 5(b) depicts the three cases with a single-ended equivalent model of the DAC (only for $\Delta V_{\mathrm{logic}} >= 0$). V_{on} and V_{off} are the turn-on and turn-off voltages of the switches, respectively, which are similar to the voltage input high and voltage input low of an inverter. Fig. 5(b) also illustrates the equivalent resistance in the piecewise linear approximation model.

When the input difference of the comparator (ΔV_{in}) is 0, V_X is at $V_{DD}/2$ due to the symmetrical current drawn through the switches $(SW_P$ and $SW_N)$. When there is small V_{in}, the regeneration time constant (τ_{reg}), the gain from the latch (A_{latch}), the logic (A_{logic}), and the switch (A_{switch}) try to regenerate and amplify the input difference at V_X, which reduces the short-circuit current and biases V_X to either up/down direction, eventually. Furthermore, the logic with the register is simply modeled with a logic gain (A_{logic}) since this circuit is implemented with a dynamic latch without any positive feedback. For simplicity, A_{tot} is defined for the upcoming analysis as $A_{\mathrm{tot}} = A_{\mathrm{latch}} \times A_{\mathrm{logic}} \times A_{\mathrm{switch}}$.

V. CHARACTERIZATION OF THE ERROR AMPLITUDE

The errors are categorized in three types depending on $\Delta V_{\mathrm{logic}}$, as explained in the previous section.

A. DAC Switches Fully Off: Case 1

If the input difference of the comparator is exactly zero, the regeneration circuit is not able to make a valid decision even with time. Then, a zero residue appears on the DAC, which causes a large value of error. The first two bit conversions of a SAR ADC are considered as an example. When the decision from the first comparison is invalid, the residue for the next bit comparison remains unchanged (V_{in}). The ideal residue should be $V_{in} \pm V_{ref}/2$, and in this case, the error amplitude is at half-scale. In addition, the error magnitude varies with the current (metastable) converting bit as

$$|E_A| = \frac{1}{2^{N_C}} V_{ref} \qquad (7)$$

where N_C is the bit resolution at the current comparison. The preceding equation is valid for all SAR bit conversions, except the last one, because there is no DAC switching performed in the last step.

B. DAC Switches Weakly On and Strongly On: Case 2 and Case 3

When the comparator's output reaches a value between V_{off} and V_{on}, the residue of the DAC is not able to settle to the correct value due to the short-circuit current in the reference voltages. In addition, the resistance of the DAC switches is large as they are weakly turned on, which leads to an incomplete settling error. The error amount can be expressed as [9] (assuming that switching and decoding are consistent)

$$|E_B| = \frac{V_{ref}}{2^{N_C}} \exp\left(-\frac{T_{DAC}}{\tau_{DAC,weak}}\right) \qquad (8)$$

where τ_{DAC} is the time constant of the DAC at the weakly on condition, and T_{DAC} is the available time for the DAC settling. T_{DAC} can be indicated as (when considering the preamplification time and the regeneration of the comparator)

$$T_{DAC} = T_{conv} - T_{pre} - \tau_{reg} \ln\left(\frac{V_{off}}{A_{tot}|\Delta V_{in}|}\right) \qquad (9)$$

where V_{off} is the voltage level at the logic's output in order to weakly turn on the DAC switch, T_{conv} is the worst case bit conversion time, and T_{pre} is the required time for preamplification in order to turn on the latch operation. The error in (8), by introducing (9), can be rewritten as

$$|E_B| = \frac{V_{ref}}{2^{N_C}} \left(\frac{V_{off}}{A_{tot}|\Delta V_{in}|}\right)^{\frac{\tau_{reg}}{\tau_{DAC,weak}}} \exp\left(-\frac{T_{conv} - T_{pre}}{\tau_{DAC,weak}}\right). \qquad (10)$$

The error magnitude, as $|E_A|$ in (7), is also divided by the current resolving number of bits N_C.

Furthermore, if the DAC switches are strongly turned on, but the input voltage is still relatively small, it is also possible that the DAC might have insufficient time to settle and causes error (E_C). Then, (10) can be reused, but now, the turn-on voltage and the DAC time constant are in the strongly on condition. For E_C, V_{off} and $\tau_{DAC,weak}$ in (10) are replaced by V_{on} and $\tau_{DAC,strong}$, respectively. It is worth noting that E_B and E_C can be greatly suppressed by employing redundancy [5].
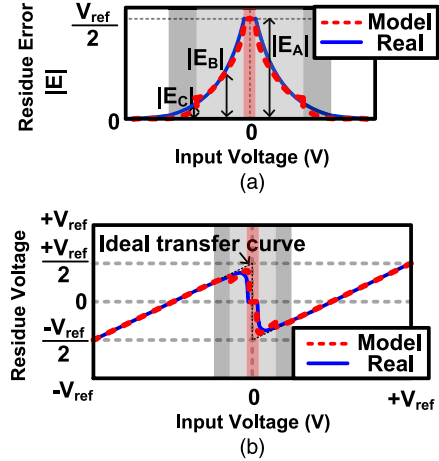

Fig. 6. Modeling and real results of the (a) error amount from $|E_A|$, $|E_B|$, and $|E_C|$. (b) Effect of these errors in the residue.

Fig. 6(a) sketches the errors $|E_A|$, $|E_B|$, and $|E_C|$, as a function of V_{in}, for a 2-bit SAR ADC. Furthermore, Fig. 6(b) illustrates the effect on the residue qualitatively. Both simulation and modeling results are provided and exhibit a good agreement.

VI. ERROR PROBABILITY

To compute the probability for which the error is greater than E_1 in the overall N-bit SAR ADC, it is important to recall from (7) and (8) that the amount of error in $|E_A|$, $|E_B|$, and $|E_C|$ are all scaled down by the number of the present comparison bit. The error probability greater than the interest amount (E_1) for a general N-bit SAR ADC, when considering the numbers of decision thresholds V_{th} and the error probability regions that double in each successive quantization bit, can be expressed as [9]

$$P(E > E_1)_{Nbit,SAR} = \max\left\{2\Delta V_{1,i} \cdot 2^{i-1}[f_{Vin}(V_{th,i})]\right\}_{i=1\sim N} \qquad (11)$$

where $f_{Vin}(V_{th,i})$ is the probability density function of the input at the corresponding thresholds, $\Delta V_{1,i}$ is the voltage difference yield E_1 in each SA bit, and $V_{th,i}$ is the corresponding comparison threshold. Equation (11) represents the error probability which has the error magnitude larger than the one of interest (E_1). The term $2\Delta V_{1,i}$ is originated from considering both the positive and negative input voltages that cause the error magnitude larger than E_1. As the error probability is affected by the input probability density function [9], f_{Vin} in each comparison threshold needs to be considered. Since the error magnitude is referred to the input in each conversion bit, the overall error probability of an N-bit SAR is given as the following equations, which is obtained by rearranging (3), (10), and E_C [by replacing V_{off} and $\tau_{DAC,weak}$ with V_{on} and $\tau_{DAC,strong}$ in (10)], according to V_{in} and then replacing $\Delta V_{1,i}$ in (11):

$$P(E = E_A)_{Nbit,SAR}$$
$$= \left\{\frac{V_{off}}{A_{tot}}\left[\exp\left(-\frac{T_{comp,g}}{\tau_{reg}}\right)\right] \times 2^i \cdot f_{Vin}(V_{th,i})\right\}_{i=1\sim N} \qquad (12)$$
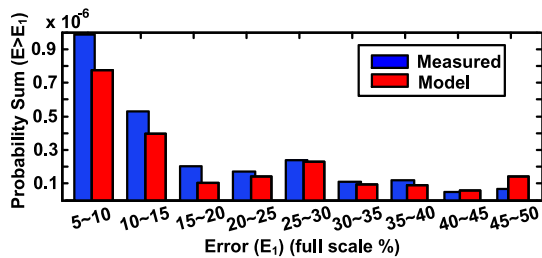
Fig. 7. Error rate versus error magnitude in histogram form, with data grouped in nine intervals.

$$P(E > E_B)_{\text{Nbit,SAR}}$$
$$= \left\{ \frac{2V_{\text{off}}}{A_{\text{tot}}} \left[\frac{E_B}{V_{\text{ref}}} \exp\left(\frac{T_{\text{conv}}}{\tau_{\text{DAC,weak}}} \right) \right]^{-\frac{\tau_{\text{DAC,weak}}}{\tau_{\text{reg}}}} \right.$$
$$\left. \times\ 2^{-i\cdot\left(\frac{\tau_{\text{DAC,weak}}}{\tau_{\text{reg}}}\right)} 2^i \cdot f_{\text{Vin}}(V_{\text{th},i}) \right\}_{i=1\sim N} \quad (13)$$

$$P(E > E_C)_{\text{Nbit,SAR}}$$
$$= \left\{ \frac{2V_{\text{on}}}{A_{\text{tot}}} \left[\frac{E_C}{V_{\text{ref}}} \exp\left(\frac{T_{\text{conv}}}{\tau_{\text{DAC,strong}}} \right) \right]^{-\frac{\tau_{\text{DAC,strong}}}{\tau_{\text{reg}}}} \right.$$
$$\left. \times\ 2^{-i\cdot\left(\frac{\tau_{\text{DAC,strong}}}{\tau_{\text{reg}}}\right)} 2^i \cdot f_{\text{Vin}}(V_{\text{th},i}) \right\}_{i=1\sim N} \quad (14)$$

$$P(E > E_1)_{\text{Nbit,SAR}}$$
$$= \max\{ P(E > E_B), P(E > E_C), P(E = E_A) \}. \quad (15)$$

The preceding equations hold only when T_{conv} are identical in every step of the conversion, which is true for TB-ASYN or SYN SAR ADCs being with a fixed worst case time slot for each cycle. From (15), depending on the time allocation, one of the errors can be dominant. It can be also noticed that the linear gain A_{tot} from the logic or before the latch should have a relatively small effect on P_E, since the exponential term from the regeneration circuit dominates the error probability. Furthermore, there should only be one metastable event in all SA cycles, and the overall error rate is the worst case among all of the N-bit stages in E_A, E_B, and E_C.

Unlike the pipeline ADC, where each stage contains its own latches, the comparator of the SAR ADC requires a reset before the next bit comparison, which induces a tradeoff between the reset time and the metastability rate. In addition, E_A occurs rarely in the pipeline ADC since $T_{\text{comp},g}$ is often long when considering the same sampling speed as the SAR ADC. Thus, the probability of those peak values which are near the comparator's decision thresholds is smaller in the pipeline ADC.

VII. EXPERIMENTAL RESULTS

The model is now verified through the measurement of a SAR ADC in 90-nm CMOS technology, which was previously presented in [8] and reconfigured to 8 bits at 130 MS/s. According to the test setup of the metastability error probability [10], the input frequency must be carefully chosen to ensure that the output code has less than 1 LSB change in adjacent samples after the decimation ($25\times$ decimation factor). By comparing the successive outputs with the error limit, the metastability error rate and magnitude can be detected. A total of 20000 samples is obtained within 24 hours of continuous testing.

As averaging cannot be performed with the adopted setup, the results are expected to be affected by electronic noise from thermal, quantization, and differential nonlinearity [10]. The metastable window of the comparator based on simulation is only 0.6 μV, whereas its input-referred noise ($V_{\text{in}}(\sigma)$) is around 0.5 mV (0.13 LSB). The ratio is more than 1000-fold. Therefore, the metastable error with less than 3 LSBs is not considered in the final results.

In Fig. 7, the histogram of the raw measured data and the model values are illustrated, where the x-axis (error magnitude) is grouped into nine bins. Both statistics share similar characteristics, and there are peaks in the error probabilities at 12.5%, 25%, and 50% due to the contribution of E_A. Although there is some discrepancy in the error magnitude, the developed model shows a reasonable agreement. The values of the parameters for obtaining the model curve are as follows: $\tau_{\text{reg}} = 13$ ps, $A_{\text{tot}} = 3.8$, $\tau_{\text{DAC,weak}} = 187$ ps, $\tau_{\text{DAC,strong}} = 85$ ps, $V_{\text{on}} = 0.95$ V, $V_{\text{off}} = 0.36$ V, $T_{\text{pre}} = 120$ ps, $T_{\text{comp},g} = 200$ ps. Finally, we have also adopted the developed model in the pure synchronous SA loop, where the total available regeneration is equally distributed for each bit. The P_E of the synchronous loop is increased by ~1000 times versus the timer-based asynchronous loop.

VIII. CONCLUSION AND FUTURE WORK

Different from the flash or pipeline ADCs, the SAR ADC has its own characteristics with regard to metastability. Depending on the time allocation in the design, both the comparator and the incomplete settling of the DAC have significant effects on the error probability. Although this work was concentrated on a certain switching scheme, the metastable error probability of different switching approaches can be also investigated based on the method presented. The developed model is only suitable for the TB-ASYN and fully SYN SAR ADCs; on the other hand, metastability in purely asynchronous architectures is an interesting subject for future work.

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