A Novel Algorithm for Automated Optimum Design of IIR SC Decimators

Cheong Ngai, Rui P. Martins, and José E. Franca

***Abstract*—This brief presents a novel algorithm for optimizing the design of infinite-impulse response (IIR) switched-capacitor (SC) decimators. It is implemented with a computer-assisted iterative methodology to achieve minimum capacitance spread and usually leading also to the minimization of the total capacitor area, while considering scaling for maximum signal handling capability. A linear/nonlinear programming method is adopted for optimum adjustment of the capacitance values, within a specific decimator structure and a finite number of iterations. Several examples of automatic and optimum design of second-order IIR SC decimators are presented, together with a comparison against previous designs, obtained for the same circuits through the use of traditional methods.**

***Index Terms*—Automated optimum design, infinite-impulse response (IIR) switched-capacitor (SC) decimator, linear/nonlinear programming.**

I. Introduction

In infinite-impulse response (IIR) switched-capacitor (SC) decimator design, several sets of capacitance ratios are usually generated for implementation of the numerator and denominator of complex transfer functions. Conventional design methods that employ a structure of two-integrators-in-a-loop (TIL) to implement the denominator, assume that all feedback capacitors, in each integrator, have a unit value before the design equations are solved [1]–[3]. The different capacitance values in the SC input branches are usually difficult to be determined in order to map onto the given numerator coefficients of the modified z-transfer function [4]–[6]. Those values are normally calculated after a complex trial-and-error procedure that implies several design iterations to determine the most appropriate coefficient arrangement that minimizes the total capacitor area and capacitance spread. Furthermore, the adoption of these methods can lead to unacceptably large capacitance ratios in the cascade design of such decimators, after scaling for maximum signal handling capability and normalization with respect to the unit capacitance values.

In this brief we will present an alternative method which uses a novel algorithm based on a constraint programming model that employs multiple objectives and linear/nonlinear constraints to achieve the minimum possible capacitance spread and also minimization of total capacitor area, which will lead to a smaller power consumption. Rather than changing the topology of SC decimator, this approach uses mathematically defined requirements as a set of independent objectives that will be achieved after a design sequence with two steps for the implementation of the denominator and numerator of the modified z-transfer function. The main objectives are defined to obtain a convergent solution, while simultaneously satisfying the constraints determined by the design procedure. For example, all the capacitance values from the input branches are initially expressed as a linear algebraic expression obtained from the modified numerator function of the decimator. Then, after capacitance scaling, the capacitance spread will depend on the final absolute deviations between the unit capacitance and each capacitance value of the set of capacitors that are connected to the same operational amplifier (OA) input. Hence, the capacitance values in the input branches are defined under a minimum nonlinear objective to achieve minimum capacitance spread and also the minimization of total capacitor area, while also considering the maximum signal handling capability and capacitance scaling [2]–[6]. An interactive SC compiler, designated as **I**nteractive Compiler of **S**witched **C**apacitor **M**ulti**RATE** Circuit (**ISCMRATE**) recently developed [7], embodies the new algorithm and uses MATLAB[1] [8] for linear/nonlinear programming and optimization of the implementation.

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II. Iterative and Automatic Design Methodology

The design methodology for IIR SC decimators proposed in this brief (programmed in C++ for Unix), can be described and illustrated by the simple flow-chart of Fig. 1. This comprises an initial design procedure in two steps, followed by a first test of a feasible solution and finally by the simulation and final test of the results (after maximizing the signal handling capability and scaling the capacitance values). This iterative process will continue until an optimum solution (with minimum capacitance spread and the corresponding minimized total capacitor area) is reached.

To illustrate the proposed design methodology, we shall consider the design of a second-order IIR SC decimator. The design starts by the determination of the z-transfer function of the prototype filter, as part of the *initialization* process (that uses the program QED [9]), and which can be expressed as

$$H(z) = \frac{\sum_{j=0}^{N} (a_j \cdot z^{-j})}{1 - 2\cos(\theta_p) \cdot r_p \cdot z^{-1} + r_p^2 \cdot z^{-2}} \tag{1}$$

where N is an arbitrary order of the numerator polynomial function. For a given decimating factor M, the modified z-transfer function of a decimator, presented in [4], can be determined as shown in (2) at the bottom of the next page where $\alpha_j = \alpha_{[2(M-1)-j]}$, with $\alpha_0 = 1$ and $\alpha_j = \sum_{\ell=0}^{j/2} [2\cos(2\ell \cdot \theta_p)] + 1$, for j even and $\alpha_j = 2\sum_{\ell=0}^{j/2} \cos[(2\ell + 1)\theta_p]$, for j odd.

Then, the corresponding SC implementation [4]–[6], as shown in Fig. 2, can be obtained from the following z-transfer function as shown in (3a) at the bottom of the next page where

$$X(z) = \sum_{i=0}^{M-1+N} (X_i \cdot z^{-i}) \quad \text{and} \quad Y(z) = \sum_{i=0}^{M-1+N} (Y_i \cdot z^{-i}). \tag{3b}$$

From this z-transfer function, it would be possible to obtain the final capacitor ratios, after maximizing the signal handling capability (scaling both outputs of the OAs in order to have the same peak amplitude value) or dynamic range adjustment (according with [2], [3]) by capacitance scaling. Based on this procedure, the capacitance spread (C_{spread}) and the total capacitor area ($Total\,C$) can be expressed as

a)

$$\mathbf{C_{spread}} = \max\left\{ \frac{\mu_1}{\nu_2} A,\ \frac{\mu_1}{\nu_1} B,\ \frac{\mu_1}{\nu_1} FB,\ \frac{\mu_2}{\nu_2} C,\ \frac{\mu_2}{\nu_2} D,\ \frac{\mu_2}{\nu_2} FD,\ \frac{\mu_2}{\nu_1} E,\ \sum_{i=0}^{M-1+N} \frac{X_i}{\nu_1},\ \sum_{i=0}^{M-1+N} \frac{Y_i}{\nu_2} \right\} \tag{4}$$

where $\nu_1 = \min\{\mu_1 B, \mu_1 FB, \mu_2 C, \mu_2 E, X_i\}$ and $\nu_2 = \min\{\mu_1 A, \mu_2 D, \mu_2 FD, Y_i\}$, ν_j represents the minimum capacitance value in the input node j of each OA and μ_i

[1]MATLAB is a registered trademark of The MathWorks, Natick, MA.

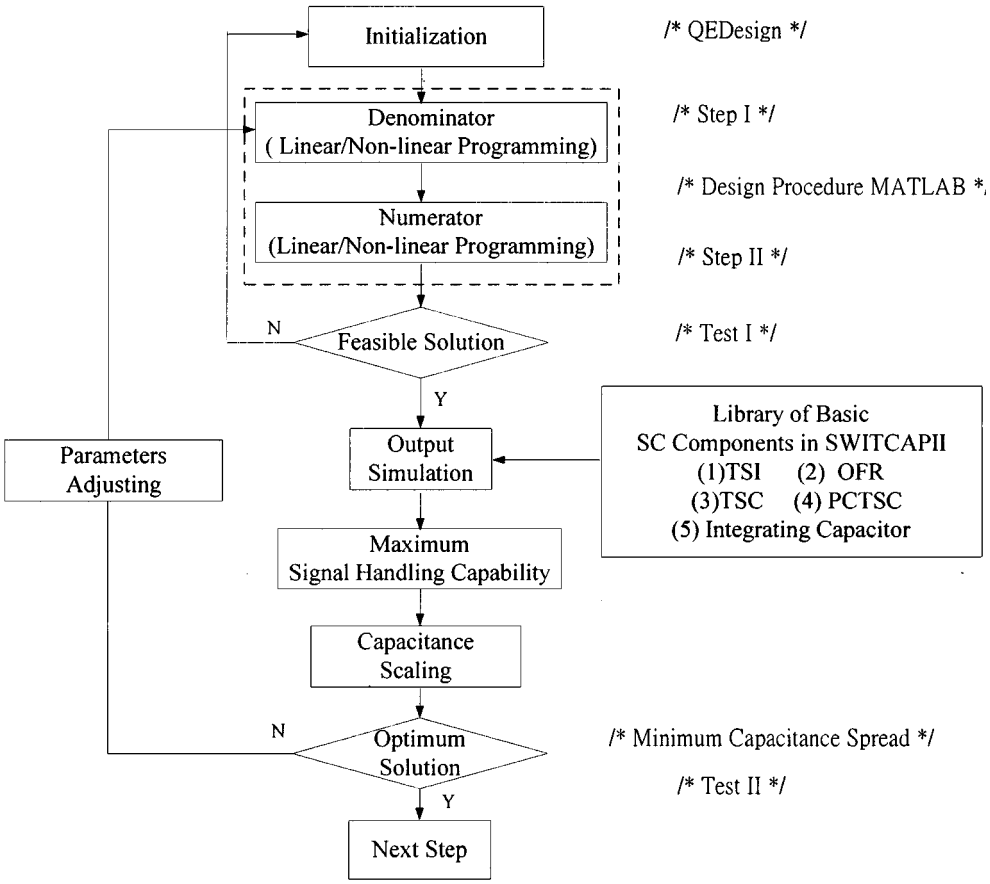

Fig. 1. Interactive and automatic design methodology for IIR SC decimators (C++, Unix).

$$\overline{H}(z) = \frac{\sum_{j=0}^{N}(a_j\cdot z^{-j})\cdot\sum_{j=0}^{M-1}\left\{\left[\frac{\cos(\theta_p)+i\cdot\sin(\theta_p)}{r_p}\right]^{M-1-j}\cdot z^{-j}\right\}\sum_{j=0}^{M-1}\left\{\left[\frac{\cos(\theta_p)-i\cdot\sin(\theta_p)}{r_p}\right]^{M-1-j}\cdot z^{-j}\right\}}{\left\{\left[\frac{\cos(\theta_p)+i\cdot\sin(\theta_p)}{r_p}\right]^{M}-z^{-M}\right\}\cdot\left\{\left[\frac{\cos(\theta_p)-i\cdot\sin(\theta_p)}{r_p}\right]^{M}-z^{-M}\right\}}$$
$$= \frac{\sum_{j=0}^{N}(a_j\cdot z^{-j})\cdot\left[1+\alpha_1\cdot r_p\cdot z^{-1}+\cdots+\alpha_j\cdot r_p^{j}\cdot z^{-j}+\cdots+\alpha_{2(M-1)}\cdot r_p^{2(M-1)}\cdot z^{-2(M-1)}\right]}{1-2\cos(M\theta_p)\cdot r_p^{M}\cdot z^{-M}+r_p^{2M}\cdot z^{-2M}}$$
$$= \frac{\sum_{j=0}^{N}(a_j\cdot z^{-j})\cdot\sum_{j=0}^{2(M-1)}(\alpha_j\cdot r_p^{j}\cdot z^{-j})}{1-2\cos(M\theta_p)\cdot r_p^{M}\cdot z^{-M}+r_p^{2M}\cdot z^{-2M}} = \frac{\sum_{j=0}^{2(M-1)+N}(\overline{a}_j\cdot z^{-j})}{1-2\cos(M\theta_p)\cdot r_p^{M}\cdot z^{-M}+r_p^{2M}\cdot z^{-2M}} \tag{2}$$

$$T(z) = \frac{(B+FB)[X(z)-(C+E)\cdot Y(z)]+[E\cdot Y(z)-B\cdot X(z)]\cdot z^{-M}}{(D+FD)(B+FB)+[A\cdot(C+E)-(2B\cdot D+D\cdot FB+B\cdot FD)]\cdot z^{-M}+[B\cdot D-A\cdot E]\cdot z^{-2M}} \tag{3a}$$

represents the peak amplitude value at the output node i of each OA.

b)

$$\mathbf{Total\,C} = \frac{\mu_1}{\nu_2}A+\frac{\mu_1}{\nu_1}(B+FB)+\frac{\mu_2}{\nu_1}C+\frac{\mu_2}{\nu_2}(D+FD)+\frac{\mu_2}{\nu_1}E+\sum_{i=0}^{M-1+N}\frac{X_i}{\nu_1}+\sum_{i=0}^{M-1+N}\frac{Y_i}{\nu_2} \tag{5}$$

A design procedure with feasible directions can then be chosen with the following assumptions.

i) The X_i and Y_i are the capacitors in the two polyphase networks connected to the input of the OAs, which can be implemented by toggle switched inverter (TSI) branches for the positive transmission factors, or parasitic compensated toggle switched capacitor (PCTSC) branches for the negative transmission factors [10].

ii) For optimum design, the capacitors in the same OA feedback path (for example, B and FB or D and FD) must be dimensioned with similar values [7].

iii) After the set-up of a unit capacitance value, the objective target of the design will be the determination of the minimum capacitance spread that usually imposes also the minimization of total capacitor area.

According to the above characteristics of the design of IIR SC decimators, a novel algorithm for automated design was formulated and developed as a constrained optimization problem with two sequential steps, which can be described as follows.

1) The *first-step* allows the determination of the capacitance values (A, B, C, D, E, FD, FB) in the TIL of the above decimator after defining the *minimizing objective* of the denominator, which implies the formulation of additional nonlinear equality/inequality constraints. Then, the objective and the corresponding constraints that can be obtained for the denominator are

Objective: minimize

$$(B-FB)^2+(D-FD)^2+(C-E)^2 \tag{6-a}$$

Subject to:

$$(B+FB)\cdot(D+FD)=1, \tag{6-b}$$

$$A\cdot(C+E)-(2B\cdot D+B\cdot FD+D\cdot FB) = -2\cos(M\theta_p)\cdot r_p^M, \tag{6-c}$$

$$B\cdot D-A\cdot E=r_p^{2M}, \tag{6-d}$$

$$\{B,\,C,\,D,\,E,\,FB,\,FD\}\le\alpha \tag{6-e}$$

where α is set to be the maximum capacitance value of the set $\{B, C, D, E, FB, FD\}$, while the value of the coupling capacitor (A) is made flexible as an additional degree of freedom, to cope with the requirements of maximum signal handling capability. In the end of the *first-step* all the capacitance values in the TIL have been determined.

2) The *second-step* comprises a nonlinear objective and a series of linear and nonlinear constraints for the practical implementation of the numerator, which can be presented as

Objective: minimize

$$\sum_{i=0}^{M-1+N}(X_i^2-\varepsilon_1)^2+\sum_{i=0}^{M-1+N}(Y_i^2-\varepsilon_2)^2 \tag{7-a}$$

Subject to:

$$\begin{bmatrix} B+FB & & -(C+E) & & \\ & \ddots & & \ddots & \\ -B & & B+FB & E & -(C+E) \\ & \ddots & & \ddots & \\ & & -B & & E \end{bmatrix}\cdot \begin{bmatrix} X_0 \\ \vdots \\ X_{(M-1+N)} \\ Y_0 \\ \vdots \\ Y_{(M-1+N)} \end{bmatrix} = \begin{bmatrix} \overline{a}_0 \\ \vdots \\ \overline{a}_{2(M-1)+N} \end{bmatrix} \tag{7-b}$$

and $-\xi_i\le X_i\le\xi_i$; $-\zeta_i\le Y_i\le\zeta_i$ where $\pm\xi_i$ and $\pm\zeta_i$ are the limits of the coefficients in the input X_i and Y_i branches. On the other hand, ε_1 and ε_2 can be set as the minimum capacitance values from each OA set of the TIL (ε_1 being the minimum of B, FB, C, E, and ε_2 the minimum of A, D, FD, respectively).

After the above two design steps, all the capacitors were dimensioned, and a *first test of the solution* (TEST I), based on the values of α, ξ_i and ζ_i, can be made. Initially, those values are set to allow the implementation of a *feasible solution* (the typical values for fast convergence of the iteration process are $\alpha=50$ and ξ_i and $\zeta_i=10$).

Following the test of the solution an *output simulation* is made, using SWITCAP-II [11]. Here, the values μ_1 and μ_2 are usually determined, having into consideration the maximum amplitude peak levels at each

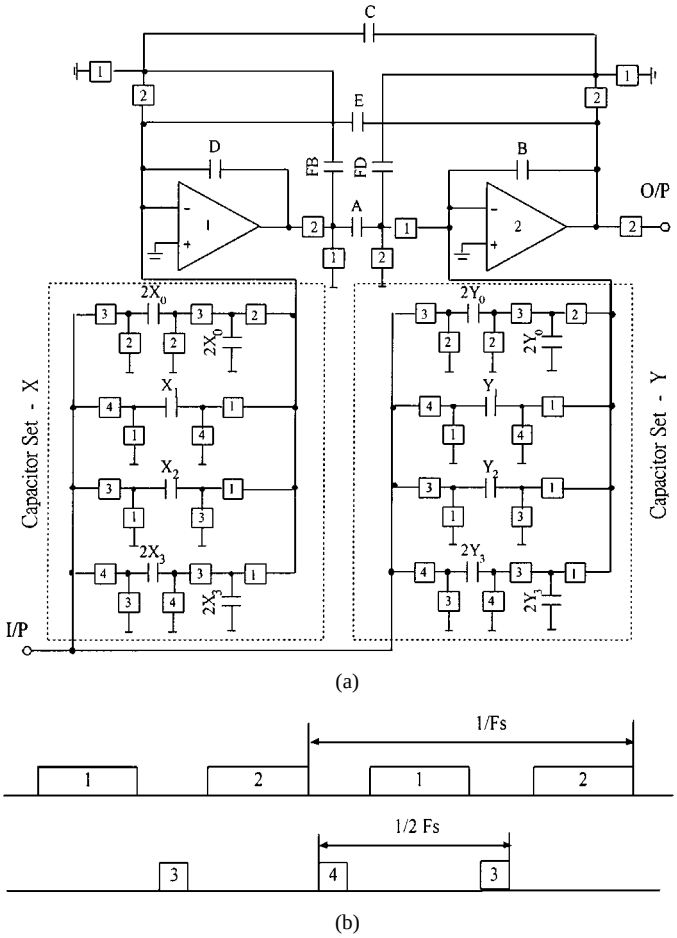

Fig. 2. Second-order IIR SC bandpass-notch decimator with $M=2$. (a) Circuit architecture. (b) Switching waveforms.

TABLE I
COMPARISON OF THE RESULTS OBTAINED BY THE CONVENTIONAL METHOD IN [4] AND THE AUTOMATIC DESIGN METHODOLOGY

Capacitor	Case A in reference [4]	Automatic methodology	
		without iterations	with 8 iterations
A	6.037	7.153	4.006
B	6.076	7.018	4.026
C	3.242	3.138	3.213
D	2.763	2.727	2.727
E	1.696	1.632	1.672
FD, FB	0.000	0.000	0.000
X_0	5.692	6.613	4.143
X_1	1.650	1.974	1.105
X_2	1.000	1.000	1.000
X_3	3.042	3.640	2.039
Y_0	2.027	1.889	2.423
Y_1	1.000	1.000	1.000
Y_2	1.251	1.207	1.389
Y_3	2.473	2.470	2.475
C_{spread}	11.38	13.32 (+17.04%)	8.29 (-27.28%)
Total C	77.65	85.30 (+10.05%)	64.46 (-17.01%)

TABLE II
COMPARISON OF THE RESULTS OBTAINED BY THE CONVENTIONAL METHOD IN [5] AND [6] AND THE AUTOMATIC DESIGN METHODOLOGY

Type	Lowpass decimator with M=3		Lowpass decimator with M=5	
Method	Table III in [5]	Automatic methodology (with a few iterations)	Table I in [6]	Automatic methodology (without iterations)
$\mathbf{C_{spread}}$	18.82	12.94 (-31.26%)	96.02	95.60 (-0.44%)
Total C	78.87	62.64 (-20.57%)	292.62	288.16 (-1.53%)

OA output terminal, which imply the *maximization of the signal handling capability*, according with the definition presented before. After this phase, a *capacitance scaling* using ν_1 and ν_2, is necessary again to ensure a final normalization before the *second test of the solution* (TEST II), that now should have almost reached the *optimum solution* for the application with minimum capacitance spread (if not, a new iteration, namely involving *parameter adjusting*, could be necessary).

For completeness, and based on the basic principle explained before, the above *design methodology* could also be applied for designing higher-order IIR SC decimators. For a given topology of a multistage IIR SC decimator, the design can also be formulated as a linear and nonlinear programming problem to adjust automatically some parameters, while simultaneously keeping the objectives in a simple form [7]. In order to simplify the corresponding constraints, we can set some of the unknown values of the feedback capacitors to a unity value, and make also some capacitor values equal, or zero value in the input branches, if possible.

III. DESIGN EXAMPLES

The above method was applied in the design of the second-order IIR SC bandpass-notch decimator from the reference [4], that reduces the sampling rate from $2F_s = 19.2$ kHz to $F_s = 9.6$ kHz. For the above specifications, and after the automatic design procedure previously described, the circuit structure of the decimator was obtained, as presented in Fig. 2(a) and (b). If the automatic procedure is followed according with the flowchart of Fig. 1, without any iteration (no parameters adjustment), the design method can only lead to a minimum capacitance spread of 13.32 (17.04% higher than the conventional design method [4] as presented in Table I). However, if the automatic procedure includes several iterations with adjustment of some parameters (closed-loop in the flowchart of Fig. 1), namely, 8 iterations in this case, this will lead to the optimum design presented also in Table I, with a minimum capacitance spread of 8.29 (27.28% less than the conventional case [4]).

Brief comparisons were also made with a lowpass decimator with $M = 3$ from [5] and the first stage (also lowpass decimator) with $M = 5$ of the bandpass cascading decimator from [6], and the results are presented in Table II, showing also the achievement of optimum results.

In the above examples it was demonstrated that the proposed automatic design procedure allows the achievement of an optimum solution, for maximum signal handling capability, with minimum capacitance spread and the minimization of the total capacitor area. These examples also show the possibility of achieving even better results than the ones calculated by the conventional trial-and-error method previously used [4]–[6].

IV. CONCLUSION

This brief presents a novel algorithm for the automatic and optimum determination of the capacitor values in IIR SC decimators, which performs the optimization based on defined objectives (linear and nonlinear) and fulfilling multiple design constraints. The iterative and automatic design methodology has two steps process, to dimension the capacitance values that implement the denominator and the numerator, respectively. Several design examples clearly show the efficiency of the automated method, not only by obtaining the minimum capacitance spread and achieving the minimization of the total capacitor area, with the consequent reduction of power consumption, without changing the decimator structure, but also by the capture of the optimum capacitor values with an efficient procedure containing a rather limited number of iterations. This novel method has also been revealed as extremely useful when applied to the design of higher order decimating filters.

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