Letters

A Dual-Output Wireless Power Transfer System With Active Rectifier and Three-Level Operation

Yan Lu, Mo Huang, Lin Cheng, Wing-Hung Ki, Seng-Pan U, and Rui P. Martins

***Abstract*—This letter presents a 6.78 MHz wireless power transfer (WPT) system for wirelessly powered flash drives that need multiple supplies with a total power of sub-1 W. A new architecture that merges an *N*-level single-inductor multiple-output switching converter with a multistage rectifier is proposed for the WPT receiver, and the regulated outputs attain small ripples. A prototype of a 2X active rectifier that merges with a three-level single-inductor dual-output dc–dc converter is implemented in a 0.35 μm CMOS process.**

***Index Terms*—AC–DC power conversion, dc–dc converters, inductive power transmission, rectifiers, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) systems for batteryless and wirelessly charged devices have attracted enormous attention in recent years [1]–[5]. To cut the last wire of the electronic devices, this letter is designed for the wirelessly powered flash memory drives that need multiple supply levels with a total power consumption of sub-1 W.

The concept of *N*-level converter was first used in a high-power inverter [6] to reduce the harmonics of output voltage. A similar idea was then employed in dc–dc converters [7]. Here, *N*-level single-inductor multiple-output (SIMO) converter is incorporated in the low-power WPT system with a $2(N-1)$-stage rectifier, as shown in Fig. 1. Now, any output voltage that has a value between $V_{\mathrm{dc}k}$ and $V_{\mathrm{dc}(k-1)}(k=1,2,\ldots,N)$ can be regulated by sinking currents from these two rectifier outputs through L_3 as a buck converter such that the inductor current and output voltage ripples are reduced. Moreover, the ac input is boosted without introducing the well-known right-half-plane zero that exists in boost and buck–boost converters. Basically, the maximum achievable efficiency of the series–parallel multistage rectifier does not change with the number of stages [8], since all the stages get energy from the ac input in one phase and then being stacked to attain a high V_{dc} in the other phase.

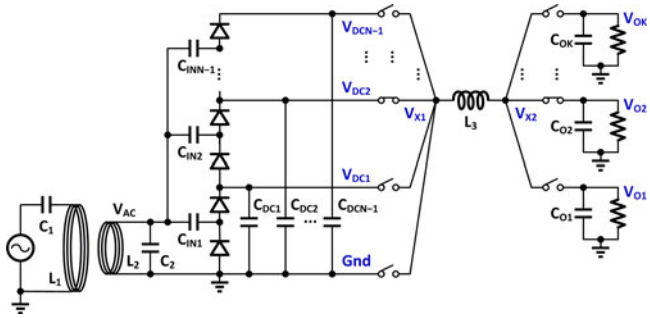

Fig. 1. Generic $2(N-1)$-stage rectifier merged with *N*-level single-inductor multi-input multiple-output converter for WPT systems.

For a wireless power receiver (RX), a direct way to regulate the rectifier output is to cascade a dc–dc converter [4] that needs one more bulky inductor. Thus, the 3R operation was proposed to eliminate one inductor by reusing the RX coil [3]. Instead, a 10 μF flying capacitor was used to regulate the output voltage. In multiple-output scenarios, SIMO techniques were employed to reduce the number of inductors [9], [10].

In this prototype, a three-level single-inductor dual-output dc–dc converter that inherently cooperates with a 2X active rectifier (voltage doubler) is designed for the WPT RX. The system architecture and the building block circuit design are discussed in Section II. Then the experimental results and the conclusions are given in Section III.

II. System Architecture and Circuit Design

As shown in Fig. 2, the three-level dc–dc and the SIMO techniques are merged with a 2X rectifier, which readily has two dc supplies (three-level). When the V_{ac} amplitude is 3.2 V, V_{dc1} will be 2.7 V and V_{dc2} will be 5.5 V. The higher output voltage V_{O2} retrieves current from V_{dc2} and V_{dc1} and can be programmed to range from 3.3 to 5 V for I/O and memory circuits; and the lower output voltage V_{O1} retrieves current from V_{dc1} and Gnd and can be ranged from 1.0 to 1.8 V for core circuits. The SIMO converter switches at the WPT frequency of 6.78 MHz. One benefit of operating the dc–dc converter at

Manuscript received July 22, 2016; accepted August 17, 2016. Date of publication August 19, 2016; date of current version November 11, 2016. This work was supported by the Research Committee of University of Macau under Grant MYRG2015-00107-AMSV and the Macao Science and Technology Development Fund (FDCT).

Y. Lu and M. Huang are with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China (e-mail: yanlu@umac.mo; moorehuang@outlook.com).

L. Cheng and W.-H. Ki are with the ECE Department, The Hong Kong University of Science and Technology, Hong Kong, China (e-mail: lin.cheng@connect.ust.hk; eeki@ust.hk).

S.-P. U is with the State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China (e-mail: benspu@umac.mo).

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China, on leave from the Instituto Superior Técnico, Universidade de Lisboa, Lisboa 1649-004, Portugal (e-mail: rmartins@umac.mo).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2601623

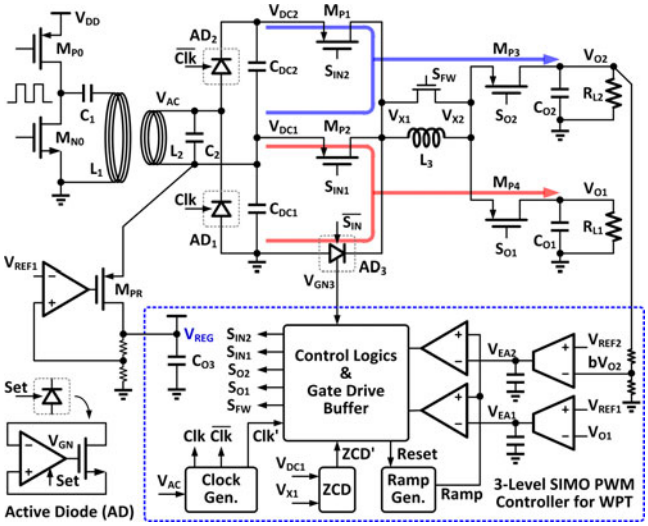

Fig. 2. WPT system with 2× rectifier and three-level SIMO converter.

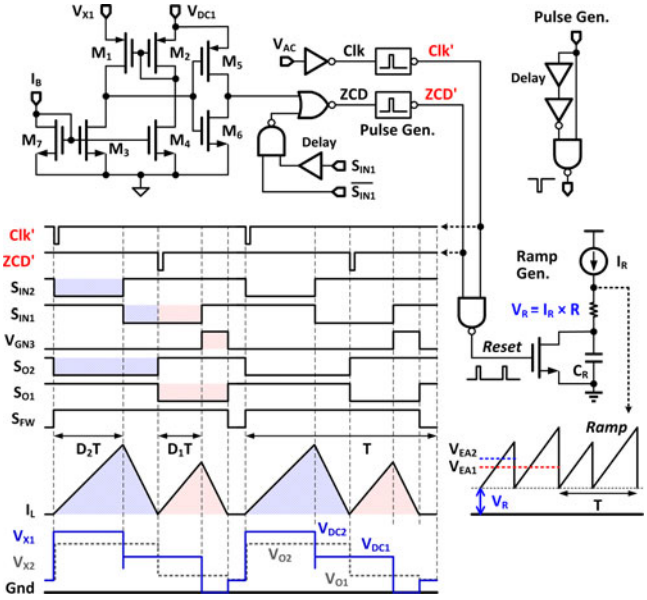

Fig. 3. Timing diagram of the three-level SIMO converter in DCM operation, and the schematics of the clock recovery, ZCD, pulse and ramp generators.

the WPT frequency is that, part of the discontinuous rectifier output currents will directly go to the dc–dc converter inputs in every half cycle, bypassing the rectifier load capacitors $C_{\rm dc1}$ and $C_{\rm dc2}$, further reducing the output ripple. With load resistors R_{L1} and R_{L2} connected in parallel, the equivalent load impedance $R_{L,EQ}$ seen from the RX resonator can be expressed as [11]

$$R_{L,EQ} = (\alpha_{\rm REC} R_{L1}/D_1^2) \parallel (\alpha_{\rm REC} R_{L2}/D_2^2) \qquad (1)$$

where D_1 and D_2 are the voltage conversion ratios of the dual-output three-level converter and $\alpha_{\rm REC}$ is the impedance transformation factor of the rectifier; here, $\alpha_{\rm REC} \approx 1/8$ [12].

The volume of a passive component is roughly proportional to its value (inductance or capacitance). In this letter, smaller L_3 and capacitors can be used, benefiting from the three-level, 6.78-MHz discontinuous conduction mode (DCM) operation. Independent pulsewidth-modulated (PWM) control loops are used for each output, such that cross-regulation can be reduced as long as I_{L3} remains in DCM.

Intuitively, $V_{\rm dc1}$ is a low voltage that can simply be used for the control logics and the gate driving buffer. However, since instantaneous current of the switches and drivers will cause bond-wire induced ringing, a large on-chip decoupling capacitor is needed to filter it. Thus, a low-dropout regulator (LDO) with 120 pF load capacitor is used to smoothen the load current of the controller and to provide a clean $V_{\rm REG}$.

As depicted in Fig. 3, the clock pulse Clk' that initiates the PWM control for V_{O1} is recovered from $V_{\rm ac}$ by an inverter and a pulse generator and the zero current detection (ZCD) signal that determines the connection of V_{X2} is generated by sensing the current of M_{P2}. Since both V_{O2} and V_{O1} need to get current from $V_{\rm dc1}$, M_{P2} is kept on for the output transition period to avoid one-time switching loss of M_{P2} in every cycle. A common-gate input comparator formed by M_1 through M_6 is used to detect the voltage crossing point of V_{X1}. When V_{X1}>$V_{\rm dc1}$ during the ON state of $S_{\rm IN1}$, a pulse ZCD' that initiates the PWM control for V_{O2} swaps the output control signals S_{O2} and S_{O1}. To compensate the delay of the gate drive buffer, an artificial offset is designed into the comparator by tuning the sizes of M_5 and M_6. For fast speed, the quiescent current of the comparator is about 60 μA. Alternatively, the speed requirement on the ZCD can be relaxed by using an additional slow autocalibration loop to adjust the comparator offset, as demonstrated in [13]. Since the calibration loop only requires a low bandwidth, for example, 200 kHz in [13], its current consumption is only in the order of 1 μA.

When both M_{P1} and M_{P2} are off during the transition period between $S_{\rm IN1}$ and $S_{\rm IN2}$, large glitches on V_{X1} can occur during this dead-time period, and additional logics are used to prevent malfunctioning of the switches.

A simple and effective ramp generator is proposed for the SIMO converter, as shown in Fig. 3. The capacitor C_R for the ramp is charged up by a constant current I_R and is discharged by a switch triggered by either Clk' or ZCD'. To satisfy the output range of the error amplifiers (EAs), the ramp signal is shifted up by V_R that is the voltage drop on the resistor.

Good rectifier efficiencies were achieved in [3] with Schottky diodes that are not available in a standard CMOS process, while CMOS active rectifiers have lower cost with comparable efficiency at relatively lower power levels [2]. Fig. 4 shows the schematics of the N-type active diode (AD) for $\rm AD_1$ and $\rm AD_3$, and the P-type $\rm AD_2$ in Fig. 2. The common-gate input pairs $M_1 - M4$ in the N-type AD compare $V_{\rm ac}$ and Gnd, and in the P-type AD, they compare $V_{\rm ac}$ and $V_{\rm dc2}$. M_9 and M_{10} provide additional currents to generate an input offset for reverse current control (RCC), and the strategy is to turn off the power MOS earlier to compensate for the comparator delay and the buffer delay. The RCC switches will be kept on for half cycle and then be reset in the subsequent half cycle to prevent multiple pulsing of the gate voltage [14]. Further, large on-chip $V_{\rm ac}$ glitches induced by bond wires can also turn on the active diodes multiple times in one half cycle. To reduce $V_{\rm ac}$ glitches, two on-chip

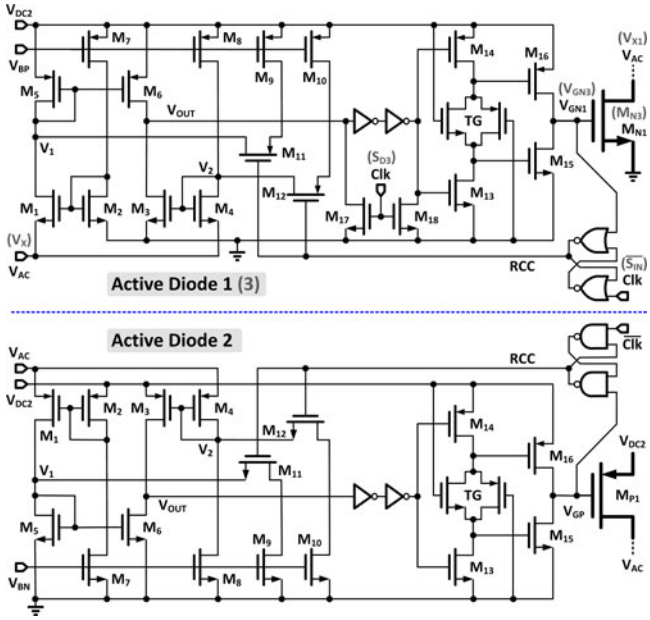

Fig. 4. Schematics of the active diodes.

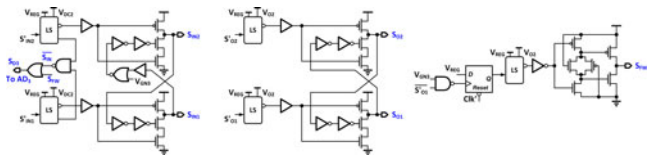

Fig. 5. Gate drive circuits for $S_{\rm IN2}$, $S_{\rm IN2}$, S_{O2}, S_{O1}, and $S_{\rm FW}$.

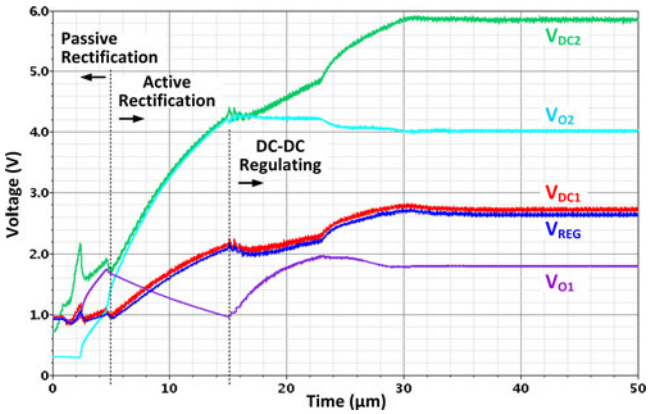

Fig. 6. Simulated start-up process of the WPT receiver.

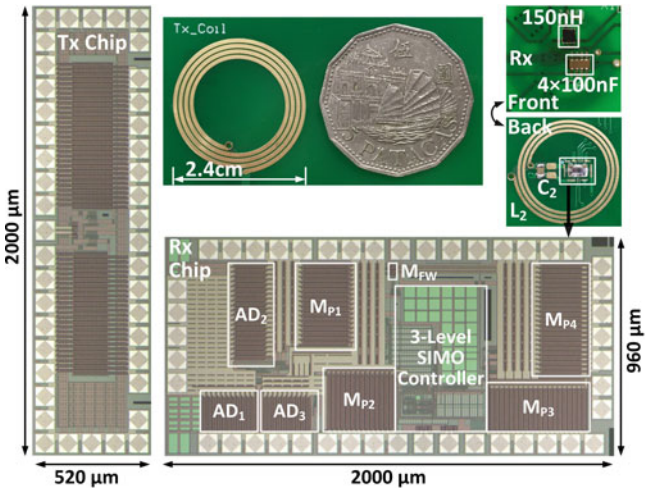

Fig. 7. Chip micrographs and off-chip components of the proposed system.

capacitors of 50 pF each are added between $V_{\rm ac}$ and $V_{\rm dc2}$ and $V_{\rm ac}$ and Gnd, respectively.

The gate drive circuits for $M_{P1}-M_{P4}$ and $S_{\rm FW}$ are shown in Fig. 5. The input signals of the buffers come from the control logics and are not shown for the sake of simplicity. The freewheel switch $S_{\rm FW}$ will be turned on at the end of each cycle when both $\rm AD_3$ and M_{P4} are off, to suppress the possible ringing caused by L_3 and the parasitic capacitors on V_{X1} and V_{X2} nodes when they are floating [15]. The three-transistor-based inverters [16] are employed to eliminate the short-circuit current of the buffers driving $M_{P1}-M_{P4}$ and to avoid M_{P1} (M_{P3}) and M_{P2} (M_{P4}) being ON simultaneously. By doing so, M_{P2} can only be turned on after M_{P1} is off, and similarly, M_{P4} can only be turned on after M_{P3} is off. A transmission gate (TG) is added to the second last buffer stages of the ADs and $S_{\rm FW}$, to reduce the short-circuit current of the last two stages. If one of M_{P1}, M_{P2}, and $S_{\rm FW}$ is ON, a signal S_{D3} is fed to the shutdown (SD) pin of $\rm AD_3$ to disable it.

Fig. 6 shows the simulated start-up process of the proposed WPT RX with $R_{L1}=100\ \Omega$ and $R_{L2}=200\ \Omega$. There are three operation regions within the start-up process: at the very beginning, the parasitic passive rectifier will operate first and charge up the output voltages to relatively low levels [4], [14]; then, the active rectifier will take over to continue the charging of the load capacitors; finally, when the rectifier outputs are good enough for the three-level SIMO operation, regulated output voltages can be provided.

III. Experimental Results

The WPT system was fabricated in a 0.35 μm CMOS process using both 5 and 3 V devices, and it was measured with the PCB coils shown in Fig. 7. A transmitter (TX) chip consists of a single-ended Class-D power amplifier driving a series *LC* resonant tank at 6.78 MHz was also fabricated for testing. The chip areas of the WPT TX and RX are 1.04 and 1.92 mm^2, respectively. The inductances of L_1 and L_2 are 573 and 225 nH, with outer diameters of 2.4 and 1.6 cm, and their matching capacitors C_1 and C_2 are 0.96 and 2.4 nF, respectively. Fig. 8 shows the measured waveforms of the RX with coil distance of 5 mm. The regulated outputs V_{O1} and V_{O2} exhibit much lower ripples when compared to the unregulated outputs $V_{\rm dc2}$ and $V_{\rm dc1}$. The current of the shielded L_3 of 150 nH is measured with a high-bandwidth ac current probe. The measured output voltage ripples are smaller than 120 mV for all outputs at a total output power of 0.5 W. Besides the *LC* resonant tank, off-chip components of only one 2 $\times$ 2 mm^2 miniature power inductor L_3 and one 1.6 $\times$ 3.2 mm^2 capacitor array (which houses 4 $\times$ 100 nF capacitors) are used. All core circuits are

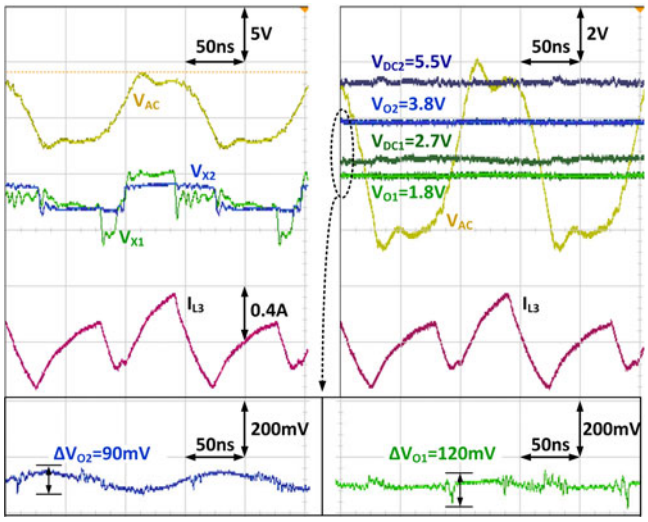

Fig. 8. Measured voltage and inductor current waveforms of the WPT RX.

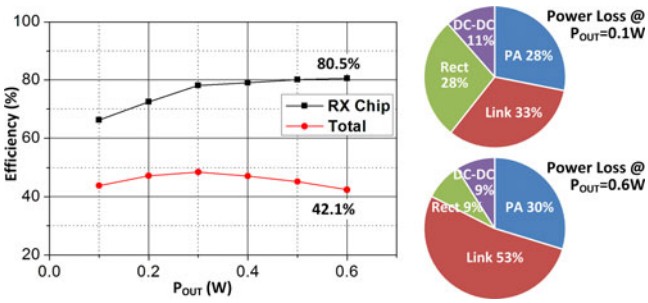

Fig. 9. Efficiency curves versus output power, and power loss breakdown.

TABLE I
COMPARISON WITH STATE-OF-THE-ART WPT WORKS

	[2]	[3]	[4]	This Letter
Process (μm)	0.35 CMOS	0.35 BCD	0.18 BCD	0.35 CMOS
Receiver Topology	1X/2X Rect.	3R	Rect. + Buck + 3-LDOs	2X Rect. + three-level SIMO
Rectifier Type	Active	Passive	Active	Active
F_{WPT} (MHz)	13.56	6.78	6.78	6.78
F_{PWM} (MHz)	N/A	0.848	2	6.78
No. Regulated (Unreg.) V_o	0 (1)	1 (0)	4 (1)	3 (2)
Passives for Regulation	N/A	$C = 10\ \mu$F	LC: Not rated	$L = 150$ nH
RX Chip Area (mm^2)	1.41	5.52	12.25	1.92
$P_{\mathrm{OUT,Max}}$ (W)	0.032	6	6	0.6
Eff. RX Chip	84.2%	86%	80.86%	80.5%
Eff. Total	N/A	55%	N/A	42.1%
C_{Load} (nF)	4	20 000	Not rated	100
Ripple (mV)	210	~120*	Not rated	120

Estimated from figure.

within the area of the RX coil. Fig. 9 shows the efficiency curves versus P_{OUT} and the power loss breakdown at $P_{\mathrm{OUT}} = 0.1$ and 0.6 W, respectively.

Performance comparison with state-of-the-art WPT works is listed in Table I. With the proposed architecture, three regulated outputs (including V_{REG}) are provided. The two unregulated outputs can further be cascaded by LDOs to realize more customized supply rails. Small output ripples are achieved with only 100-nF output capacitors. The power-handling capability of the dc–dc converter in DCM can be increased by decreasing its switching frequency [10].

IV. CONCLUSION

A highly integrated three-level single-inductor dual-output dc–dc cooperating with a 2X active rectifier is proposed for the WPT RX and is measured with PCB coils. Dual regulated outputs with small voltage ripples are achieved with only one capacitor array and a miniature-sized inductor.

REFERENCES

[1] V. Valente, *et al.*, "A high-power CMOS class-D amplifier for inductive-link medical transmitters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4477–4488, Aug. 2015.
[2] Y. Lu, *et al.*, "A 13.56 MHz fully integrated 1X/2X active rectifier with compensated bias current for inductively powered devices," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 66–67.
[3] J.-H. Choi, *et al.*, "Resonant regulating rectifiers (3R) operating for 6.78 MHz resonant wireless power transfer (RWPT)," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2989–3001, Dec. 2013.
[4] H. Park, *et al.*, "A design of a wireless power receiving unit with a high-efficiency 6.78-MHz active rectifier using shared DLLs for magnetic-resonant A4 WP applications," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4484–4498, Jun. 2016.
[5] K. Tomita, *et al.*, "1-W 3.3–16.3-V boosting wireless power transfer circuits with vector summing power controller," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2576–2585, Nov. 2012.
[6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.
[7] F. Zhang, F. Z. Peng, and Z. Qian, "Study of the multilevel converters in DC-DC applications," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Jun. 2004, pp. 1702–1706, vol. 2.
[8] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 153–166, Jan. 2007.
[9] D. Ma *et al.*, "Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 89–100, Jan. 2003.
[10] X. Jing, P. K. T. Mok, and M. C. Lee, "A wide-load-range constant-charge-auto-hopping control single-inductor-dual-output boost regulator with minimized cross-regulation," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2350–2362, Oct. 2011.
[11] W. X. Zhong and S. Y. R. Hui, "Maximum energy efficiency tracking for wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 4025–4034, Jul. 2015.
[12] K. Van Schuylenbergh and R. Puers, *Inductive Powering: Basic Theory and Application to Biomedical Systems*. The Netherlands: Springer, 2009.
[13] L. Cheng, W. H. Ki, Y. Lu, and T. S. Yim, "Adaptive on/off delay-compensated active rectifiers for wireless power transfer systems," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 712–723, Mar. 2016.
[14] Y. Lu and W.-H. Ki, "A 13.56 MHz CMOS active rectifier with switched-offset and compensated biasing for biomedical wireless power transfer systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 3, pp. 334–344, Jun. 2014.
[15] D. Ma, W.-H. Ki, and C. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1007–1014, Jun. 2003.
[16] C. Yoo, "A CMOS buffer without short-circuit power consumption," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 9, pp. 935–937, Sep. 2000.