Active–Passive $\Delta\Sigma$ Modulator for High-Resolution and Low-Power Applications

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***Abstract*— This paper discusses the use of a low gain amplifier and a passive switched-capacitor (SC) network to enable the SC integrator function. The method is applied to a delta-sigma modulator to achieve high resolution as proved by the 65-nm CMOS technology test vehicle. Compared with the conventional operational amplifier (op-amp)-based SC integrator, this solution utilizes a low-gain open-loop amplifier to drive a passive SC integrator with positive feedback. Since the open-loop amplifier requires a low dc gain and implements an embedded current adder, the power consumption is very low. Power reduction for single bit is obtained by using passive feedforward with built-in adder to assist the first amplifier. The low swing obtained at the output of the active blocks relaxes the slew rate requirement and enhances the linearity. Implemented in 65-nm digital CMOS technology with an active area of 0.1 mm^2, the test chip achieves a dynamic range of 91 dB, peak signal-to-noise ratio of 88.4 dB, peak signal-to-noise-plus-distortion ratio of 88.2 dB, and a spurious free dynamic range of 106 dB while consuming 73.6 μW in a 25-kHz signal bandwidth at 1 V supply, yielding a FoM$_{\text{Walden}}$ of 70 fJ/conv-step and FoM$_{\text{Schreier}}$ of 176 dB.**

***Index Terms*— Delta-sigma modulator ($\Delta\Sigma$M), discrete time (DT), low-gain-amplifier-based switched-capacitor (SC) integrator, noise shaping, passive SC integrator.**

I. Introduction

THE increasing demand for audio devices for portable or autonomous apparatuses used in daily life continues to drive the need for highly power-efficient data converters with high resolution. Delta-sigma modulators ($\Delta\Sigma$Ms) are the preferred solution and the ones based on switched capacitor (SC) are optimal for low power medium conversion speed because of their accurate setting of zeros of the noise transfer function (NTF) and their insensitivity toward clock jitter and process [1]. As is well known, $\Delta\Sigma$M demands using one operational amplifier (op-amp) per zero of the NTF and this results in relatively high power consumption, which becomes a limitation in many applications [2], [3]. Sharing the op-amp [4] and special techniques [5]–[7] reduces the number of active blocks but performance requests become more severe. Even the use of a passive $\Sigma\Delta$ modulator [8]–[12], consisting of switches, capacitors, and quantizer only, reduces the power. However, the passive operation causes a loss in the NTF that reduces the signal-to-noise ratio (SNR) and attenuates the signal along the architecture, thus making the thermal noise dominant [10]. To overcome the reduced loop gain problem in the passive $\Sigma\Delta$ modulator, several active–passive hybrid implementations were presented [13]–[17]. A fourth-order continuous-time (CT) active–passive modulator employs two amplifiers with passive networks to achieve a high SNR. The active stage utilizes a fully functional op-amp which has stringent requirements and leads to a high power consumption [13]. A fifth-order CT hybrid active–passive modulator which uses three high power active integrators and two passive integrators, and which also employs a low-gain preamplifier with a dynamic comparator, can only achieve a 10-b resolution [14]. A third-order discrete-time (DT) active–passive modulator utilizes a power hungry G_m-C integrator in the second stage and a passive integrator in the first and third stages; besides, it also uses a preamplifier in front of the comparator. Because of the inability to define an accurate NTF, zeros from the passive integrators and the thermal noise limit the $\Delta\Sigma$M to 9-b resolution [15]. A fourth-order DT $\Delta\Sigma$M which uses first an active integrator followed by three passive SC integrators to relax the loop gain requirement utilizes a simple dynamic comparator to achieve 13 b (with only simulated results provided) [16]. It was recently reported that in a 2-1 MASH CT active–passive $\Delta\Sigma$M that was implemented in 65-nm CMOS the first stage utilizes two passive integrators with a simple differential amplifier. The small signal swing allows the comparator to be used as a gain stage and relaxes the loop gain requirement, but an inaccurate time constant leads to the limitation represented by an 11.6-b resolution with a power dissipation of 1.57 mW [17].

None of the active–passive modulators presented in the literature improves the traditional passive SC integrator structure for better noise shaping in the $\Delta\Sigma$M.

Manuscript received January 18, 2016; revised April 17, 2016; accepted June 1, 2016. Date of publication July 7, 2016; date of current version December 26, 2016. This work was supported in part by the Research Committee within the University of Macau and Macao Science and Technology Development Fund under Grant SKL/AMS-VLSI/SSW/13-Y3/FST.

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Digital Object Identifier 10.1109/TVLSI.2016.2580712

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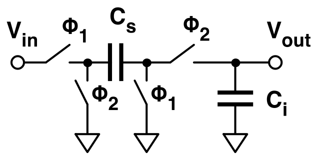

Fig. 1. Passive SC integrator.

This paper considers hybrid solutions that use active functions to compensate for the limits of the passive operation. It uses three techniques for reducing power consumption. The main one consists of using a forward gain K and a positive feedback across a passive SC integrator. The method needs a gain stage though. Second, its required low gain is attained with a circuit that embeds the positive feedback. Since the amplifier includes a built-in adding function for superposing the signal and the feedback path, the power required is very low. Third, power reduction for a single-bit modulator is proposed with feedforward and built-in adder to assist the first amplifier. This improves the linearity and relaxes the slew rate requirements. Since gain and speed requirements are relaxed, the resulting power consumption is very competitive.

A test vehicle made using a third-order single-bit $\Delta\Sigma$M experimentally verifies the proposed method. The technology used is a 65-nm CMOS. After the introduction, Section II describes the integrator with a low-gain amplifier. Section III focuses on the system-level architecture for an active–passive integrator in a higher order $\Delta\Sigma$M. Section IV describes the test vehicle and its integrated SC realization. Section V provides measurement results. Section VI summarizes the paper's conclusions.

II. Integrator With Low-Gain Amplifier

The integrator that grants the lowest consumed power is the passive SC implementation shown in Fig. 1. It does not drain power from V_{DD} being an equivalent RC network but the transfer function is not one of the ideal integrators $H_I = z^{-1}/(1 - z^{-1})$ used in $\Delta\Sigma$Ms. The transfer function $H_P = \alpha z^{-1}/[1 - (1 - \alpha)z^{-1}](\alpha = C_s/(C_s + C_i)$ implies a gain error and a phase error. The gain error is important because it causes signal attenuation and this leads to a more critical noise performance. However, the phase error is more problematic because it denotes a shift of the integrator pole inside the unity circle [10]. As a result, the NTF becomes flat at low frequencies, thus affecting the maximum achievable SNR, especially for high oversampling ratios.

A technique that employs a positive feedback across the passive SC integrator can compensate for the phase error [18]. Moreover, with forward gain K, it is possible to attenuate the gain error. Fig. 2(a) illustrates the block diagram of the method. The circuit analysis yields

$$\frac{V_{\text{out}}}{V_{\text{in}}} = H(z) = \frac{K\alpha z^{-1}}{[1 - z^{-1} + \alpha(1 - \beta)z^{-1}]}. \qquad (1)$$

Here $\beta = 1$ makes the integrator transfer function ideal in terms of elimination of the phase error. However, since $\beta > 1$ would bring the pole of $H(z)$ into the region of instability, it is necessary to ensure a proper margin in a real implementation.

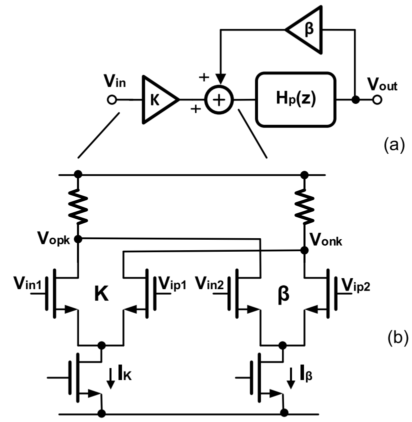

Fig. 2. (a) Compensation technique model. (b) Circuit implementation.

The circuit realizing the forward gain and feedback branch consumes power. However, it can be very simple: the parallel connection of two differential pairs with resistive load can obtain the result, as shown in Fig. 2(b). The currents and the aspect ratio of transistors determine the value of β and K. The value of the currents used in the circuit of Fig. 2(b) determines the required bandwidth. Since K can be as low as 14–16 dB, the resulting low value of load resistance, even with a very small value of the bias current I_K, generates a large bandwidth thanks to the small used capacitive loads.

The circuit of Fig. 2(b) has a limited region of linearity because the overdrive voltage of the input differential pair is quite low for very small bias currents. In order to ensure good spurious free dynamic ranges (SFDRs), it is therefore necessary to limit the swing of the input differential voltage. This, as will be discussed, can be achieved by architectures that ensure a low swing at the input of each active–passive integrator.

The gains of the branches of the circuit of Fig. 2(b) are $K = g_{mK}R_L$ and $\beta = g_{m\beta}R_L$, where g_{mK} and $g_{m\beta}$ are the transconductances of the two differential pairs. Since transconductance and resistance depend on technological parameters, the accuracy of the two gains is limited. The value of K is not critical but the value of β must be equal to 1 in order to obtain the required compensation. Since its value is inaccurate, it is necessary to account for its spread in the design circuits that use the active–passive scheme.

III. Active–Passive Integrator in a High Order $\Delta\Sigma$ Modulator

An active–passive integrator that replaces a conventional integrator in $\Delta\Sigma$ architecture greatly reduces the consumed power. The scheme of Fig. 2(b) uses just 10% (22 μW with an $f_T = 150$ MHz, 0.2-pF load) of the power consumed by a conventional two-stages amplifier designed with the same technology (CMOS 65 nm) granting an equal unity gain frequency. This power reduction is such that the amount needed by the active–passive integrator almost equals that of the comparator (21 μW including a preamplifier).

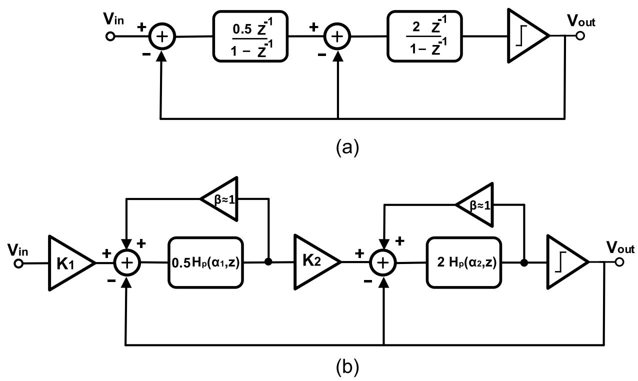

Fig. 3. (a) Second-order $\Delta\Sigma$M. (b) Implementation with active–passive integrators.

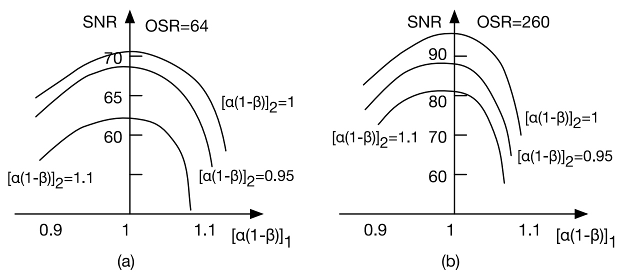

Fig. 4. (a) SNR versus the $\alpha(1-\beta)$ parameter of the first integrator at OSR $=64$. (b) SNR versus the $\alpha(1-\beta)$ parameter of the first integrator at OSR $=260$.

The conventional second-order architecture of Fig. 3(a) becomes the scheme of Fig. 3(b) with the coefficients 1/2 and 2 incorporated in the H_p blocks. The value of K_1 and K_2 should be equal to $1/\alpha_1$ and $1/\alpha_2$, respectively, but the gain in the first integrator cannot be greater than 1 because it would affect the input dynamic range and, in addition, the active block would operate in a nonlinear region. The α_1 attenuation can be compensated together with α_2 but the resulting gain can become large. A compromise solution is to admit some attenuation that, in turn, reduces the SNR. The power consumption of the second-order active–passive $\Delta\Sigma$M would diminish by a factor of 7 compared with second-order active modulator, as shown in Fig. 3(a). However, the inaccuracy of the parameter β caused by the technology implementation degrades the performance. Since the value of β cannot exceed 1, its designed value must account for possible technological spread. Since the nonzero value of the $\alpha(1-\beta)$ coefficient causes a loss, in order to compensate for the limit, the oversampling ratio (OSR) must increase. This requires active blocks with higher f_T. Therefore, the equivalent power benefit becomes less than what was expected. The inaccuracy of the two β coefficients dominates loss and consequently causes a drop in the SNR. On the other hand, the accuracy of the K coefficients is not very critical.

Behavioral simulations of the second-order active–passive $\Delta\Sigma$M of Fig. 3(b) give rise to the diagrams of Fig. 4. It plots the SNR versus the parameter $\alpha(1-\beta)$ of the first active–passive integrator for three different values of the same parameter of the second integrator. Considering OSR $=64$, the drop of the SNR is about 6 dB for $\alpha(1-\beta)=0.9$ and the

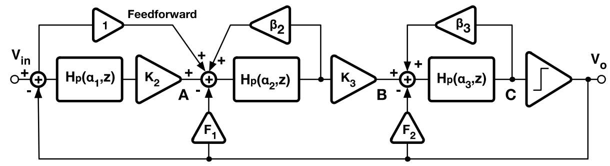

Fig. 5. Block diagram of a third-order active–passive $\Delta\Sigma$M.

second integrator is ideal. Moreover, the modulator is stable even for $\alpha(1-\beta)>1$ until about 1.14. The situation is worse for the nonideal behavior of the second integrator. The drop is much higher when the OSR becomes large (OSR $=260$), as shown in Fig. 4(b).

The gains of the simple circuit of Fig. 2(b) are determined by products $g_m R$, with g_m being the transconductance of the differential pair and R the resistive load. Since the two parameters are technologically independent, the inaccuracies are quadratically superposed. The resulting inaccuracy can be 20%. Therefore, also accounting for the results of Fig. 4, a safe choice would be $\beta=0.9$, with a nominal improvement of the position of the pole of the approximate integrator by a factor of 10. In order to augment accuracy, a diode-connected n-channel transistor can replace the resistive load, provided that a small output swing keeps the operation of the circuit in the linear region.

A. Third-Order Active–Passive $\Delta\Sigma$ Modulator

An active–passive integrator in a second-order $\Delta\Sigma$M potentially achieves excellent power performance but the SNR reductions caused by variations in technology parameters can be problematic. Improving the SNR with higher OSRs causes a quadratic increase in power in active blocks. Multibit quantizers need more comparators: the additional power consumed impedes power effectiveness. Also due to the active–passive integrator, the signal swings inside the loop filter become very small. Its low value in front of the quantizer makes implementing a multibit operation rather difficult.

Using a supplementary passive integrator as the first stage adds a zero in the NTF and increases by one the order of the modulator formally. In order to make the solution beneficial, the new zero must be just inside the z-domain unity circle, and for this, a very low time constant equivalent RC network is required. However, the passive integrator causes signal attenuation to be compensated with the gain block of the successive stage. Fig. 5 shows the behavioral diagram of the resulting third-order active–passive modulator. The scheme also uses a feedforward path, bringing the input signal to the input of the second passive integrator, which corrects the position of the signal transfer function (STF) poles. Moreover, the output signal that feeds back to the input of the third passive integrator is attenuated (the factor F_2 is less than 1) to match the low swing at the output of the block K_3.

The transfer function from the input of the block $H_P(\alpha_1, z)$ to node A is

$$H_A(z)=\frac{\alpha_1 K_2 z^{-1}}{[1-(1-\alpha_1)z^{-1}]}=\frac{\alpha_1 K_2 z^{-1}}{[1-b_1 z^{-1}]} \tag{2}$$

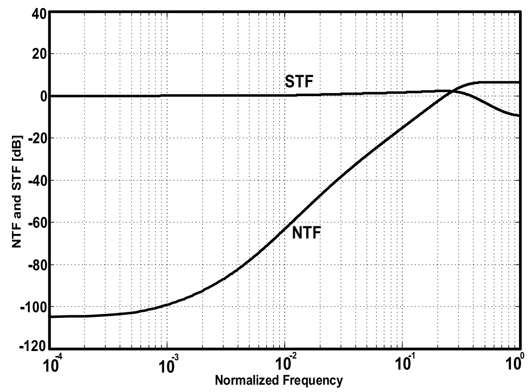

Fig. 6. STF and NTF of the modulator.

TABLE I
MATLAB MODEL DESIGN PARAMETERS

Parameter	Value
Amplifier K_2 Gain	6
Amplifier K_3 Gain	5
Adder β_2 Gain	1.2
Adder β_3 Gain	1.25
First Passive Integrator (α_1)	0.01
Second Passive Integrator (α_2)	0.01
Third Passive Integrator (α_3)	0.055
First Intgerator Feedback	1
Second Integrator Feedback (F_1)	1
Third Integrator Feedback (F_2)	0.1
Quantizer gain G	47 dB

where $b_1 = 1 - \alpha_1$. The transfer function from the input of the block H_P (α_2, z) to node B is

$$H_B(z) = \frac{\alpha_2 K_3 z^{-1}}{[1 - z^{-1} + \alpha_2(1 - \beta_2)z^{-1}]} = \frac{\alpha_2 K_3 z^{-1}}{[1 - b_2 z^{-1}]} \tag{3}$$

where $b_2 = [1 - \alpha_2(1 - \beta_2)]$. The transfer function from the input of the block H_P (α_3, z) to node C is

$$H_C(z) = \frac{\alpha_3 z^{-1}}{[1 - z^{-1} + \alpha_3(1 - \beta_3)z^{-1}]} = \frac{\alpha_3 z^{-1}}{[1 - b_3 z^{-1}]} \tag{4}$$

where $b_3 = [1 - \alpha_3(1 - \beta_3)]$. The (2), (3), (4) transfer functions and the block diagram with linear quantizer gain G of Fig. 5 yield

$$[\{(V_{\text{in}} - V_o)H_A + V_{\text{in}} - F_1 V_o\}H_B - F_2 V_o]GH_C + \varepsilon_Q = V_o. \tag{5}$$

This determines the STF and the NTF

$$\text{STF}(z) = \frac{z^{-2}[1 + \gamma z^{-1}]}{[1 + \delta_1 z^{-1} + \delta_2 z^{-2} + \delta_3 z^{-3}]} \tag{6}$$

$$\text{NTF}(z) = \frac{[1 - \alpha_1 z^{-1}][1 - \alpha_2 z^{-1}][1 - \alpha_3 z^{-1}]}{[1 + \delta_1 z^{-1} + \delta_2 z^{-2} + \delta_3 z^{-3}]} \tag{7}$$

where the γ and δ coefficients depend on the modulator parameters. The task of the designer is to ensure stability and maximize the SNR for the chosen oversampling ratio. Indeed, a third-order architecture is not always stable when a single comparator is used. Using suitable attenuation factors along the chain can ensure stability. This is what we have naturally with passive SC approximate integrators. It is also necessary to use suitable gain factors K_2 and K_3 that increase the signal levels for making the thermal noise limit negligible.

There is a complex dependence of the SNR on the design parameters and the optimal set can be determined by recursive behavioral simulations. The goal is to have a maximum SNR and minimum sensitivity due to a variation in parameters. According to the linear model of the quantizer, it is working as a gain stage with gain G. The equivalent gain G of the quantizer is defined as the ratio of its output root-mean-square (rms) value to its input rms value. Since ΔΣM is a nonlinear system, this gain G can only be determined by simulation. The set of parameters reported in Table I leads to

$$\text{STF}(z) = \frac{z^{-2}(0.68 - 0.64z^{-1})}{[1 - 1.63z^{-1} + 0.96z^{-2} - 0.28z^{-3}]} \tag{8}$$

$$\text{NTF}(z) = \frac{[1 - 3.01z^{-1} + 3.01z^{-2} - 1.006z^{-3}]}{[1 - 1.63z^{-1} + 0.96z^{-2} - 0.28z^{-3}]}. \tag{9}$$

The denominators denote three poles where the real is located at $z = 0.92$. It is close to $z = 1$ and reduces the benefit of the NTF by a factor of 12.5, and it also affects

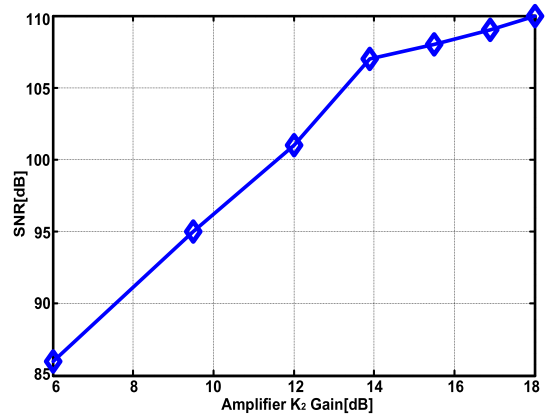

Fig. 7. SNR versus K_2 gain.

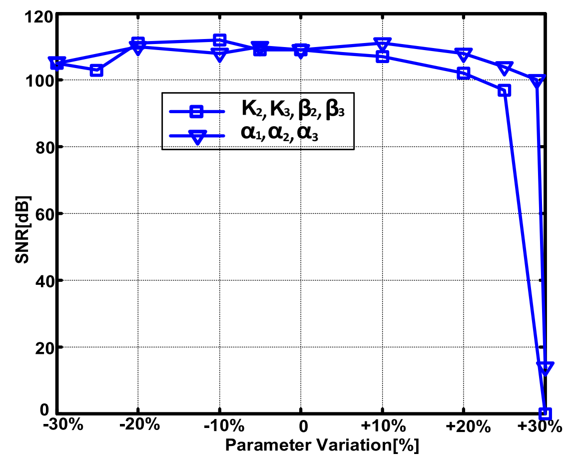

Fig. 8. SNR sensitivity to parameter variation.

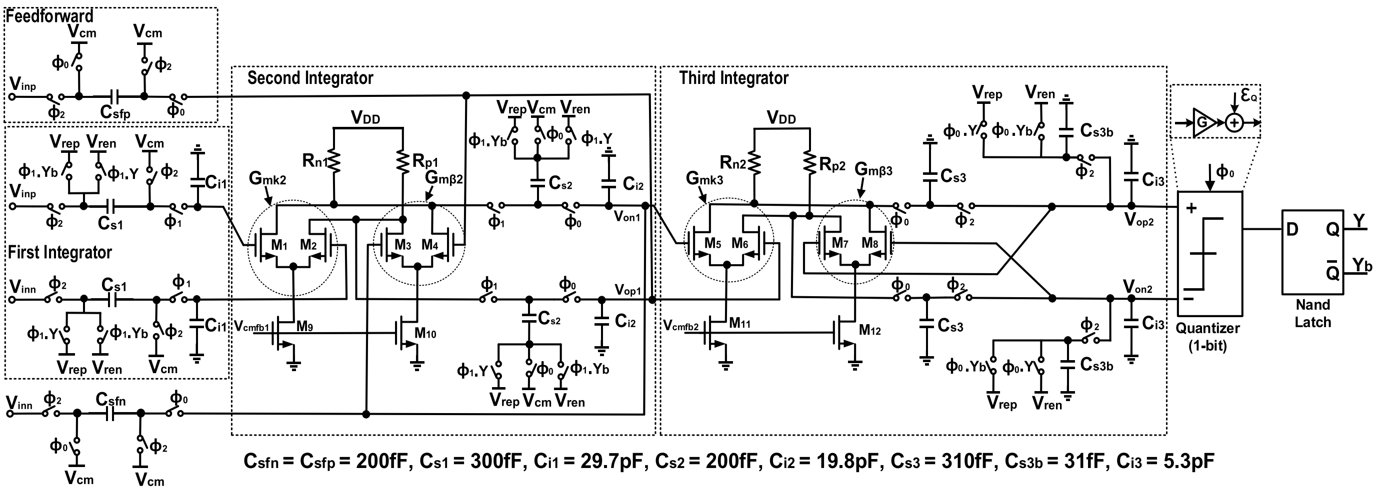

Fig. 9. Fully differential SC implementation with linear quantizer model (with gain G and quantization noise ε_Q).

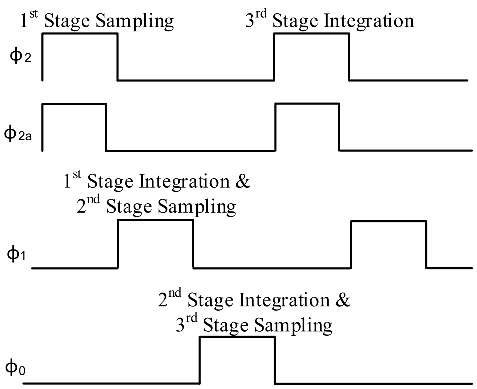

Fig. 10. Three phase timing operation.

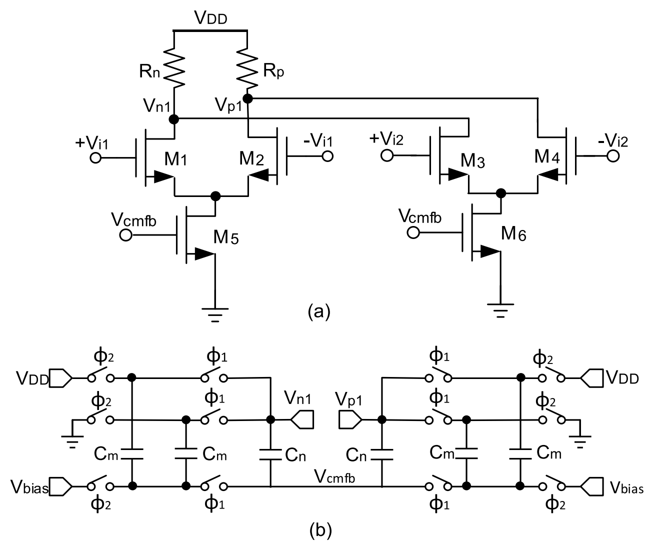

Fig. 11. (a) Amplifier with current adder. (b) Common mode feedback circuit.

the STF. However, the STF has a zero at $z = 0.865$ that almost neutralizes the real pole. The complex conjugate poles of the denominators are at $z = 0.356 \pm j0.423$, relatively far away from $z = 1$. The zeros of the NTF are around $z = 1$; the product of their distances from $z = 1$ is 2.7×10^{-7}. The resulting NTF at $z = 1$, accounting for the attenuation of all the poles, is -105 dB. Fig. 6 displays both NTF and STF to outline the above-discussed features.

The modulator parameters of Table I give rise to SNR = 107 dB with OSR = 260. This value is about 18 dB higher than that of an active–passive second-order modulator with the same OSR and 11 dB higher than that achieved using ideal integrators. The power benefit of this modulator is almost the same as that of the active–passive second-order modulator.

B. Noise Performance

The noise of the first integrator dominates noise performance because the noise of the later stages is suppressed by the gain of the preceding integrators. Therefore, the performance depends on the kT/C power of the sampling capacitor divided by the oversampling ratio [19]–[21]. If C_{s1} is the sampling capacitor of a fully differential scheme, the in-band kT/C noise caused by the sampling capacitance C_{s1} is

$$V_n^2 = \frac{4kT}{C_{s1}\mathrm{OSR}}. \tag{10}$$

TABLE II

SUMMARY OF THE AMPLIFIERS AND ADDERS' PARAMETERS

Parameter	Amplifier 1	Amplifier 2
DC gain of the Amplifier	15.6 dB	14.7 dB
GBW of the Amplifier	145 MHz	126 MHz
G_m of the Amplifier	196 μS	175 μS
DC gain of the Adder	4.2 dB	5.8 dB
GBW of the Adder	31 MHz	41 MHz
G_m of the Adder	53 μS	63 μS

This accounts for the sampling and injection phase of the two sampling paths.

Supposing that V_{FS} is the full-scale voltage and $\bar{n}$ is the target bit, the value of C_{s1} that gives rise to a noise voltage equal to half least-significant-bit (LSB) is

$$C_{s1} = \frac{4 \cdot k \cdot T \cdot 2^{2\bar{n}}}{V_{\mathrm{FS}}^2 \mathrm{OSR}}. \tag{11}$$

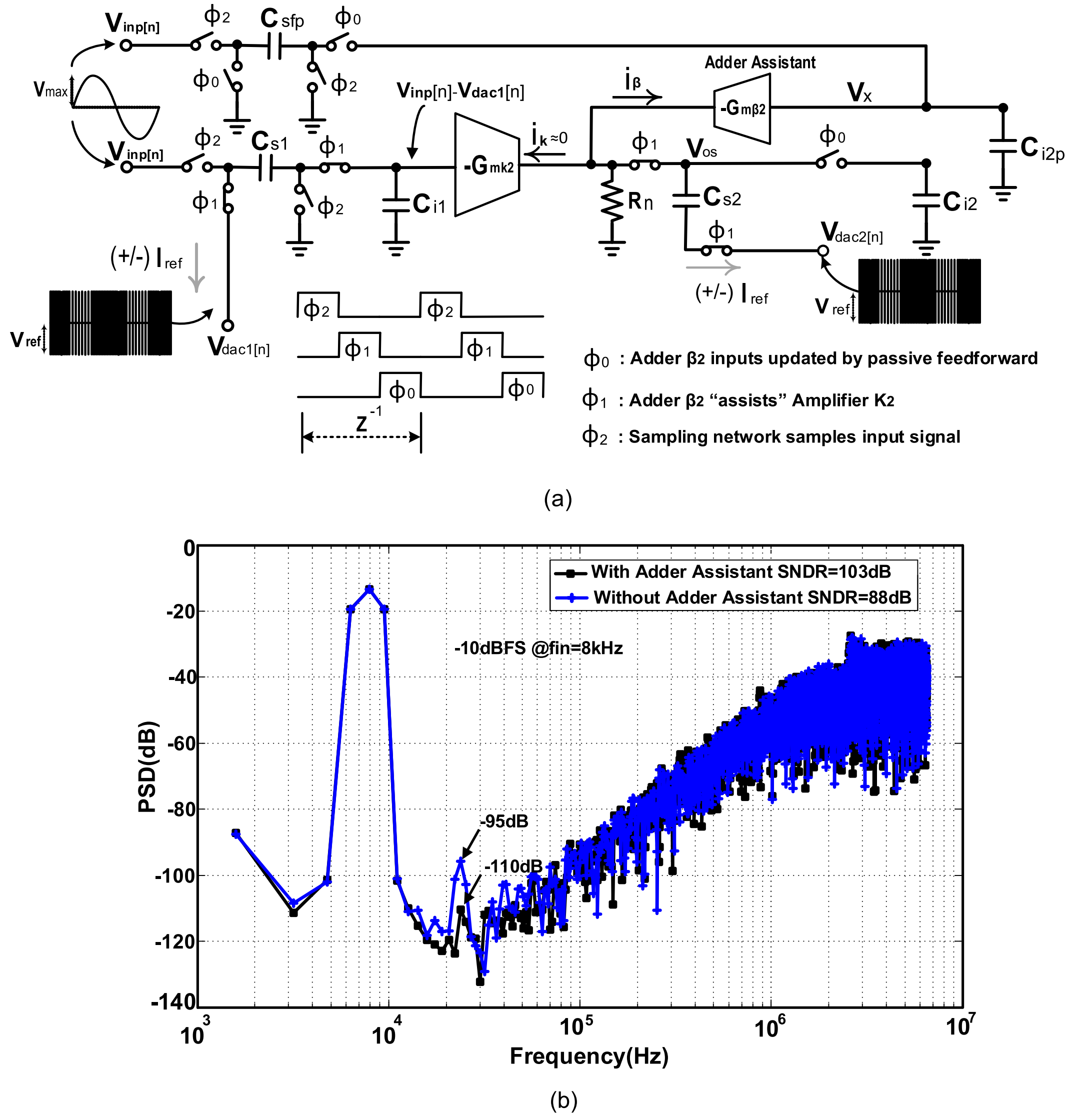

Fig. 12. (a) Circuit diagram during phase ϕ_1 operation (single sided). (b) PSD comparison for adder β_2 inputs with or without feedforward.

With $V_{\text{ref}} = 1.1$ V, the full-scale amplitude is 2.2 V. The requirement of having $\bar{n} = 17$ (SNR $= 104$ dB) leads to a minimum value of C_{s1} of 0.23 pF, a value which is small enough to allow designs with very low α_1, down to 0.01.

The SNR further increases if the gain K_2 increases. Fig. 7 shows the dependence of the SNR on K_2 for a constant $K_3 = 14$ dB.

The sensitivity of other parameters is low. Fig. 8 reports behavioral simulation results with variation of the value of various parameters in a wide range. The results show that even a change of ±20% causes a very small variation in the SNR.

IV. Circuit Implementation

Fig. 9 shows the full SC implementation of Fig. 5. The schematic shown in Fig. 2(b) realizes the active blocks. The capacitors C_{s1} and C_{s2} implement the subtraction of signal and feedback. The third integrator uses a small capacitance C_{s3b} to realize the feedback coefficient F_2. The nominal values of capacitances are indicated in Fig. 9. The positive reference V_{rep} is 1 V and negative reference V_{ren} is 0 V.

The voltage swings at various nodes inside the loop filter are small but large enough to guarantee the required SNR. The swing at the input and output of the amplifier K_2 is around 20 mV$_{\text{PP}}$ and 85 mV$_{\text{PP}}$, respectively, while the swing at the input and output of amplifier$K_3$is around 30 mV$_{\text{PP}}$ and 170 mV$_{\text{PP}}$, respectively. The swing at the input of the comparator is 14 mV$_{\text{PP}}$, a value that does not create significant problems for switching the comparator. Having a small swing at the input of the interstage amplifiers benefits linearity as verified by the experimental test.

In order to further reduce the power consumed, the two amplifiers can be time-shared. For this, the nonoverlapping phase's scheme ϕ_2, ϕ_1, ϕ_0 of Fig. 10 allows each stage to operate with two of the indicated nonoverlapping periods for implementing passive SC integration. The gain of the two active stages is not large but ensures proper control of the quiescent output, which is important for keeping the operation within the linear region. Because of this, the circuit, redrawn in Fig. 11(a) with the component sizes $R_n = R_p = 43$ kΩ, uses the sampled-data common mode feedback of Fig. 11(b) with capacitor $C_m = 100$ fF and $C_n = 200$ fF. The amplifiers K_2 and K_3 have aspect ratios of 9 μm/0.18 μm and 7 μm/0.18 μm, respectively. Both adders' β_2 and β_3 have the same aspect ratio of 6 μm/0.12 μm. Table II reports the summary of the amplifiers and adders' parameters of the second and third integrators.

When a low-gain op-amp is used, the effect of the limited gain is much more dominant. The limited gain results in the shift of the integrator pole toward the origin ($z = 0$), which reduces the effective in-band noise suppression in a $\Delta\Sigma$M, while the positive feedback gain will cause the integrator pole to move away from dc slightly ($z = 1.005$), thus resulting in the increase in the effective in-band noise suppression in the $\Delta\Sigma$M with improved noise shaping. As long as the input signal amplitude remains small with a small signal swing inside the loop filter, the quantizer will not saturate. The modulator remains stable and provides maximum suppression at dc in the $\Delta\Sigma$M. It is clear that a low-gain amplifier is an important advantage.

In conventional active DT $\Delta\Sigma$ converters, the first integrator demands high linearity and large gain to suppress circuit nonidealities in single-bit implementations. An assisted op-amp technique has been proposed to reduce the power of high-resolution single-bit CT $\Delta\Sigma$M. It suggests an extra op-amp with feedforward as an assistant to relax the slew rate requirement of the op-amp in the first integrator [22].

In the proposed active–passive design, the first integrator has no active gain. Due to the sharp steps of the first-stage single-bit feedback digital-to-analog converter (DAC) switches, the nonlinear behavior of amplifier K_2 causes performance degradation. It requires larger bias current for higher slew rates and bandwidth requirements to respond to large input steps. It is observed that the inability of amplifier K_2 to source or sink large currents instantaneously is responsible for nonlinearity. To overcome this challenge, a feedforward with built-in adder β_2 is used to assist amplifier K_2 for slew rate requirement.

Fig. 12(a) shows amplifier K_2's input and output network during the ϕ_1 phase. The input network has analog input signal $V_{\text{inp}}[n]$ and the first feedback DAC $V_{\text{dac1}}[n]$, while the output is connected to the top plate of the second integrator sampling capacitor C_{s2}. The bottom plate of C_{s2} is connected to the second feedback DAC $V_{\text{dac2}}[n]$, which has the same coefficient and timing as the first feedback DAC $V_{\text{dac1}}[n]$. The passive feedforward SC network C_{sfp} has already sampled the analog input signal $V_{\text{inp}}[n]$ during the ϕ_2 phase and will be integrated to C_{i2p} during the ϕ_0 phase. The C_{i2p} is the cross-coupled integration capacitor of the second passive SC integrator from the opposite side. Currently, C_{i2p} has analog input samples stored in the previous cycle $V_{\text{inp}}[n-1]$, as it is updated during the ϕ_0 phase after the ϕ_1 phase. This forms a passive feedforward integrator transfer function at node V_x with $\alpha_{fp} = 0.01 = (C_{sfp}/(C_{sfp}+C_{i2p}))$. The adder β_2 input is connected to the integration capacitor C_{i2p}, while its output is sharing the same resistive load of amplifier K_2. Due to the analog input signal $V_{\text{inp}}[n-1]$ provided at the input of adder β_2, amplifier K_2 will be assisted by adder β_2 by delivering the necessary discharging current. The sharp jumps

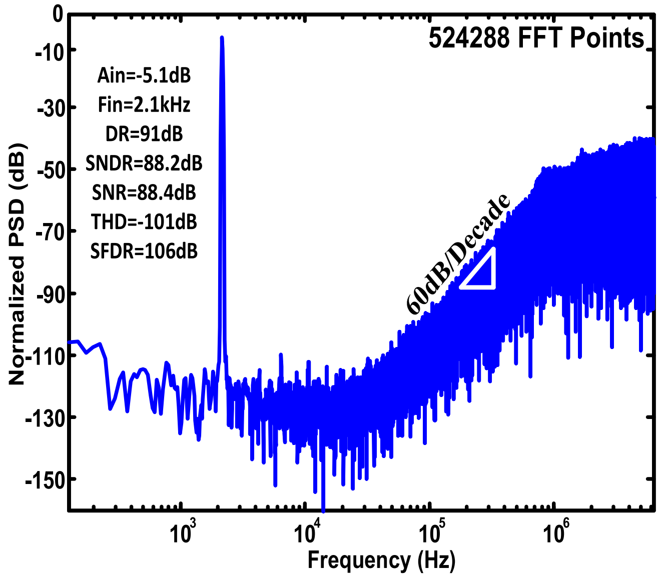

Fig. 13. Output PSD plot.

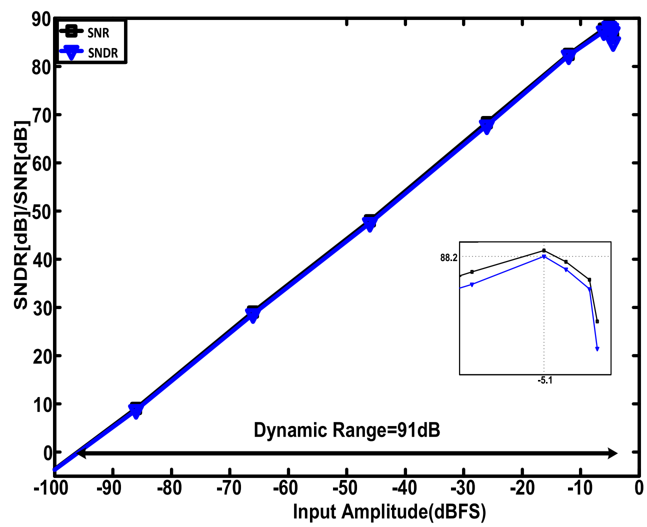

Fig. 14. Dynamic range plot.

at amplifier K_2's input caused by first feedback DAC switches no longer create any significant linearity problems. Amplifier K_2's output $V_{\text{os}}(z)$ during the ϕ_1 phase can be written as

$$V_{\text{os}}(z) \approx G_{mk2} R_n \left[\alpha_1 + \frac{G_{m\beta 2}}{G_{mk2}} \frac{\alpha_{fp} z^{-1}}{[1-(1-\alpha_{fp})z^{-1}]} \right] V_{\text{inp}}(z) - G_{mk2} R_n \cdot \alpha_1 V_{\text{dac1}}(z) + V_{\text{dac2}}(z). \tag{12}$$

Fig. 12(b) compares the power spectral density (PSD) of the modulator with and without adder β_2 inputs connected to the passive feedforward, which confirms that using adder β_2 improves the signal-to-noise-plus-distortion ratio (SNDR) by 15 dB in the implementation at transistor level. From the discussion above, it is shown that adder β_2 significantly improves the distortion performance of the integrator. Amplifier K_2 does not need to source/sink the main current thanks to adder β_2; it is thus designed with much lower quiescent currents, thereby saving power.

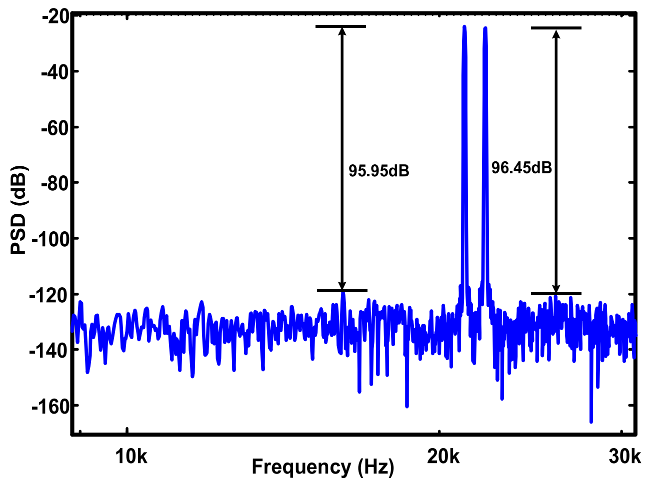

Fig. 15. Two-tone test.

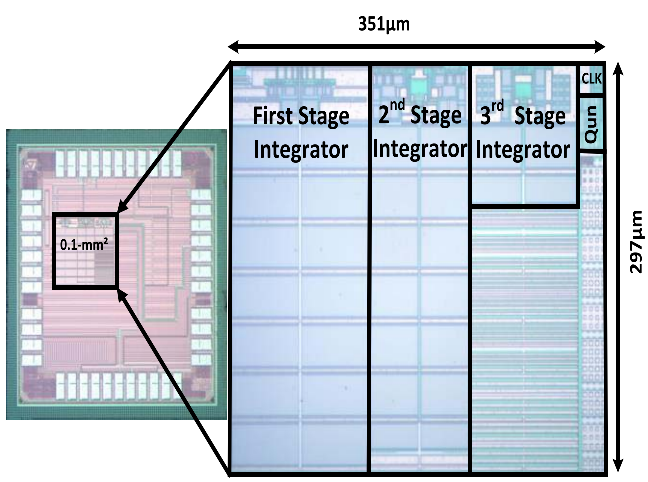

Fig. 16. Die microphotograph.

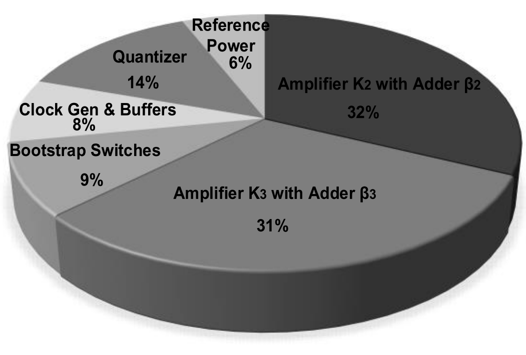

Fig. 17. Power breakdown.

V. Measurement Results

The prototype of the ΔΣM was fabricated with a standard 65-nm 1P7M digital CMOS process. For the testing of the chip, a low distortion function generator (SRS DS360) provides the differential input signal while an Agilent E4438C signal generator generates the clock. The output data, captured by the logic analyzer, were processed by MATLAB to determine the output PSD. Fig. 13 shows the output PSD for an input signal amplitude of −5.1 dBFS with an input frequency of 2.13 kHz. The spectrum accounts for a series of 512K fast Fourier transform points shaped by a Blackman–Harris window. The third harmonic is at −106 dBc, a very low value generated by the minimum swing and the limited slew rate requirement of the first amplifier K_2. The peak SNR is more than 88 dB and occurs at −5.1 dBFS. The flat in the spectrum extends until the signal band mainly limits the value of the SNR. The measured dynamic range of the modulator is 91 dB as shown in Fig. 14. A two-tone test determines the third-order intermodulation distortion (IMD3).

As Fig. 15 shows the two tones at 21.3 kHz and 22.13 kHz with an amplitude for each of them equal to 530 $\mathrm{mV_{PP}}$ cause IMD products at −94.95 and −96.85 dB, respectively. The active area of the modulator, excluding the pads and output drivers, is approximately 0.1 mm^2. As shown in Fig. 16, it is dominated by the large integration capacitor. The test chip was also measured under a supply variation of ±10% and the peak SNRs and SNDRs vary between 1 and 2 dB. The power consumption of the analog section is 45.5 μW, the reference power is 4.6 μW, while the digital power is 23.5 μW for a total consumption of 73.6 μW at 1 V supply; Fig. 17 shows the estimated breakdown in power consumption. The reference voltage was buffered off-chip. The measured summary of the modulator performance is presented in Table III. The result corresponds to a Walden $\mathrm{FoM_{walden}}$ [23] of 70 fJ/conv-step as given in (13) and Schreier $\mathrm{FoM_{Schreier}}$ [23] of 176.3 dB as given in (14). These figures are competitive with high-resolution audio CT implementations with similar performances, as shown in Table IV. A comparison with state-of-the-art passive and active–passive modulators is also shown

TABLE III
Summary of the Measurement Results

Parameter	Value
Technology	65 nm CMOS
Supply Voltage	1 V
Signal Bandwidth	25 kHz
Sampling Frequency	13 MHz
Oversampling Ratio	260
Peak SNR	88.4 dB
Peak SNDR	88.2 dB
SFDR	106 dB
Dynamic Range	91 dB
Input Range(Differential)	1.1 $\mathrm{V_{PP}}$
Core Size Area	0.1 mm^2
Total Power Consumption (including reference)	73.6 µW
PSRR@1kHz with 100 $\mathrm{mV_{PP}}$	68 dB
CMRR@1kHz with 50 $\mathrm{mV_{PP}}$	67 dB
$\mathrm{FoM_{Walden}}$	70 fJ/conv-step
$\mathrm{FoM_{Schreier}}$	176.3 dB

TABLE IV
BENCHMARKING WITH THE STATE-OF-THE-ART AUDIO $\Delta\Sigma$Ms

Parameters	[22] JSSC'10	[24] JSSC'11	[25] CICC'11	[26] JSSC'12	[27] JSSC'13	[28] JSSC'14	**This Work**
Type	CT	CT	DT	DT	DT	CT	**DT**
Tech (nm)	180	130	65	130	65	180	**65**
Area (mm²)	0.26	0.11	0.41	0.57	0.3	0.22	**0.1**
V_{DD} (V)	1.8	0.6	1	0.5	0.8	1.8	**1**
Power (μW)	122	28.6	371	35.2	230	280	**73.6**
SNDR (dB)	89.1	79.1	95	81.7	91	98.2	**88.2**
DR (dB)	91.5	82	96.4	85	98	103	**91**
BW (Hz)	24 k	20 k	24 k	20 k	20 k	24 k	**25 k**
FoM_{walden}	109	97	168	88	198	88	**70**
$FoM_{Schreier}$	174.4	170.4	174.5	172.5	177.3	182.3	**176.3**

TABLE V
BENCHMARKING WITH THE STATE-OF-THE-ART PASSIVE AND ACTIVE–PASSIVE $\Delta\Sigma$Ms

Parameters	[13] ISSCC'05	[14] JSSC'08	[15] TCAS-I'08	[10] TCAS-I'14	[11] JETCAS'15	[17] ISSCC'16	**This Work**
Type	Hybrid, CT	Hybrid, CT	Hybrid, DT	Hybrid, DT	Passive, DT	Hybrid, CT	**Hybrid, DT**
Tech (nm)	90	250	130	65	65	65	**65**
Power (μW)	5400	2700	5500	1.27	0.47	1570	**73.6**
SNDR (dB)	N/A	63.4	56	70	71	72.2	**88.2**
DR (dB)	86	68	54	70.5	74	77	**91**
BW (Hz)	600 k	2 M	10 M	500	500	10 M	**25 k**
FoM_{walden}	N/A	558	533	491	162	23.6	**70**
$FoM_{Schreier}$	166.4	156.6	146.5	156.4	164.2	175	**176.3**

in Table V

$$\mathrm{FoM}_{\mathrm{Walden}} = \frac{\mathrm{Power}}{2 \times \mathrm{Bandwidth} \times 2^{(\mathrm{SNDR}-1.76)/6.02}} \tag{13}$$

$$\mathrm{FoM}_{\mathrm{Schreier}} = \mathrm{DR}_{\mathrm{dB}} + 10\log\left(\frac{\mathrm{Bandwidth}}{\mathrm{Power}}\right). \tag{14}$$

VI. CONCLUSION

A method utilizing a low-gain amplifier with a positive feedback that improves the performance of a passive SC integrator and makes it suitable for use in high-resolution $\Delta\Sigma$M was introduced. The method significantly reduces the power consumed and achieves power effectiveness comparable to or better than those of CT counterparts. The proposed technique, applied to a third-order $\Delta\Sigma$M with a single-bit comparator, has been experimentally verified. Also power reduction for a single-bit modulator is achived by utilizing a feedforward with built-in adder β_2 to assist the first amplifer K_2. The 65-nm CMOS prototype that uses a passive SC integrator in the first stage achieves a dynamic range of 91 dB, an SNR of 88.4 dB, and an SNDR of 88.2 dB. The power consumed is 73.6 μW at a supply voltage of 1 V. The corresponding $\mathrm{FoM}_{\mathrm{Walden}}$ is 70 fJ/conv-step and the $\mathrm{FoM}_{\mathrm{Schreier}}$ is 176.3 dB.

REFERENCES

[1] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. New York, NY, USA: Wiley, 1997, pp. 168–169.

[2] L. Yao, M. S. J. Steyaert, and W. Sansen, "A 1-V 140-μW 88-dB audio sigma-delta modulator in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1809–1818, Nov. 2004.

[3] J. Roh, S. Byun, Y. Choi, H. Roh, Y.-G. Kim, and J.-K. Kwon, "A 0.9-V 60-μW 1-bit fourth-order delta-sigma modulator with 83-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 361–370, Feb. 2008.

[4] I.-J. Chao, C.-M. Kuo, B.-D. Liu, C.-Y. Huang, and S.-J. Chang, "A 3rd-order delta-sigma modulator with timing-sharing opamp-sharing technique," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2013, pp. 2002–2005.

[5] A. Pena-Perez, E. Bonizzoni, and F. Maloberti, "A 88-dB DR, 84-dB SNDR very low-power single op-amp third-order $\Sigma\Delta$ modulator," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2107–2118, Sep. 2012.

[6] J. Koh, Y. Choi, and G. Gomez, "A 66 dB DR 1.2 V 1.2 mV single-amplifier double-sampling 2nd-order $\Delta\Sigma$ ADC for WCDMA in 90 nm CMOS," in *Proc. IEEE Int. Solid-State Circuit Conf. (ISSCC)*, Feb. 2005, pp. 170–591.

[7] R. Zanbaghi, S. Saxena, G. C. Temes, and T. Fiez, "A 75-dB SNDR, 5-MHz bandwidth stage-shared 2–2 MASH $\Delta\Sigma$ modulator dissipating 16 mW power," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1614–1625, Aug. 2012.

[8] F. Chen and B. Leung, "A 0.25-mW low-pass passive sigma-delta modulator with built-in mixer for a 10-MHz IF input," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 774–782, Jun. 1997.

[9] F. Chen, S. Ramaswamy, and B. Bakkaloglu, "A 1.5 V 1 mA 80 dB passive $\Sigma\Delta$ ADC in 0.13 μm digital CMOS process," in *Proc. IEEE Int. Solid-State Circuit Conf. (ISSCC)*, Feb. 2003, pp. 32–33.

[10] A. F. Yeknami, F. Qazi, and A. Alvandpour, "Low-power DT $\Delta\Sigma$ modulators using SC passive filters in 65 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 358–370, Feb. 2014.

[11] F. Qazi and J. Dabrowski, "Passive SC sigma delta modulators revisited: Analysis and design study," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 4, pp. 624–636, Dec. 2015.

[12] J. L. A. de Melo, F. Querido, N. Paulino, and J. Goes, "A 0.4-V 410-nW opamp-less continuous-time $\Sigma\Delta$ modulator for biomedical applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Jun. 2014, pp. 1340–1343.

[13] A. Das, R. Hezar, R. Byrd, G. Gomez, and B. Haroun, "A 4th-order 86 dB CT $\Delta\Sigma$ ADC with two amplifier in 90 nm CMOS," in *Proc. IEEE Int. Solid-State Circuit Conf. (ISSCC)*, Feb. 2005, pp. 496–498.

[14] T. Song, Z. Cao, and S. Yan, "A 2.7-mW 2-MHz continuous-time $\Sigma\Delta$ modulator with a hybrid active–passive loop filter," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 330–341, Feb. 2008.

[15] R. Yousry, E. Hegazi, and H. F. Ragai, "A third-order 9-bit 10-MHz CMOS $\Delta\Sigma$ modulator with one active stage," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 9, pp. 2469–2482, Oct. 2008.

[16] A. F. Yeknami and A. Alvandpour, "A 0.7-V 400-nW fourth-order active-passive $\Delta\Sigma$ modulator with one active stage," in *Proc. 21st IEEE Int. Conf. Very Large Scale Integr. (VLSI-SoC)*, Oct. 2013, pp. 1–6.

[17] B. Nowacki, N. Paulino, and J. Goes, "A 1 V 77dB-DR 72dB-SNDR 10 MHz-BW 2-1 MASH CT $\Delta\Sigma$M," in *Proc. IEEE Int. Solid-State Circuit Conf. (ISSCC)*, Jan./Feb. 2016, pp. 274–275.

[18] A. Hussain, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "NTF zero compensation technique for passive sigma-delta modulator," in *Proc. IEEE PRIMEASIA*, Oct. 2011, pp. 82–85.

[19] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2358–2368, Nov. 2005.

[20] F. Maloberti, *Analog Design for CMOS VLSI Systems*. Dordrecht, The Netherlands: Kluwer, 2001.

[21] F. Maloberti, *Data Converters*. Dordrecht, The Netherlands: Springer-Verlag, 2007.

[22] S. Pavan and P. Sankar, "Power reduction in continuous-time delta-sigma modulators using the assisted opamp technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1365–1379, Jul. 2010.

[23] B. Murmann. (2015). *ADC Performance Survey 1997–2015*. [Online]. Available: http://stanford.edu/~murmann/adcsurvey.html

[24] J. Zhang, Y. Lian, L. Yao, and B. Shi, "A 0.6-V 82-dB 28.6-μW continuous-time audio delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2326–2335, Oct. 2011.

[25] L. Liu, D. Li, Y. Ye, L. Chen, and Z. Wang, "A 95 dB SNDR $\Delta\Sigma$ audio modulator in 65 nm CMOS," in *Proc. IEEE CICC*, Sep. 2011, pp. 1–4.

[26] Z. Yang, L. Yao, and Y. Lian, "A 0.5-V 35-μW 85-dB DR double-sampled $\Delta\Sigma$ modulator for audio applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 722–735, Mar. 2012.

[27] H. Luo, Y. Han, R. C. C. Cheung, X. Liu, and T. Cao, "A 0.8-V 230-μW 98-dB DR inverter-based $\Sigma\Delta$ modulator for audio applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2430–2441, Oct. 2013.

[28] A. Sukumaran and S. Pavan, "Low power design techniques for single-bit audio continuous-time delta sigma ADCs using FIR feedback," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2515–2525, Nov. 2014.

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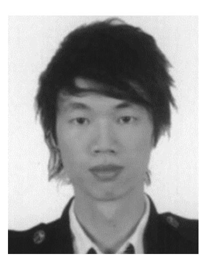

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Prof. Martins is a Nominations Committee Member of the IEEE CASS. He was a recipient of two government decorations: the Medal of Professional Merit from the Macau Government (Portuguese Administration) in 1999, and the Honorary Title of Value from the Macau SAR Government (Chinese Administration) in 2001. In 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences in Lisbon, being the only Portuguese Academician living in Asia. He was the Founding Chairman of the IEEE Macau Section from 2003 to 2005, and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 (2009 World Chapter of the Year of the IEEE CASS). He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS–APCCAS'2008, and the Vice President for the Region 10 (Asia, Australia, and the Pacific) of the IEEE CAS Society from 2009 to 2011. He was the Vice President (World) Regional Activities and Membership of the IEEE CAS Society form 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2010 to 2013. He was nominated as the Best Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II form 2012 to 2013. He was a member of the IEEE CASS Fellow Evaluation Committee in 2013 and 2014, and the CAS Society Representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)–Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference in 2016.