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A 4x Time-Domain Interpolation 6-bit 3.4 GS/s 12.6 mW Flash ADC in 65 nm CMOS

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Abstract— **A 6-bit 3.4 GS/s flash ADC in a 65 nm CMOS process is reported along with the proposed 4x time-domain interpolation technique which allows the reduction of the number of comparators from the conventional 2^N-1 to 2^{N-2} in a N-bit flash ADC. The proposed scheme effectively achieves a 4x interpolation factor with simple SR-latches without extra clocking and calibration hardware overhead in the interpolated stage where only offset between the 2^{N-2} comparators needs to be calibrated. The offset in SR-latches is within ±0.5 LSB in the reported ADC under a wide range of process, voltage supply, and temperature (PVT). The design considerations of the proposed technique are detailed in this paper. The prototype achieves 3.4 GS/s with 5.4-bit ENOB at Nyquist and consumes 12.6 mW power at 1 V supply, yielding a Walden FoM of 89 fJ/conversion-step.**

Index Terms—**Flash ADC, time comparator, 4x time-domain interpolation, SR-latch**

I. INTRODUCTION

Low-power gigahertz sampling rate ADCs are in high demand for the next generation communication systems. Recently, time-interleaved (TI) and multi-bit ADCs based on low-power SAR-type sub-ADCs have entered the mainstream of high-speed and show good energy efficiency in this range of specifications [1-4]. Nevertheless, high-speed TI ADCs have calibration overhead issues due to mismatches between sub-channels, whereas flash ADCs are known as the fastest single channel ADC architecture achieving GS/s conversion speeds which relies on the parallelism operation of the comparators. This keeps flash ADCs still attractive for high speed applications. However, its number of comparator grows exponentially with the bit resolution leading to a large area overhead. Besides, the power dissipation is also not efficient because only a single comparator is critical at each conversion whereas the rest are just dissipating power to obtain a trivial answer. In particular, the size and power consumption of comparators is usually large when considering fast latching speed without pre-amplifiers. Thus, the input capacitance also increases, which reduces the bandwidth of the input network. In addition, the ADC performance tends to degrade as signal frequency increases, since the enlarged area due to a large number of comparators implies a different timing errors of the distributed clock and the input signal in all comparators.

Allowed by technology scaling, x2 interpolation techniques that reduce the number of the first stage comparators by half, have been reported using only dynamic comparators [5] or SR-latches [6]. However, in the applications where lower power and wider signal bandwidth are requested, a higher interpolation factor larger than two is preferable, which will reduce hardware complexity and related burdens such as input capacitance and clock distribution. A total interpolation factor of 4 is proposed in [7] with a two-stage cascaded latch interpolation technique. But, it requires background calibration in order to eliminate the offset in the 2nd stage

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latches, besides the 1st stage comparators. This adds hardware complexity and higher power consumption.

This paper reports a time-interpolation flash ADC [8] which achieves the same interpolation factor as [7]. However, the interpolated SR-latches do not require extra calibration or clock control; therefore, the design complexity and hardware overhead is low. Only 16 comparators are required in the proposed 6-bit flash ADC; therefore, both the input capacitance and the power of the clock buffers are reduced. The measurement results are also presented to show the effectiveness of the proposed interpolation technique. The power consumption is 12.6 mW at 3.4 GS/s with 1 V supply and achieving 34.2 dB SNDR at Nyquist input rate. Design considerations of the proposed technique are also discussed, especially on its non-ideality due to the process, supply voltage and temperature (PVT) variation. The analysis shows that the interpolation technique is robust in low-to-moderate resolution design.

The paper is organized as follows: Section II shows the architecture of this work. Section III describes the working principle of the proposed 4x time-domain interpolation technique and discusses its non-ideality effect under PVT variation. Section IV and V depicts the measurement results and draws a conclusion.

II. ADC Architecture

Fig. 1 illustrates the architecture of the proposed 4x time-domain interpolation flash ADC. For simplicity, the architecture is described in a single-ended version. The ADC mainly consists of a bootstrapped-switch sampling front-end, a reference ladder for reference generation, 16 dynamic comparators (CMP), 45 SR-latches which are interpolated between every two adjacent CMPs' output, a digital encoder and a digital offset calibration circuit for the dynamic comparators. The architecture of CMP is StrongArm with NMOS transistors as the inputs [13] plus an extra input pair for calibrating its offset voltage. The calibration procedure is similar as [14]. In the comparison phase, the CMPs compare the sampled signal with their corresponding reference voltages and then the interpolated SR-latches compare the time difference from every two adjacent CMPs' outputs. In the end, the obtained 61 bits thermometer codes (from both CMPs and SR-latches) are stored and encoded in a four-

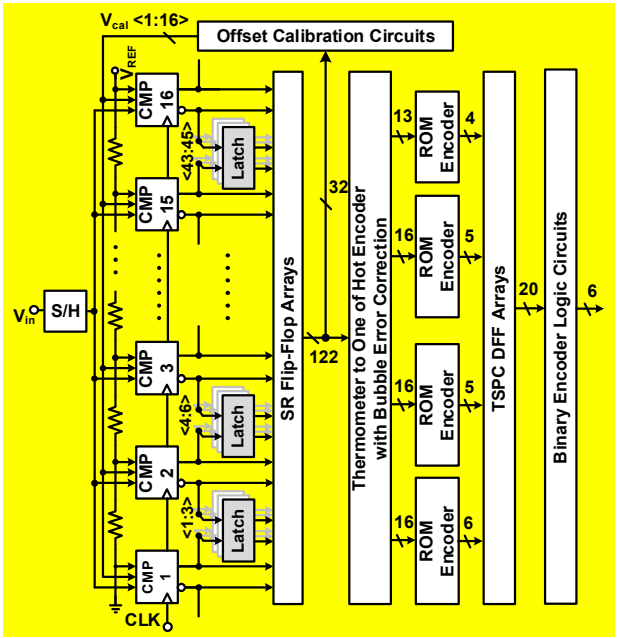


Fig. 1. Overall ADC architecture.

sectioned ROM-based encoder [12]. Their outputs are then further decoded by the binary decoder logic circuits. With the interpolation, the number of comparators in the proposed architecture is reduced to only 16 for 6-bit from the conventional flash ADC design.

III. Proposed 4x Time-Domain Interpolation

1. Diagram of 4x Time-Domain Interpolation

Fig. 2 shows a detailed configuration of the proposed 4x time-domain latch interpolation technique (one unit). It consists of two stages where the 1st stage includes two comparators and the 2nd stage has three interpolating SR-latches. The 1st stage comparators (CMP1 and CMP2) compare the input signal (V_{in}) with their corresponding reference voltages ($V_{REF}[k-2]$ / $V_{REF}[k+2]$). Further, three comparators are removed between CMP1 and CMP2, which are supposed to have their reference voltages as: $V_{REF}[k-1]$, $V_{REF}[k]$ and $V_{REF}[k+1]$ which divides the voltage between $V_{REF}[k-2]$ and $V_{REF}[k+2]$ to 4 equal parts. Instead, the decisions of these reference voltages are given in the SR-latches in the 2nd stage. The inverters between the CMPs and SR-latches are used as buffers and change the falling edges of outputs of CMPs to rising edges as shown in Fig. 2. So the NAND-based SR-latches can be

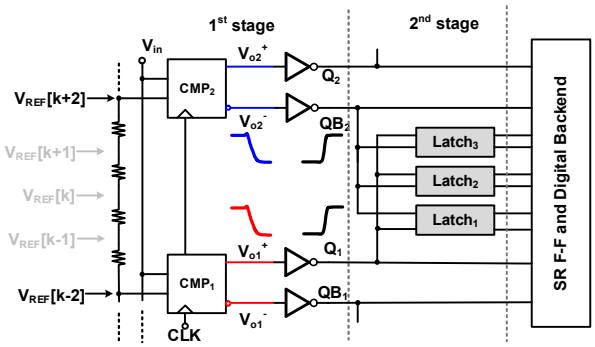


Fig. 2. Proposed 4x time-domain interpolation architecture.

used in cascade for better sensitivity, speed and power under the same area as the NOR-based. There is a total of 3 SR-latches in the 2nd stage and only 2 with deliberate built-in time offset (1 and 3) and latch 2 is with zero offset. These 3 SR-latches compare the time difference at the neighboring comparator's outputs (QB_2 and Q_1) and generate extra three decisions for reference voltages at $V_{REF}[k-1]$, $V_{REF}[k]$ and $V_{REF}[k+1]$ as explained in detail next.

2. Principle of the 4x Time-Domain Interpolation

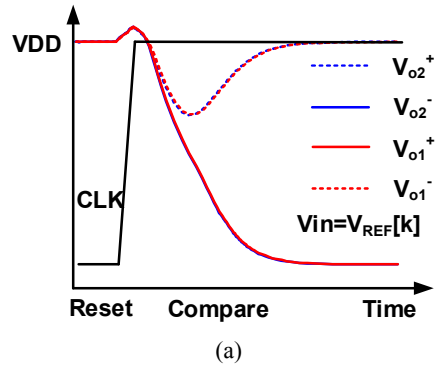
Most models of bi-stable circuits operating in latches assume that the cross-coupled gate circuits act as two linear amplifiers in its first order model and the time required for the latch to regenerate to a valid-logic-level (V_{valid}) is [9]:

$$t_{comp} = \tau_{reg} \cdot \ln\left(\frac{V_{valid}}{\Delta V_{in}}\right) \quad (1)$$

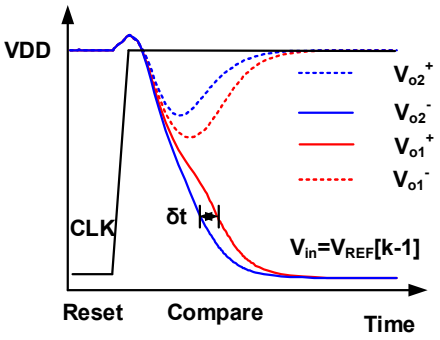
where ΔV_{in} is the initial voltage at the beginning of the latching phase, and the time constant τ_{reg} is the product of g_m and C_L, which is the transconductance and load capacitance of the amplifier in the bi-stable circuit, respectively. For the two adjacent comparators in the flash ADC as shown in Fig. 2, the time difference δt_{comp} of both rising/falling edge is given by

$$\delta t_{comp} = t_{comp1} - t_{comp2} = \tau_{reg} \ln\left(\frac{V_{LSB} - \Delta V_{in}}{\Delta V_{in}}\right) \quad (2)$$

where V_{LSB} is the LSB voltage of the ADC. Referring to Fig. 2 of the 4x time latch interpolation scheme, when V_{in}



(a)



(b)

Fig. 3. Simulated transient behaviors of two adjacent comparators in Flash ADC with input equal to three threshold of zero-crossing (a) $V_{in}=V_{REF}[k]$, (b)$V_{in}=V_{REF}[k-1]$.

is at the center of $V_{REF}[k-2]$ and $V_{REF}[k+2]$ ($V_{in}=V_{REF}[k]$ and $\Delta V_{in}= V_{LSB}/2$), the time difference δt_{comp} between V_{o1}^+ and V_{o2}^- or V_{o1}^- and V_{o2}^+ is zero. The positive output of CMP1 and negative output of CMP2, V_{o1}^+ and V_{o2}^-, fall from supply (VDD) to ground (zero) simultaneously and their signals' behavior in this case is plotted in Fig. 3(a). In the other case, when V_{in} is at $V_{LSB}/4$ away from $V_{REF}[k-2]$, i.e., $V_{in}=V_{REF}[k-1]$ and the time difference δt_{comp} between V_{o1}^+ and V_{o2}^- (δt) can be obtained from (2), where $\delta t = \tau_{reg}\ln 3$ with $\Delta V_{in} = V_{LSB}/4$. Besides, V_{o2}^- falls faster than V_{o1}^+ in this case as shown in Fig. 3(b). While if $V_{in}=V_{REF}[k+1]$, the absolute time difference between V_{o1}^+ and V_{o2}^- keeps the same except that V_{o1}^+ falls faster than V_{o2}^- with the case when $\Delta V_{in}= 3V_{LSB}/4$.

The regeneration time of CMP1 and CMP2 with the adopted size versus different V_{in} between $V_{REF}[k-2]$ and $V_{REF}[k+2]$ is shown in Fig. 4. It can be observed that the time difference δt_{comp} of CMP1 and CMP2 is determined by the input. Thus, the time difference contains more than binary information of the input. If more time information can be detected, more bits resolution can be obtained. In this work, the time difference $\pm\delta t$ and 0, corresponding to

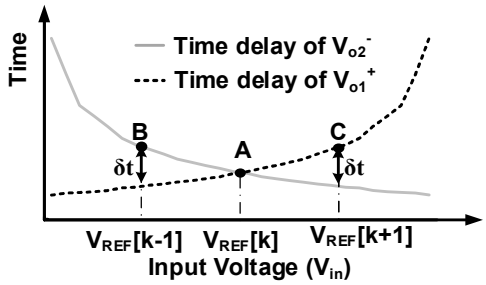


Fig. 4. Regeneration time with different input voltage between $V_{REF}[k-2]$ and $V_{REF}[k+2]$.

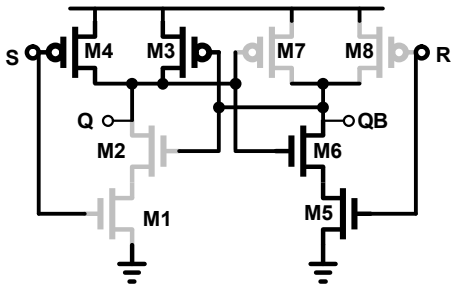


Fig. 5. Circuit schematic of the adopted SR-latch.

B, C and A as shown in Fig. 4, are detected by zero-crossing detectors at reference voltages of $V_{REF}[k-1]$, $V_{REF}[k]$ and $V_{REF}[k+1]$.

Simple NAND-based SR-latches are used to detect the time difference δt_{comp} in this design. The latch with symmetrical configuration have a zero-crossing at $\delta t_{comp} = 0$. To detect the δt_{comp} at $\pm\delta t$, deliberate mismatches are inserted in the NAND-based SR-latch as depicted in Fig. 5. Mismatched sizes in the bi-stable circuit in the NAND-based SR-Latch generating two different time constants which give rise to a time reference (δt_{SR}) with a new zero-crossing point. The negative time reference can be obtained by simply swapping the input (S & R). It is worth noting that although unbalance is intentionally inserted in the latch for the time reference, it does not affect the time difference δt_{comp} of comparators in the first stage. This is because there are two SR-latches with positive and negative time reference that are cascaded at Q_1 and QB_2, and the total loads between Q_1 and QB_2 are equal.

3. PVT Analysis of the Proposed Interpolation Technique

The adopted comparator circuit schematic is shown in Fig. 6. The adopted sizing of the latch with time

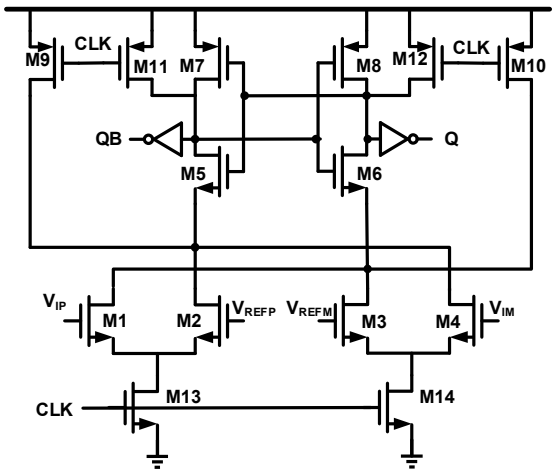


Fig. 6. Circuit schematic of the adopted comparator.

Table 1. Sizes of latch/comparator

(a) Sizes of SR-latch as the time comparator

Type \ Name, W/L (um/um)	M1&M2	M3&M4	M5&M6	M7&M8
Adopted size	1.03/0.06	0.4/0.06	0.4/0.06	1.03/0.06
Minimal size	1.9/0.06	0.4/0.06	0.4/0.06	1.9/0.06

(b) Sizes of StrongArm architecture comparator

Type \ Name, W/L (um/um)	M1-M4	M5&M6	M7&M8	M9&M10	M11&M12	M13&M14
Adopted size	2/0.06	1/0.06	1.2/0.06	0.6/0.06	0.9/0.06	0.5/0.06
Minimal size	0.5/0.06	0.3/0.06	0.4/0.06	0.2/0.06	0.3/0.06	0.2/0.06

reference and the ArmStrong comparator in this design is shown in Table 1(a) and (b), respectively. Since the total size between M1-M4 and M5-M8 keeps the loading of Q and QB equal, the time reference (δt_{SR}) at zero-crossing between S & R mainly originates from the mismatches of the transconductance (gm) of the transistors in the bistable circuit. In the bi-stable circuit model from [9], the authors show that the triggering point of the regenerative circuit is dependent on the τ of the cross-coupled amplifiers. If the τ are exactly matched in both branches of the cross-coupled amplifiers, the time offset δt_{SR} is zero. On the other hand, the mismatched τ between the branches gives rise to δt_{SR}. Since the comparators and SR-latches are both NAND-based, δt_{comp} and δt_{SR} abide by the same property [9]. This makes the offset between δt_{comp} and δt_{SR} change in a similar manner under PVT variation. Thus, the size-weighted time offset in the NAND-based SR-Latch is

Table 2. Variations of δt_{SR} and δt_{comp} under PVT

(a) Only corner changes

Corner / $\delta t_{comp}/\delta t_{SR}$ (ps/ps) / Type	FF	FS	TT	SF	SS
Adopted size	7.0/7.6	7.5/7.8	7.9/7.9	8.5/7.9	8.9/8.6
Minimal size	13.0/13.7	12.8/14.0	14.4/14.4	16.5/15.7	18.5/16.2

(b) Only supply voltage changes

Voltage/V / $\delta t_{comp}/\delta t_{SR}$ (ps/ps) / Type	0.9	1.0	1.1
Adopted size	8.8/8.3	7.9/7.9	7.5/8.0
Minimal size	16.0/15.0	14.4/14.4	13.1/14.6

(c) Only temperature changes

Temp./°C / $\delta t_{comp}/\delta t_{SR}$ (ps/ps) / Type	-45	27	125
Adopted size	6.6/6.2	7.9/7.9	9.8/9.2
Minimal size	12.0/11.3	14.4/14.4	16.78/17.8

robust to PVT variation in low-to-medium resolution designs and does not need calibration like in [7].

Table 2 lists the δt_{comp} at $Vin=V_{REF}[k+1]$ and the corresponding time reference δt_{SR} under corner (Table 2(a)), supply (Table 2(b)) and temperature (Table 2(c)) variation. The results are obtained from the interpolated latch at the boundary reference (worst case in this design) with post-layout simulation in Spice level with the adopted sizes in this design. Table 2(a)-(c) show the variation of δt_{comp} and δt_{SR} under four process corners, under 125°C and -45°C, as well as under ±10% supply voltage deviation.

In the TT corner at 27°C, with 1.0V voltage supply, $\delta t_{comp} \approx \delta t_{SR} \approx 7.9$ ps where the time reference is achieved by unbalance sizing in the latch. When the corner changes, δt_{comp} and δt_{SR} also changes in the same direction and the relative change rate is within 7.6% with the adopted sizes. The trend is kept when the voltage supply or temperature changes and the relative change rate is within 3.8% and 7.6%, respectively. That gives rise to a very small offset between δt_{comp} and δt_{SR} as shown in Fig. 7.

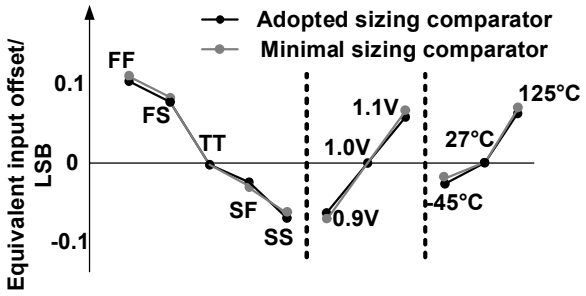


Fig. 7. Equivalent input offset of SR-latches.

Besides, we also perform another simulation analysis which reduces the size of comparators in the 1st stage to almost minimal. Since small size in the comparator makes δt_{comp} large, δt_{SR} also needs to be scaled. Accordingly, the size of SR-latch is modified as shown in Table 1 (minimal size row) and variations of δt_{SR} and δt_{comp} versus PVT variation is listed in Table 2(a)-(c) (minimum size row). The trends are similar to that of the adopted size except that δt_{SR} and δt_{comp} is nearly doubled. Therefore, it can be concluded that the proposed technique is not heavily depended on the size of the comparator and also robust with a lower speed comparator design. This characteristic is again due to the similar variation on the time constant in the comparator and the latch circuits.

To confirm the above assumptions, we also extract the transconductance (gm) value of the transistors from comparator and latch circuits with the adopted sizing. The gm %-variation with respect to the TT corner, 1.0V supply and 27°C from the comparator and SR-latch is depicted in Table 3. It shows that the gm drifted ratio from comparator and SR-latch have a similar trend as the delay. The residual gm variation differences lead to a small input-referred offset of SR-latch which is within 0.1 LSB as shown in Fig. 7. It is also worth noting that similar result is obtained with minimal sizing configuration. It can also be observed that the variation between δt_{comp} and δt_{SR} (as well as the gm) do not follow exactly. This is because 1) the different architecture of the StrongArm comparator and NAND-based SR-Latch. 2) The regeneration time will be affected by other transistors and parasitics.

IV. MEASUREMENT RESULTS

The circuit was implemented by using a 65 nm CMOS

Table 3. Gm change rate (%) under PVT with the adopted size in comparator and SR-latch

(a) Only corner changes

Type \ Corner (Gm variation %)	FF	FS	SF	SS
SR-latch	8.9	2.6	-2.6	-8.9
Comparator	16.7	10.1	-9.7	-12

(b) Only supply voltage changes

Type \ Voltage/V (Gm variation %)	0.9	1.1
SR-latch	-16.2	5.6
Comparator	-7.7	7.7

(c) Only temperature changes

Type \ Temp./°C (Gm variation %)	-45	125
SR-latch	11.4	-18.7
Comparator	10	-15.6

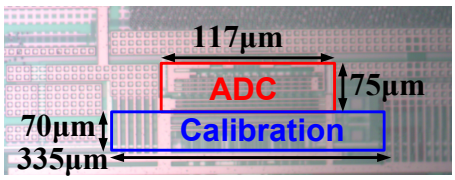


Fig. 8. Chip layout.

process. The chip, shown in Fig. 8, consists of the proposed 4x time-domain interpolation technique and calibration circuits for the comparators in the 1st stage. The active core area of the proposed ADC occupies 0.025mm^2. The ADC has a full-scale input range of 0.8 Vpp differential and an input capacitance of only 120 fF including parasitics. Fig. 9 illustrates the measured FFT plotted at near Nyquist input frequency with on-chip offset calibration. The SNDR before calibration is 18.6 dB and after calibration it improved to 34.2 dB. At high input frequency, the 3rd harmonic limits the SFDR which is due to the sampling nonlinearity and edging effect of the boundary comparators. Fig. 10 shows the measured dynamic performance across different sampling frequencies with low frequency input. It can be seen that the prototype maintains a constant SNDR in a wide range

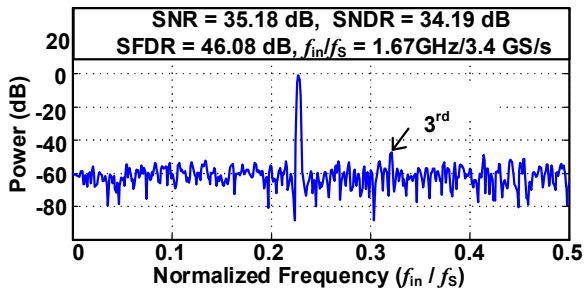


Fig. 9. Measured FFT spectrum at fin = 1.67 GHz.

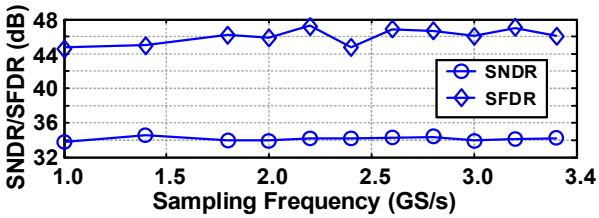


Fig. 10. Measured SFDR/ SNDR v.s. sampling frequencies.

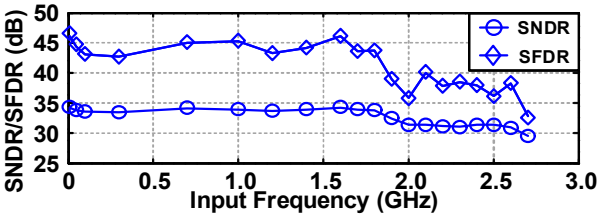


Fig. 11. Measured SNDR/SFDR vs. input frequencies.

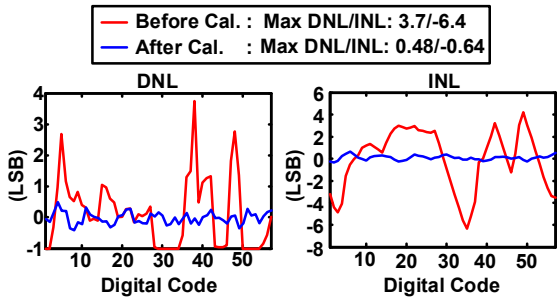


Fig. 12. Measured DNL/INL before and after calibration.

of sampling frequencies. Fig. 11 shows the measured dynamic performances across different input frequencies at 3.4 GS/s. The SNDR remained above 32 dB until a 1.8 GHz input. Fig. 12 shows the measured static performance. The on-chip offset calibration improves DNL from 3.75/-1 LSB to 0.48/-0.37 LSB and the INL from 4.21/-6.34 LSBs to 0.64/-0.48 LSBs. Fig. 13 compares this design with all state-of-the-art ADCs from ISSCC and VLSI conferences [15] with sampling frequencies larger than 2 GHz. For single channel designs,

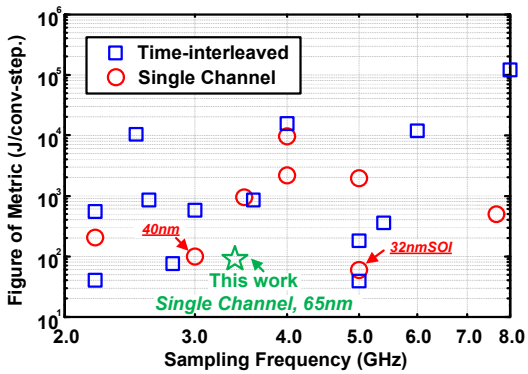


Fig. 13. FoM for previously reported >2GS/s in ISSCC and VLSI and this work.

Table 4. Performance Summary

	[7]	[6]	[5]	[10]	This work
Architecture	Flash	Flash	Flash	Flash	Flash
Resolution (bit)	7	6	6	6	6
Technology (nm)	65	40	90	32 SOI	65
Sampling Rate (GS/s)	2	3	4.1	5	3.4
Supply Voltage (V)	1.2	1.1	1.2	0.85	1.0
Power (mW)	20.7	11	76	8.5	12.6
ENOB @Nyquist	6.04	5.21	5.05	4.85	5.39
Area (mm^2)	0.2	0.021	-	0.02	0.034
Input capacitor (fF)	70	72	-	135	120
Offset Calibration	On chip	On chip	On chip	On chip	On chip
FoM @Nyq (fJ/conv.step)	157	100	625	59.6	89

the proposed ADC only has a higher FoM than one circuit in 32nm SOI. Table 4 summarizes and compares the overall measured performance with state-of-the-art flash ADCs. The total power consumption is 12.6 mW, at 3.4 GS/s from 1 V supply, where the analog and digital blocks consume 9.1 mW and 3.5 mW, respectively. This work exhibits an excellent FoM of 89 fJ/conv.-step @Nyquist for the high-speed single channel flash ADC.

V. Conclusions

A low-voltage 4x time-domain latch interpolation technique is proposed which can reduce the number of dynamic comparators by 4-fold in conventional flash ADCs with only dynamic power consumption. By utilizing the time difference between two neighboring dynamic comparators, the interpolation technique shows a moderate level of tolerance on the PVT variation, with satisfactory measured performance from verified silicon results.

Acknowledgments

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