A 312 ps response-time LDO with enhanced super source follower in 28 nm CMOS

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High quality fully integrated power supplies could notably improve the performances of the noise-sensitive building block in the UWB communication systems. Double buffers are inserted into the cascode flipped-voltage-follower (FVF) topology to enable designing the dominant pole at the output node for better power supply rejection (PSR) and less voltage variation during load transient. An enhanced super source follower (E-SSF) is proposed to further reduce the output impedance of the buffer that drives the power transistor. The FVF-based low dropout regulator (LDO) with E-SSF achieves a worst-case PSR of −18.9 dB across the full spectrum and a transient response time of 312 ps. The proposed LDO is designed in a 28 nm CMOS process and consumes 100 µA quiescent current with 1.0 V input and 0.8 V output voltages. In total, 120 pF on-chip capacitors are used for filtering.

Introduction: Power supply rejection (PSR) is one of the most important specifications for a low dropout regulator (commonly known as LDO). In particular, wideband or even full-spectrum PSR is in demand for the UWB wireless/wireline communication systems [1, 2]. In these applications, filtering capacitors have to be on-chip, in order to eliminate the bond-wire effects and to reduce the on-chip coupled supply noises [2]. Moreover, minimising the number of off-chip components can shrink the device size and reduce the cost.

Flipped-voltage-follower (FVF) [3]-based LDO is one of the most popular architectures [4, 5], due to its simplicity and the potential for fast-transient-response. Since the FVF-based LDO is a single-ended topology, for a similar dynamic response, the FVF-based LDO only consumes 50% of the bias current compared with a conventional LDO that uses a differential error amplifier (EA). Although the FVF-based LDO also consists of an auxiliary differential EA, it is not in the main loop, and only serves as a bias voltage generator which consumes low current. Thus, the FVF-based LDO is more power-efficient.

The FVF with folded-cascode gain stage used in [4] and [5] can provide better DC regulation but makes it more difficult to drive large capacitive load for stability reasons. The FVF with a buffer stage designed in [1] is a low-gain but high bandwidth loop, achieving a full-spectrum worst-case PSR of −12 dB and a fast response time of 0.65 ns. The design of Zhan and Ki [6] demonstrated a full-load worst-case PSR of −38 dB with cascoded power transistors and a dropout voltage of 600 mV, sacrificing the efficiency and the transient performance. In this design, a full-spectrum worst-case PSR of −18.9 dB is achieved for UWB wireline/wireless receivers, with 200 mV dropout voltage and 100 pF load capacitor. In addition, the designed LDO has sub-nanosecond transient response time, making it suitable for digital loads as well.

Circuit implementation: As illustrated in Fig. 1*b*, the frequency of the output pole p_{OUT} shifts with load conditions. Besides, the load capacitor C_L includes the parasitic capacitors, like the n-well/p-sub junction capacitors and the gate capacitors of the load circuit, which means p_{OUT} could be an unavoidable low-frequency pole, Therefore, designing the dominant pole at the output node can achieve higher unity gain frequency (UGF), compared with the case that designs the p_{OUT} as a non-dominant pole. In addition, allocating most of the available on-chip capacitance (chip area) to the output node can reduce the instant voltage droop during load transient, and can also better filter out the input voltage ripples. The only drawback is that more current is needed to push the internal poles to the frequencies higher than the UGF. However, this problem will be alleviated in more advanced processes, making this process scalable LDO favourable for high performance designs.

Since the cascode FVF topology provides higher DC loop gain and consequently higher UGF, it is more difficult to make the loop being stable, especially when the UGF is in the ultra-high-frequency (UHF) band. As shown in Fig. 1*a*, in this Letter, double-buffers are inserted to drive the power transistor M_P, and only add tiny load capacitance to the node V_{A2}. The first buffer B_1 is simply an N-type metal–oxide–semiconductor (NMOS) source follower, while the second one B_2 is an enhanced super source follower (E-SSF) which is first proposed in this Letter.

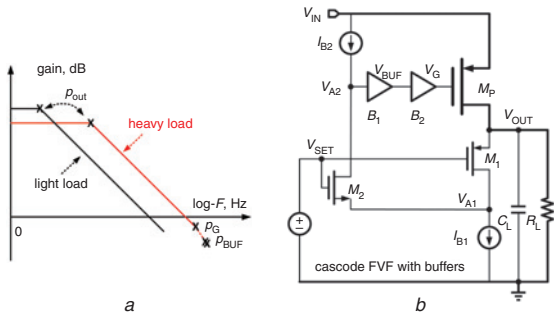

Fig. 1 *Schematic of FVF-based LDO with two buffer stages and locations of poles in conceptual Bode plot*

a Schematic of cascode FVF with buffers
b Conceptual Bode plot of open-loop transfer function

The transistor-level schematic of the proposed LDO is given in Fig. 2. V_{OUT} is a mirrored voltage of V_{MIR}, both of which are one V_{GS} higher than V_{SET}. The function of the left part is to generate the bias voltage V_{SET}. In the reference circuit design, the V_{REF} is commonly generated by conducting a current through a resistor. When the V_{REF} is close to its supply voltage V_{IN}, there is not enough voltage headroom for an accurate current source, such that the accuracy of the V_{REF} will be degraded. For using a lower reference voltage V_{REF}, a resistor ladder of R_1 and R_2 is employed to divide V_{MIR} and feed it back to the EA differential input.

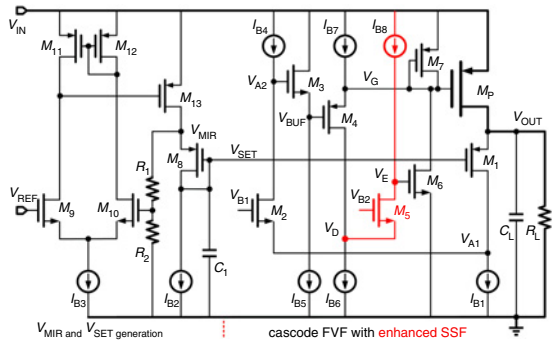

Fig. 2 *Schematic of proposed LDO*

The right part of the schematic shows the core circuits of the FVF structure with the proposed E-SSF. M_1 and M_2 serve as two common-gate amplification stages that provide the DC gain. M_3 is an NMOS source follower providing low input capacitance to the V_{A2} node, and also shifts down the voltage of V_{A2} into V_{BUF} providing more voltage headroom for V_G. To effectively drive M_P, a smaller output impedance of the SSF is needed. In the conventional SSF, only M_4 and M_6 are used, while in the proposed E-SSF, M_5 is inserted between M_4 and M_6. The output impedances of the conventional and the E-SSF are

$$r_{oB,Conv.} \approx \frac{1}{g_{m4} \cdot g_{m6} r_{o4}} \tag{1}$$

$$r_{oB,Prop.} \approx \frac{1}{g_{m4} \cdot g_{m6} r_{o4} \cdot g_{m5} r_{o5}}, \tag{2}$$

respectively. The inserted common-gate amplification stage formed by M_5 reduces the output impedance of the SSF buffer by a factor of $g_{m5}r_{o5}$, and thus provides a larger driving capability.

To reduce chip area, C_1 and C_L are implemented by low-voltage low-leakage MOS capacitors, with the values of 19 and 100 pF, respectively. Additional 1 pF is connected to the gate of the NMOS current mirrors for decoupling. Although M_2 and M_5 need gate bias voltages V_{B1} and V_{B2}, their gates can be connected to V_{MIR} to save additional bias branches. This bias sharing configuration is acceptable as both gates of M_2 and M_5 need to be referenced to ground.

Simulation results: The proposed idea is simulated in a 28 nm CMOS process. The AC responses including the Bode plots and the PSR curves with the load current ranging from 0.1 to 10 mA are given in Fig. 3. The loop UGF of the cascode FVF with the E-SSF is 1.28 GHz with 49° phase margin. Benefitting from the UHF bandwidth, full-spectrum PSR is achieved with the worst case of −18.9 dB happening at 1.55 GHz, while the low-frequency PSR is around −27 dB. The supply noise at above 1 MHz from the left part of Fig. 2 is filtered out by C_1. Thus, the PSR is improved at the 1–100 MHz range. The transient response is shown in Fig. 4. The voltage undershoot and overshoot are 26 and 21 mV, respectively, when the load current changes from 0.1 to 10 mA with the rise-/fall-time T_{Edge} of 30 ps.

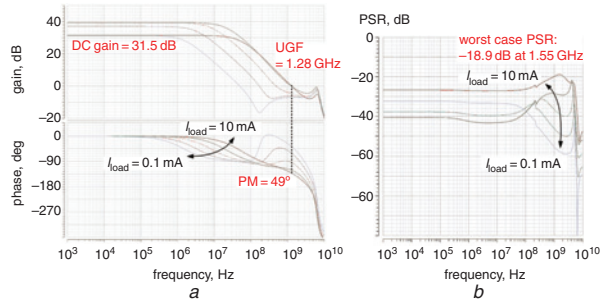

Fig. 3 *Simulated AC responses of proposed LDO with load current ranging from 0.1 to 10 mA*

a Bode plot of open-loop transfer function
b PSR performance of proposed LDO

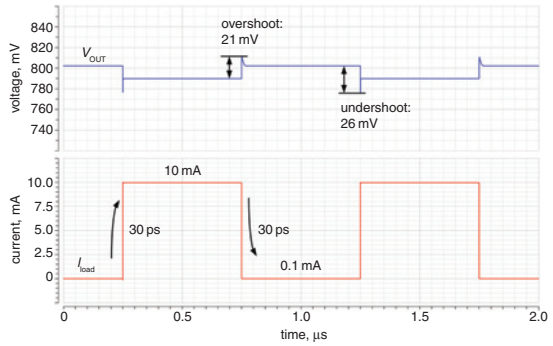

Fig. 4 *Simulated load transient response of LDO with 1.0 V input voltage and 0.8 V output voltage with voltage positioning*

The performance summary and comparisons with state-of-the-art designs are listed in Table 1. Comparing with [1], this work achieves over 6 dB better worst case PSR and about 70% less ΔV_{OUT} during the load transient. The figure-of-merit (FOM) equation of speed, as given below, was proposed in [4] and adopted here for comparison

$$\text{FOM} = T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}} \quad (3)$$

Table 1: Performance comparison with state-of-the-art designs

Publication	[4] 2005	[6] 2014	[1] 2015	This work
Technology, nm	90	350	65	28
V_{OUT}, V	0.9	1.2	1	0.8
Dropout, mV	300	600	150	200
I_Q	6 mA	44 µA	50–90 µA	100 µA
I_{MAX}, mA	100	12	10	10
Total cap.	600 pF	100 pF	140 pF	120 pF
Worst-case PSR	N/A	−38 dB at 50 MHz	−12 dB at 5 MHz	−18.9 dB at 1.55 GHz
ΔV_{OUT} @T_{Edge}	90 mV at 100 ps	105 mV at 500 ns	82 mV at 200 ps	26 mV at 30 ps
T_R[a]	0.54 ns	N/A	1.15 ns	312 ps
FOM[a], ps	32	N/A	5.74	3.12

[a]Calculated from T_R and FOM equations proposed in [4].

Conclusion: This Letter reports a fully on-chip FVF-based LDO with an E-SSF designed in a 28 nm CMOS process. The proposed UWB LDO achieves a −18.9 dB worst-case full-spectrum PSR with 200 mV dropout voltage, and obtained an ultra-fast response time of 312 ps and an FOM of 3.12 ps.

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One or more of the Figures in this Letter are available in colour online.

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References

1 Lu, Y., Wang, Y., Pan, Q., Ki, W.-H., and Yue, C.P.: 'A fully-integrated low-dropout regulator with full-spectrum power supply rejection', *Trans. Circuits Syst. I, Regul. Pap.*, 2015, **62**, (3), pp. 707–716, doi: 10.1109/TCSI.2014.2380644

2 Wang, Y., Lu, Y., Pan, Q., Hou, Z., Wu, L., Ki, W.-H., and Yue, C.P.: 'A 3-mW 25-Gb/s CMOS transimpedance amplifier with fully integrated low-dropout regulator for 100GbE systems'. IEEE Radio Frequency Integrated Circuits Symp., Tampa, USA, June 2014, pp. 275–278, doi: 10.1109/RFIC.2014.6851718

3 Carvajal, R.G., Ramírez-Angulo, J.A., López-Martín, J., Torralba, A., Galán, J.A.G., Carlosena, A., and Chavero, F.M.: 'The flipped voltage follower: a useful cell for low-voltage low-power circuit design', *Trans. Circuits Syst. I, Regul. Pap.*, 2005, **52**, (7), pp. 1276–1291, doi: 10.1109/TCSI.2005.851387

4 Hazucha, P., Karnik, T., Bloechel, B.A., Parsons, C., Finan, D., and Borkar, S.: 'Area-efficient linear regulator with ultra-fast load regulation', *J. Solid-State Circuits*, 2005, **40**, (4), pp. 933–940, doi: 10.1109/JSSC.2004.842831

5 Guo, J., Ho, M., Kwong, K.Y., and Leung, K.N.: 'Power-area-efficient transient-improved capacitor-free FVF-LDO with digital detecting technique', *Electron. Lett.*, 2015, **51**, (1), pp. 94–96, doi: 10.1049/el.2014.3330

6 Zhan, C., and Ki, W.-H.: 'Analysis and design of output-capacitor-free low-dropout regulators with low quiescent current and high power supply rejection', *Trans. Circuits Syst. I, Regul. Pap.*, 2014, **61**, (2), pp. 625–636, doi: 10.1109/TCSI.2014.2300847