Improved Switched-Capacitor Interpolators with Reduced Sample-and-Hold Effects

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***Abstract*—This paper proposes improved switched-capacitor (SC) interpolators using a novel sampling technique which eliminates the undesired distortion due to the sample-and-hold shaping effect at the lower input sampling rate. Such a sampling technique not only leads to a precise analog interpolation, as its digital counterpart does, but also allows to simplify the design procedures and resulting SC circuit implementations. Different circuit topologies with both finite- and infinite-impulse response characteristics are developed, respectively, for low- and high-selectivity filtering. Practical implementation issues are discussed with respect to capacitance ratio mismatches, as well as finite gain, bandwidth, and offset sensitivity effects of operational amplifiers. Besides detailed computer-based analyses, experimental results obtained from discrete component prototypes are also presented to demonstrate the proposed circuits.**

***Index Terms*—CMOS analog integrated circuits, filtering, integrated circuit design, interpolation, multirate signal processing, sampled data circuits, signal sampling/reconstruction, switched-capacitor filters.**

I. Introduction

MULTIRATE sampled-data analog (SDA) circuits were first introduced as a means of relaxing the requirements of continuous-time pre- and post-filters in the context of traditional SDA filtering systems [1], [2]. Their usage has since then been extended to many more applications in order to achieve improved operating performance at the minimum cost in terms of silicon area and power dissipation [3]. Notable examples include high-selectivity interface filtering [4], data-acquisition systems [5], high-speed analog interfaces for video coders/decoders [6], [7], magnetic disk-read channel coders [8], and analog interfaces for wireless CMOS transceivers [9]–[12].

Various circuit architectures for multirate SDA circuits have been developed using switched-capacitor (SC) techniques [1]–[18]. SC linear interpolators have been proposed initially by taking advantage of input sample-and-hold (S/H) signal for achieving their desired responses [1], but were not accurate enough for many applications. To obtain a more precise interpolation, conventional bi-phase SC filters operating at a higher output sampling rate have also been used [5], [9]. Such approach has the advantage of employing well-known SC circuit architectures, but its response is distorted by the $\sin x/x$ shaping effect at a lower input sampling rate, and for high-frequency applications it leads to higher power and larger silicon area consumption. Specialized multirate SC interpolators [2], [14]–[17] have also been developed based on polyphase structures that could take advantage of the sampling rate increase inherent in the interpolation process [19].

For finite-impulse response (FIR) transfer functions, direct-form (DF) polyphase [2], parallel-cyclic (PC) polyphase [17], and differentiator-based (DB) nonrecursive polyphase [16] SC interpolators have been proposed. The former DF and PC architectures are not practical for high-selectivity filtering due to the resulting large number of SC branches and clock phases, which degrade the circuit performance with increased sensitivity to both capacitance ratio mismatches and switch timing. On the other hand, all these three architectures cannot make good use of the inherent superiority of polyphase structures, i.e., low-speed operation at input lower rate. For infinite-impulse response (IIR) transfer functions, optimum SC interpolator building blocks combining first- and second-order recursive sections together with DF polyphase networks have also been proposed [14], [15], employing output accumulators based either on a high-speed amplifier or on parasitic-sensitive unity-gain buffer. These specialized multirate SC interpolators, however, require a more complicated design due to the need of modifying the original digital interpolating transfer function according to

$$H'(z) = H(z) \cdot \sum_{l=0}^{L-1} z^{-l} \tag{1}$$

to account for the S/H shaping effect at the input lower rate [2].

This paper proposes improved SC interpolators using a novel sampling technique which eliminates the input S/H shaping effect, and thus operates in a similar way as its digital counterparts. Such interpolators are based on polyphase structures synthesized from the original prototype digital interpolation filter transfer function without any modification. Two types of SC circuit are proposed for optimum implementation. One employs a novel L-output-accumulator approach suitable for high-frequency operation, while another employs a one-output-accumulator approach yielding a reduced component count. After this introductory section, we discuss in Section II the analytical model of the new improved analog interpolation process with a comparison to the conventional one. Then, in Section III, the improved DF and active-delayed block (ADB) polyphase structures are presented together with their SC implementations for linear phase FIR interpolation. For IIR interpolation functions

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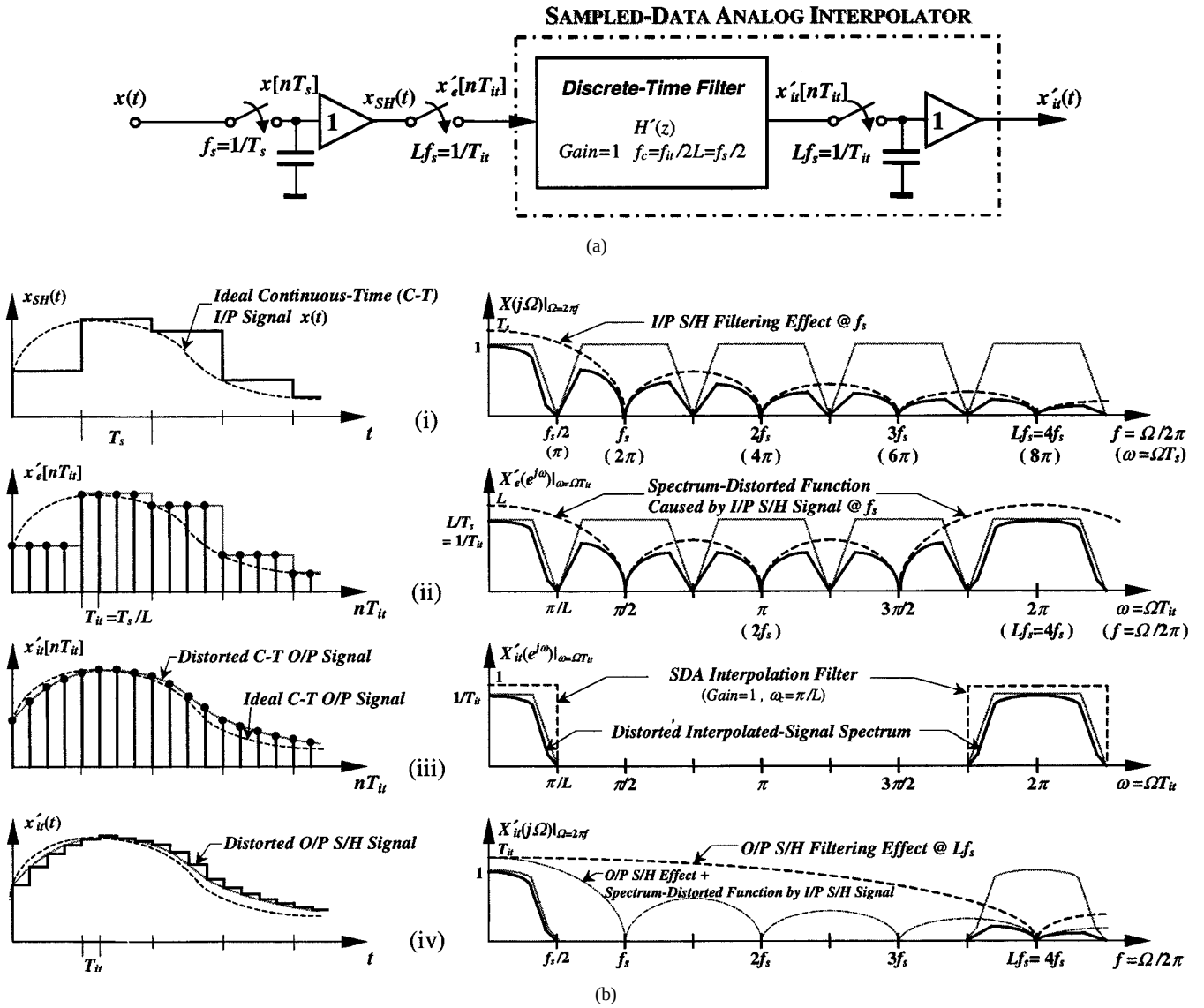


Fig. 1. SDA interpolation with integer conversion factor L (LP case). (a) Architecture model. (b) Time- and frequency-domain illustrations.

that are more suitable for high-selectivity or wide-stopband filtering, an efficient amplifier-shared combination of nonrecursive ADB polyphase structures and recursive DF II structures is investigated in Section IV. In Section V, the analysis will be focused on the power efficiency of such SC interpolators, together with the associated imperfections resulting from capacitance ratio inaccuracies, as well as finite-gain and bandwidth and input-referred offset effects of the operational transconductance amplifiers (OTA's). In addition to detailed computer simulations, experimental results obtained from discrete-component prototype realizations are presented in Section VI to validate the improved SC interpolation architectures. Finally, Section VII draws the conclusions of this paper.

II. Analog Interpolation

A. Digital versus Sampled-Data Analog Interpolation

Interpolation by a factor L is a process for a sampling rate increase from f_s to Lf_s and, in general, it can be carried out in either digital or SDA domains. Digital interpolation is a combined operation of an up-sampler, for increasing the sampling rate from f_s to Lf_s and inserting $(L\text{-}1)$ zero-valued samples between two consecutive input samples, and an interpolation filter, for removing the unwanted frequency-translated image components associated with the signal sampled at the input lower rate. The spectrum of the resulting ideal output interpolated samples $x_{\rm it}[nT_{\rm it}]$ is given by

$$X_{\rm it}(e^{j\omega}) = X_e(e^{j\omega}) \cdot H(e^{j\omega}) = X(e^{j\omega L}) \cdot H(e^{j\omega})$$
$$\omega = \Omega T_{\rm it} = \Omega T_s / L \tag{2}$$

where $X_e(e^{j\omega})$ and $X(e^{j\omega})$, respectively, are the spectrum of the up-sampled and the original samples, and $H(e^{j\omega})$ is the ideal frequency response of the interpolation filter (gain = L, cutoff frequency $\omega_c = \pi/L$, for lowpass (LP) case). Therefore, an ideal S/H interpolated output signal $x_{\rm it}(t)$ can be obtained by passing such interpolated samples through an ideal hold circuit, and its spectrum is represented by

$$X_{\rm it}(j\Omega) = X_{\rm it}(e^{j\Omega T_{\rm it}}) \cdot \frac{T_{\rm it}\sin(\Omega T_{\rm it}/2)}{\Omega T_{\rm it}/2} e^{-j\Omega T_{\rm it}/2} \tag{3}$$

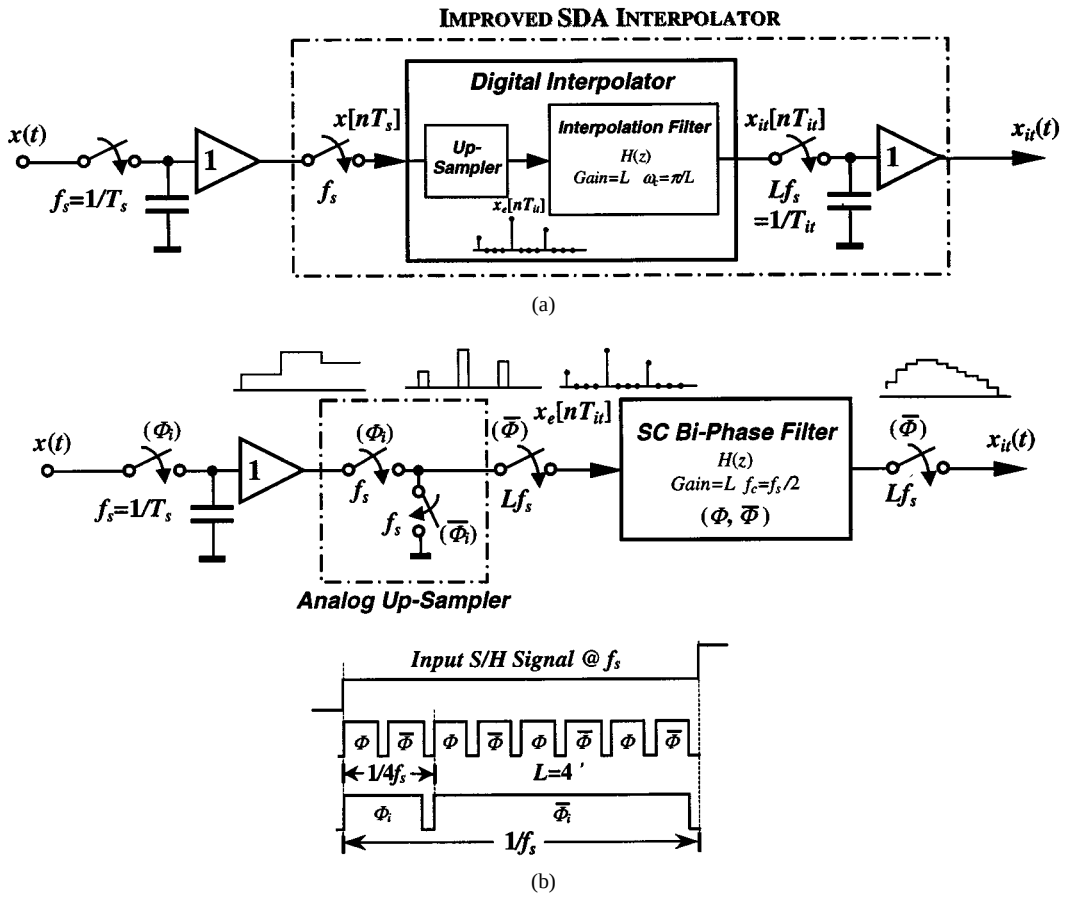


Fig. 2. Improved SDA interpolation with reduced S/H effects. (a) Architecture model. (b) Conventional implementation with a high-speed bi-phase SC filter.

In the SDA case, the exact interpolation (as in the above digital case) cannot be obtained due to the input S/H signal and it is described by the interpolation model in Fig. 1(a). The SDA interpolation filter, which can be analyzed as a discrete-time processor operating at Lf_s with an output hold at Lf_s, will sample and process the input signal at Lf_s (thus having L successive equal-value samples owing to the constant-held input within a full sampling period $1/f_s$) and its operation is depicted in Fig. 1(b), both in time and frequency domains. The spectrum of the input S/H samples $x'_e[nT_{\rm it}]$ can be expressed in terms of the spectrum of the up-sampled discrete sequences $x_e[nT_{\rm it}]$ by

$$X'_e(e^{j\omega}) = X_e(e^{j\omega}) \cdot H^0_{SD}(e^{j\omega}) \tag{4a}$$

where

$$H^0_{SD}(e^{j\omega}) = \frac{\sin(\omega L/2)}{\sin(\omega/2)} \cdot e^{-j(L-1)(\omega/2)}, \qquad \omega = \Omega T_{\rm it} \tag{4b}$$

in which $|H^0_{SD}(e^{j\omega})| = L$, for ω = 0.

From (4), the spectrum of the processed samples in an SDA interpolator, as illustrated in Fig. 1(b-ii) , is a deformed version of $X_e(e^{j\omega})$ due to the amplitude shaping by $H^0_{SD}(e^{j\omega})$, which is referred as spectrum-distorted function with a dc gain of L caused by the sampling of constant-held input. Thus, a unity-gain interpolation filter ($H'(e^{j\omega}) = H(e^{j\omega})/L$) must be employed to process such samples, and the spectrum of the resulting output interpolated samples $x'_{\rm it}[nT_{\rm it}]$ is expressed as

$$\begin{aligned} X'_{\rm it}(e^{j\omega}) &= X'_e(e^{j\omega}) \cdot H'(e^{j\omega}) \\ &= X_e(e^{j\omega}) \cdot H^0_{SD}(e^{j\omega}) \cdot H'(e^{j\omega}), \quad \omega = \Omega T_{\rm it} \end{aligned} \tag{5}$$

which indicates that the spectrum of the output samples possesses an extra deformation due to the spectrum-distorted function $H^0_{SD}(e^{j\omega})$, as shown in Fig. 1(b-iii). After taking into account the inherent output S/H filtering effect at higher sampling rate, the spectrum of the distorted S/H output signal $x'_{\rm it}(t)$ shown in (b-iv) of Fig. 1 can finally be represented by

$$X'_{\rm it}(j\Omega) = X_{\rm it}(e^{j\Omega T_{\rm it}}) \cdot \frac{T_s \cdot \sin(\Omega T_s/2)}{\Omega T_s/2} e^{-j(\Omega T_s/2)} \tag{6a}$$

or

$$X'_{\rm it}(j\Omega) = X_{\rm it}(j\Omega) \cdot \left(\frac{1}{L} \cdot H^0_{SD}(e^{j\Omega T_{\rm it}})\right) \tag{6b}$$

in terms of the ideal interpolated discrete samples or S/H signal, respectively. Obviously, for an integer sampling rate increase, an L-fold SDA interpolation is just equivalent to an ideal L-fold digital interpolation plus the S/H $(\sin x/x)$ effects no longer at the normally higher output sampling rate (as in (3) for ideal case) but at lower input sampling rate. In other words, from (6b) the final output S/H signal of an SDA interpolator suffers from an extra distortion due to the spectrum-distortion function.

B. Improved Analog Interpolation with Reduced S/H Effects

Such additional fixed-shaping spectrum distortion in analog interpolation usually gives rise to a significant rolloff deformation in the passband when the baseband signal is wide or close to the lower input sampling rate which is usually the case for high-speed applications (like video systems). Also, this affects the overall system response when frequency-translated bandpass (BP) processing is required (like subsampling in wireless communications). Hence, a new improved SDA interpolation whose model is shown in Fig. 2(a) is proposed in this paper to eliminate such fixed-shaping spectrum distortion, thus leading to an increased simplification and freedom in design for both passband and stopband. Although the input signal is still sampled-and-held at a lower rate, the ideal overall interpolation performance will be exactly equivalent to a digital interpolation, apart from the S/H effect at the higher sampling rate that is always present in SDA systems.

A conventional approach of this improved SDA interpolation, as shown in Fig. 2(b), can be implemented by the combination of a bi-phase SC filter operating at Lf_s with a special sampling by a front two-switch input interface which operates as an up-sampler by forcing the circuit input to connect to ground at the appropriate time, thus generating zero-valued samples. Such a special sampling technique for improved SDA interpolation can be equivalently achieved by the polyphase structures based on the original digital prototype interpolation transfer function and without any modifications that were previously required. For easier explanation, this is illustrated in Fig. 3, considering an example where an input signal is required to be twofold interpolated according to a simple three-tap FIR function. The original digital transfer function for interpolation filter is decomposed into a set of L polyphase filters $\{H_m(z), m = 0, 1, 2, \ldots, L-1\}$ [19]

$$\begin{aligned} H(z) &= \sum_{m=0}^{L-1} H_m(z) \cdot z^{-m} \\ &= \sum_{m=0}^{L-1} \left(\sum_{i=0}^{I_m - 1} h_{m+iL} z^{-iL} \right) \cdot z^{-m} \\ I_m &= \left\lfloor \frac{N-m}{L} \right\rfloor \end{aligned} \tag{7}$$

where the unit delay refers to the output sampling frequency Lf_s and $\lfloor (N-m)/L \rfloor$ denotes the minimum integer greater than or equal to $(N-m)/L$. In the resulting polyphase structure derived in Fig. 3, all polyphase filters are realized in a DF structure. The first polyphase filter produces an output sample given by

$$x_{\mathrm{it}}[nT_{\mathrm{it}}] = h_0 \cdot x[nT_{\mathrm{it}}] + h_2 \cdot x[(n-2)T_{\mathrm{it}}] \tag{8a}$$

which is equivalent to having multiplied the coefficient h_1 by a zero-valued sample. Similarly, since the second polyphase filter produces an output sample given by

$$x_{\mathrm{it}}[(n+1)T_{\mathrm{it}}] = h_1 \cdot x[nT_{\mathrm{it}}] \tag{8b}$$

it is also identical to multiplying by zero the coefficients h_0 and h_2. Thus, such operation is equivalent to a digital interpolation filter processing the zero-valued samples from the up-sampler.

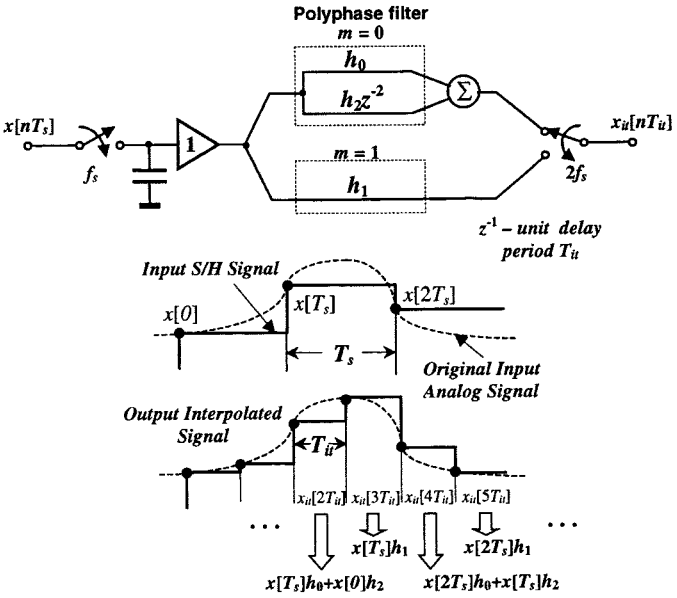


Fig. 3. Improved SDA interpolation with a novel sampling technique by DF polyphase structure $(L = 2)$.

In general, it can be concluded that the DF polyphase interpolation, with original digital prototype transfer function, implements an improved SDA interpolation without the input S/H filtering effect. Since every polyphase filter inherently operates at the lower input sampling rate, the input-held signal is only sampled by the interpolator once per period. This also explains why the input S/H effect does not affect the overall system response of the polyphase-structure-based interpolator.

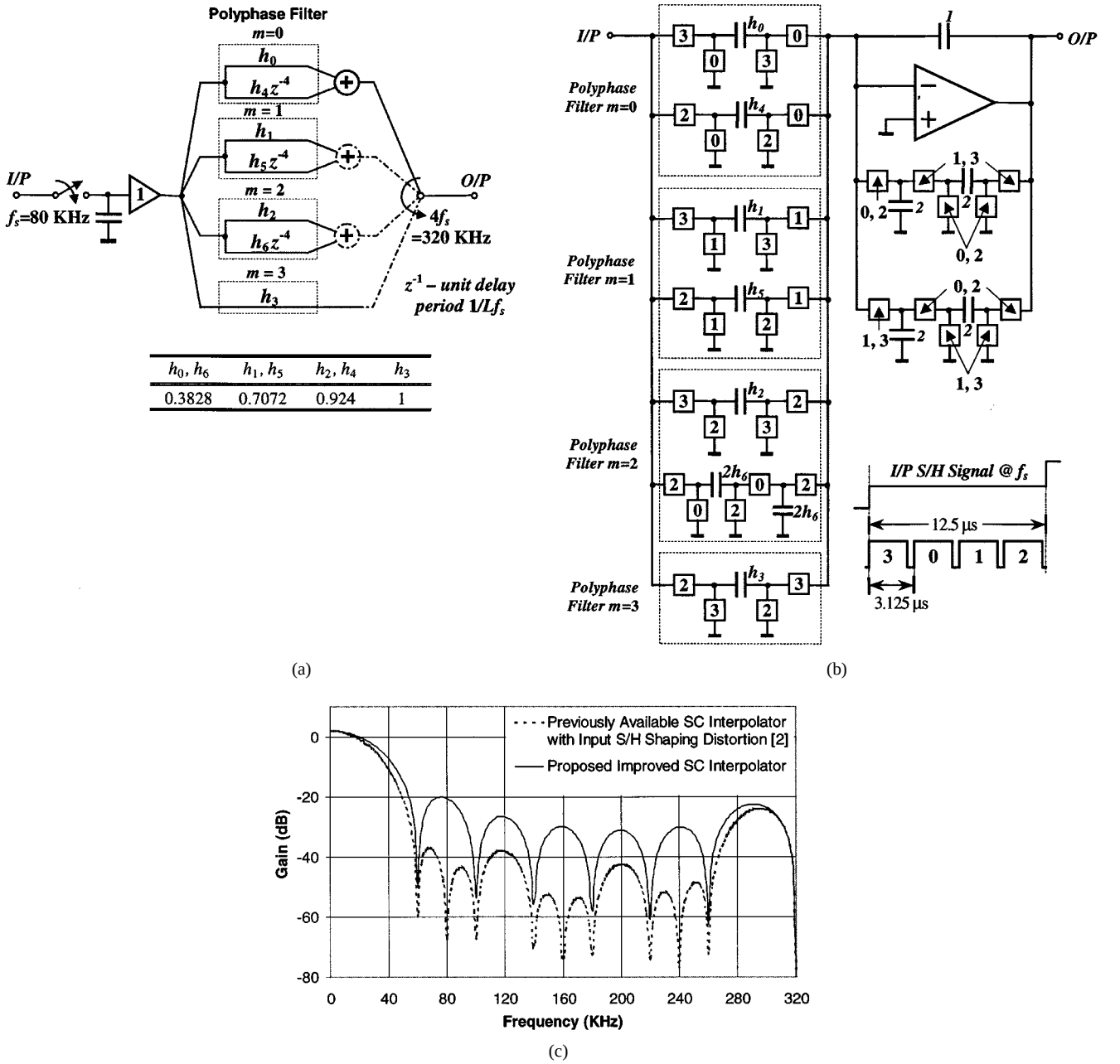
III. Improved FIR SC Interpolators

A. DF Polyphase Structure

For simplicity, we begin by considering an example of a seven-tap FIR LP interpolator [2] with sampling rate increase $L = 4$, from $f_s = 80$ kHz to $4f_s = 320$ kHz, for a narrow SC BP system (midband frequency at $f_o = 20$ kHz).

According to (7), the DF polyphase structure and its corresponding SC circuit architecture, are derived in Fig. 4(a) and (b), respectively, with the interpolated output samples produced by four polyphase filters in time slots 0, 1, 2 and 3. The simulated amplitude response shown in Fig. 4(c) demonstrates that the amplitude response of the proposed SC interpolator is free from the S/H shaping effect at the lower sampling rate. For comparison, the response of the SC interpolator previously available [2] for the same interpolation function by employing a modified transfer function is also plotted in Fig. 4(c), clearly showing its distorted response by the input S/H effect.

Besides the distortion-free response, the proposed improved SC circuit also offers extra advantages over the previous circuits [2], [16], [17], [20] in terms of the capacitance spread and total capacitor area, required SC branches, clock phases, and speed of the OTA's, as demonstrated in Table I. It is significant to point out that the reduction in capacitance spread (L times) and capacitor area is mainly attributed by the special gain scaling (L times) imposed by the proposed novel sampling techniques for improved SC interpolation.



h_0, h_6	h_1, h_5	h_2, h_4	h_3
0.3828	0.7072	0.924	1

(a) (b) (c)

Fig. 4. Improved fourfold SC DF polyphase LP interpolator. (a) DF polyphase structure. (b) SC circuit implementation. (c) Simulated amplitude responses.

TABLE I
A COMPARISON BETWEEN NEW IMPROVED AND ORIGINAL [2] SC INTERPOLATORS

	Original Design [2]	Improved Design (Fig.4)
SC Coefficient Branches	12	7
Cap. Spread	10.45	2.61 (L times smaller)
Total Cap. Area	77.29	23.97
Max. OTA Settling Time	1.042 µs (=1/3Lf_s)	3.125 µs (=1/Lf_s)
Clock Phases	15	4 (=L)
Input S/H Distortion	Yes	No

B. Canonic and Non-Canonic ADB Polyphase Structures

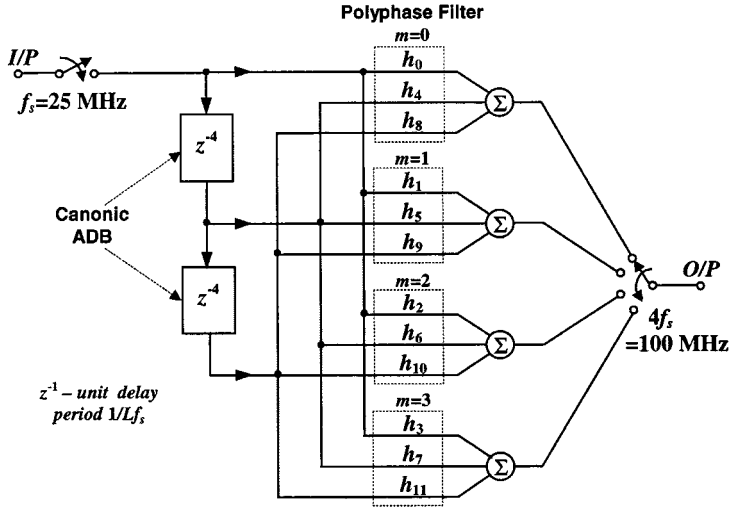
The DF polyphase SC implementation is appropriate only when the FIR filter length N is not much greater than the interpolation factor L, e.g., $N \leq 2L$, since it leads to circuits having a rather large number of SC branches and switching phases, which increase not only its complexity beyond practical acceptable limits, but the sensitivity to mismatch of capacitance ratios and switch timing [13], [21]. For $N > 2L$, such limitations can be overcome by using instead the ADB polyphase architecture.

The FIR transfer function can be canonically decomposed in $B_c + 1$ blocks, each of which has only L coefficients, and can be expressed as

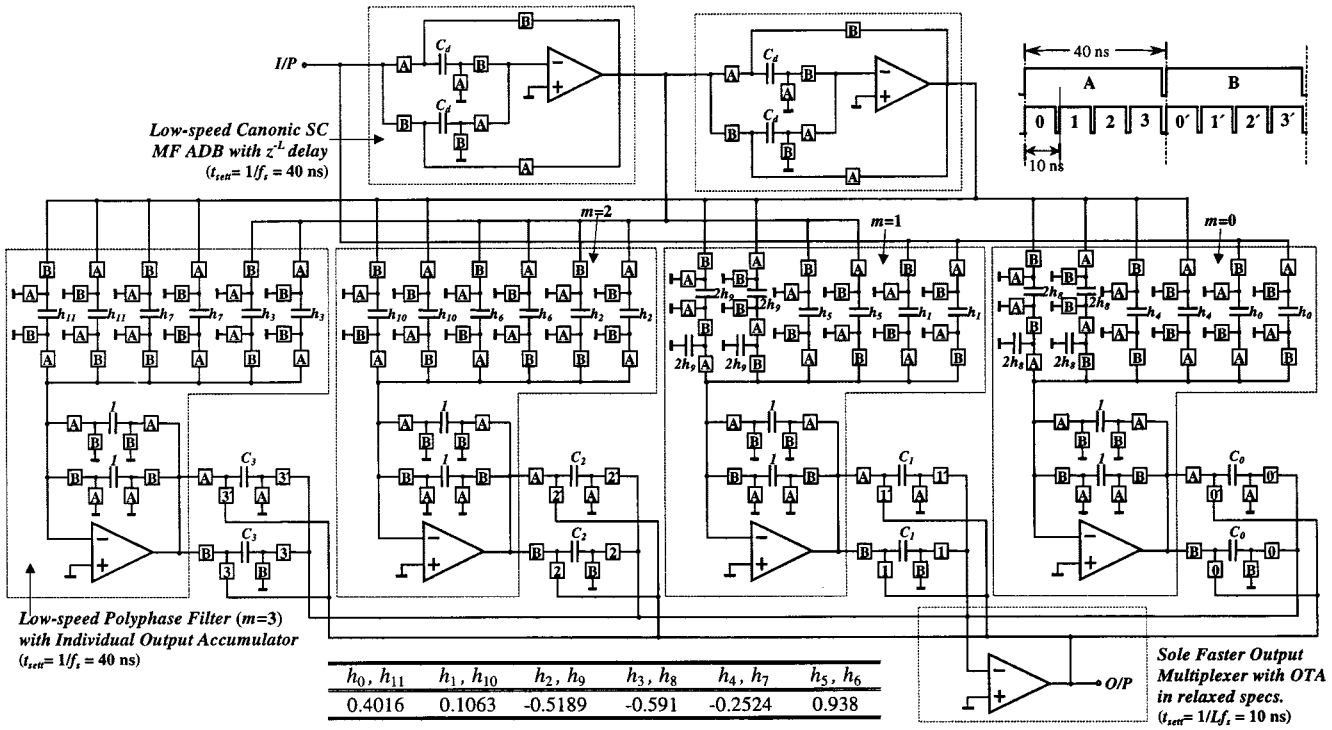
$$H(z) = \sum_{n=0}^{N-1} h_n z^{-n} = \sum_{b=0}^{B_c} \left(\sum_{n=0}^{L-1} h_{n+bL} z^{-n} \right) \cdot (z^{-L})^b$$

with

$$B_c = \left\lfloor \frac{N-L}{L} \right\rfloor. \tag{9}$$

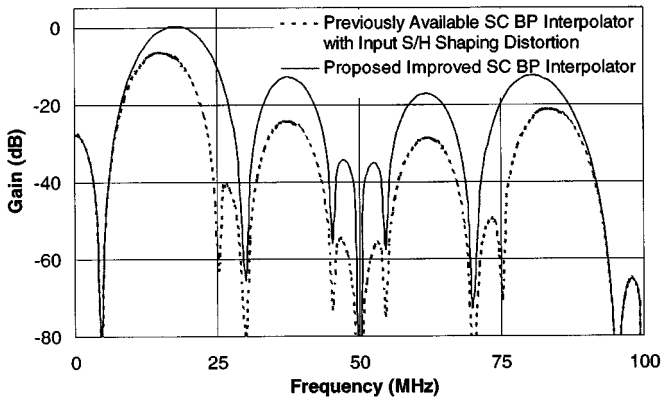


(a)



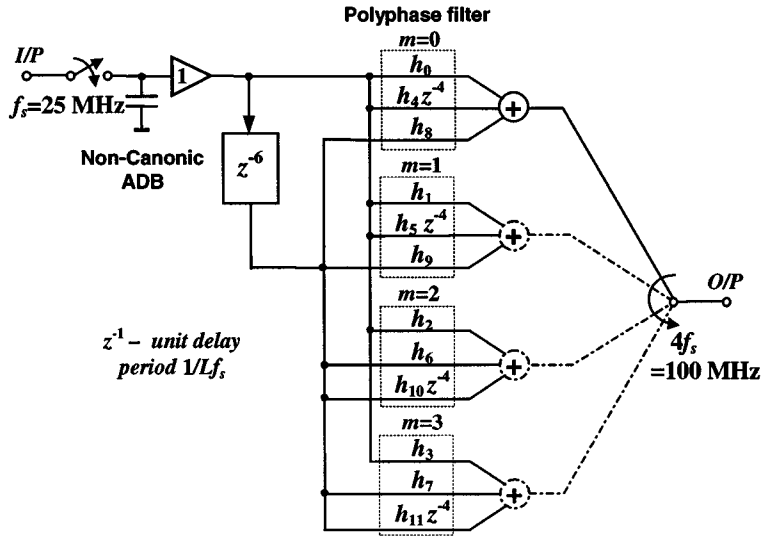
h_0, h_{11}	h_1, h_{10}	h_2, h_9	h_3, h_8	h_4, h_7	h_5, h_6
0.4016	0.1063	-0.5189	-0.591	-0.2524	0.938

(b)

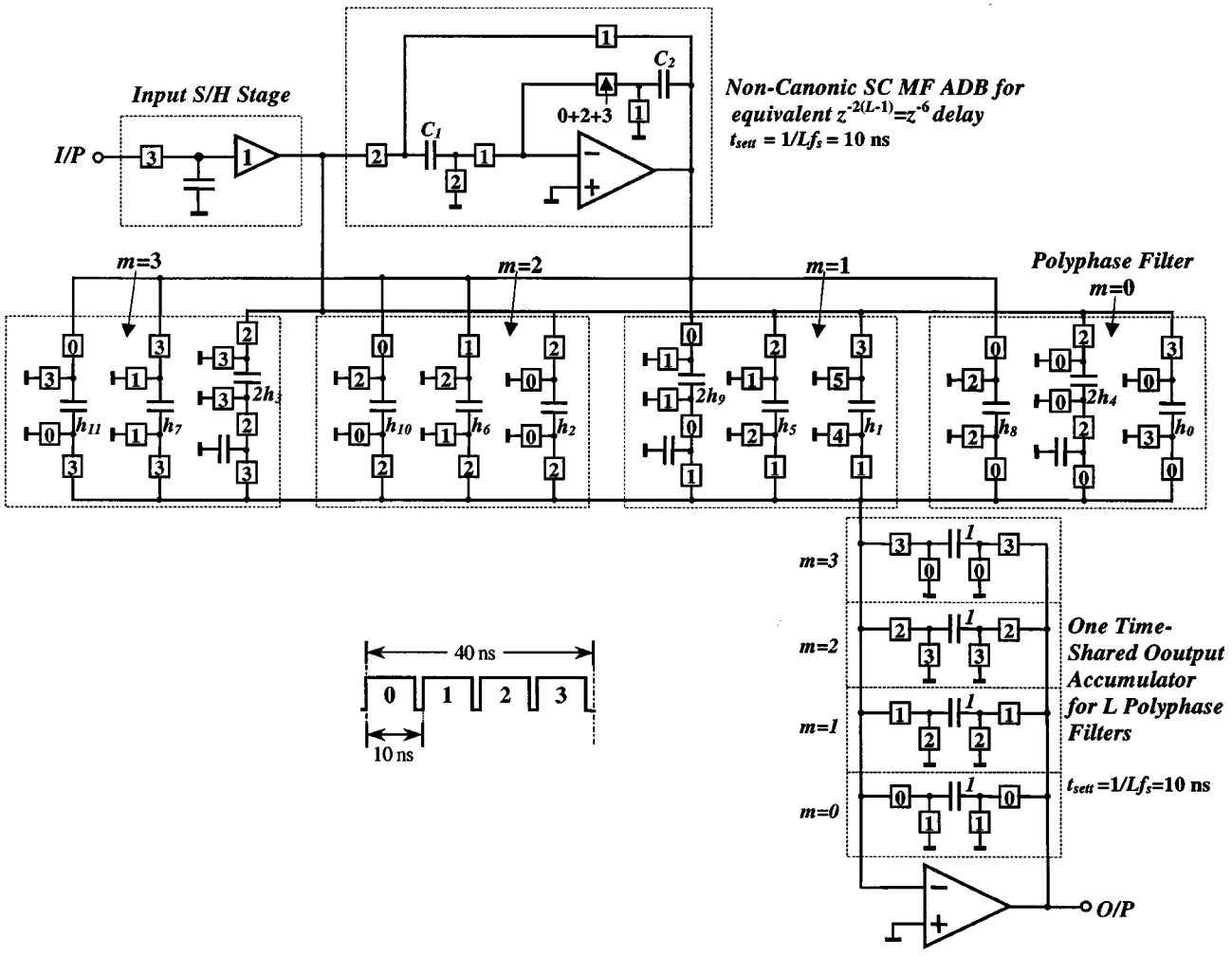


(c)

Fig. 5. Improved fourfold SC FIR BP interpolator with canonic ADB polyphase structure. (a) Canonic ADB polyphase structure. (b) SC circuit implementation. (c) Simulated amplitude responses.



(a)



(b)

Fig. 6. Improved fourfold SC FIR BP interpolator with non-canonic ADB polyphase structure. (a) Non-canonic ADB polyphase structure. (b) SC circuit implementation.

The elements in each block b will have at least b delay terms z^{-L} (except $b = 0$) that will be implemented by an SC ADB. Since each block containing L coefficients (except the last block, $b = B_c$, which contains only $N - B_cL$ blocks) can be realized by a DF polyphase structure with the sharing of a low-speed serial ADB delay line, this structure is designated as a *canonic ADB polyphase* structure [21]. Such enhancement in DF polyphase structure also suc^{^{ceeds in the inherent immunity to the input S/H distortion.

To illustrate the concept above, let us consider an example of a frequency-translated BP interpolator for a direct digital frequency synthesis (DDFS) system that interpolates a 4.5–5 MHz bandwidth input signal to a 20–20.5 MHz output signal, together with a sampling rate increase from 25 to 100 MHz. This fourfold BP interpolator is realized by the canonic ADB polyphase structure shown in Fig. 5(a) for achieving a 12-tap FIR function (gain $= 4$). The corresponding SC circuit with also the employment of double-sampling technique is shown in Fig. 5(b). The upper part forms a low-speed serial ADB delay line by two SC mismatch-free (MF) L-unit delay circuits, which have also a better reduction in the errors that will be accumulated along the delay line due to the finite gain and bandwidth, as well as offset of OTA when comparing to general charge-transferred delay circuit. By taking one of the most efficient advantage of polyphase structures, namely relaxed operation speed at the lower input sampling rate, the bottom half of the circuit contains L low-speed DF polyphase filters by employing their corresponding individual slow accumulators, each of which is responsible for generating one of L output samples at a lower input sampling rate. This contrasts with the solution adopted in Fig. 4, where only one time-shared output accumulator was used to produce all L interpolated outputs at a higher output sampling rate. Thus, all the OTA's in ADB's and accumulators have a very relaxed settling-time requirement of full large-input sampling period (40 ns), which is L times longer than that of OTA's if a conventional double-sampling bi-phase filter is used. This also contributes to the reduction of the noise, charge injection, and clock-feedthrough errors in SC circuits. L parallel toggle-switched capacitor (TSC) branches followed by an output unity-gain buffer can be simply used as a multiplexer for switching the interpolated output from four polyphase filters. We also propose here another simple high-performance MF SC multiplexer which can employ the well-known fully differential and bottom-plate sampling techniques to eliminate the signal-dependent charge-injection and clock-feedthrough errors that are unavoidably suffered in the aforementioned unity-gain buffer approach. Although it operates at higher output sampling rate (10-ns settling time—full output period), the feasibility is derived from the fact that specifications of the multiplexer OTA are much less stringent than those in ADB's or accumulators if operating at the same speed. This is because first, the OTA always operates with a large feedback factor ($>$0.5 when the sampling capacitor is greater than input parasitics capacitance of OTA), thus reducing its bandwidth or transconductance requirements. Compared with those formed by a set of coefficient capacitors (for OTA's in ADB's) with a large summing feedback capacitor (for OTA's in accumulators), the relatively smaller total equivalent capacitive loading together with usually smaller output voltage step during two consecutive phases (due to the sampling rate increase nature) normally relax the OTA slew-rate and bandwidth requirements which are all directly proportional to the OTA power consumption. If it needs to drive a large capacitive or resistive load, then buffers with low output-impedance are normally required for better performance in OTA-based analog circuits. Thus, especially in LP systems, the power of this multiplexer OTA can be even smaller than OTA's with wider settling time in ADB's (presented next). Moreover, the errors caused by finite-gain and offset of this MF multiplexer will introduce small and less important deviation, and mostly just a gain shift and a dc offset in overall system response, and its elimination of charge-transfer reduces not only the mismatch error for each path, but the special glitches in the output signal caused by the OTA high output-impedance, and normally appears in the beginning of the charge-transfer in OTA-based SC circuits. Consequently, the canonic ADB structure is very attractive for high-frequency operation.

The simulated output amplitude response of this circuit is shown in Fig. 5(c), together with the response from previously available interpolator with the additional input S/H distortion. In this frequency-translated operation, the distortion about 10 dB in the passband is much more serious than that of previous narrowband DF polyphase interpolator.

Minimizing the number of OTA's in an ADB architecture can be achieved by reducing the number of both ADB's and accumulators. Fewer ADB's can be obtained by decomposing the transfer function into blocks with more-than-L coefficients, while making their shared delays larger than z^{-L}. Such a realization is called a *non-canonic ADB polyphase* structure, and can be obtained by decomposing the transfer function of an interpolation filter into $B_{\rm nc}+1$ blocks, each with at most $2(L-1)$ coefficients, yielding

$$H(z) = \sum_{n=0}^{N-1} h_n z^{-n} = \sum_{b=0}^{B_{\rm nc}} \left(\sum_{n=0}^{2(L-1)-1} h_{n+b\cdot 2(L-1)} z^{-n} \right) \cdot (z^{-2(L-1)})^b, \quad \text{with } B_{\rm nc} = \left\lfloor \frac{N-2(L-1)}{2(L-1)} \right\rfloor \tag{10}$$

The above same BP interpolator can be also implemented with the noncanonic ADB polyphase structure shown in Fig. 6(a), yielding the SC circuit illustrated in Fig. 6(b) with the MF SC delay line and only one time-shared output accumulator. This noncanonic realization saves one ADB and $(L-1) = 3$ output accumulators at the expense of narrowing the time slots for amplifier settling to $1/Lf_s$, which is nevertheless still better than that in [2], [16], [17], [20]. The new configuration of one output accumulator with multiplexed accumulation branches reduces the total capacitor area due to capacitance group scaling in each polyphase filter. The simulated circuit response is the same as that of the previous canonic one in Fig. 5(c). This structure normally has better performance in terms of capacitor-ratio sensitivity and gain and offset errors due to the fewer requirement of OTA's being more appropriate for the application where the speed is not the first concern.

IV. Improved IIR SC Interpolators

A. Canonic and Non-Canonic Recursive-ADB (R-ADB) Polyphase Structures

Efficient structures for implementation of IIR interpolators are also based on the polyphase structure, where the original Dth-order denominator and $(N-1)$th-order numerator IIR transfer function needs to be modified according to the multirate transformation in order to restrict the composition of denominator to only powers of z^{-L} [19]. Consequently, the original and the modified transfer functions can be expressed, respectively, as

$$H(z)=\frac{N(z)}{D(z)}=\frac{\sum_{i=0}^{N-1}a_i z^{-i}}{1-\sum_{j=1}^{D}b_j z^{-j}} \tag{11}$$

and

$$\hat{H}(z)=\frac{\hat{N}(z)}{\hat{D}(z)}=\frac{\sum_{i=0}^{(N-1)+D(L-1)}A_i z^{-i}}{1-\sum_{j=1}^{D}B_{jL}(z^{-L})^j}. \tag{12}$$

This particular form of (12), which allows the recursive part to operate at the lower input sampling rate, can be constructed by combining a nonrecursive ADB polyphase structure together with a recursive direct-form II (DFII) structure for realizing, respectively, the numerator and the denominator polynomials. Such architecture, where the common delay blocks (z^{-L}) are realized by a low speed ADB serial delay line and are efficiently shared by both recursive and nonrecursive parts, can be referred to as *R-ADB polyphase* structure [22]. This structure offers a more general, straightforward, and flexible design, with enhanced efficiency in terms of amplifier speed and number of phases over the previous structures [14], [15]. Moreover, since it evolves from the improved FIR ADB polyphase structure, the precise characteristic of improved interpolation is also maintained.

As in it's FIR counterpart, this R-ADB polyphase structure can also be implemented in canonic and noncanonic forms, categorized by the corresponding delay of the shared ADB's. The former has L unit delays, whereas the latter requires delays of $2(L-1)$ (except the first block that has always a unity delay due to the extra summing function in the first ADB). Thus, for a general case $(D \neq N-1)$, the IIR-modified transfer function (12) in canonic form, which requires $\max(B_{\rm cn}, B_{\rm cd})$ SC ADB's, is reformulated as

$$\hat{H}(z)=\frac{\sum_{j=0}^{B_{\rm cn}}\left(\sum_{i=0}^{L-1}A_{i+jL}z^{-i}\right)\cdot(z^{-L})^j}{1-\sum_{j=1}^{B_{\rm cd}}B_{jL}(z^{-L})^j}$$

with

$$B_{\rm cn}=\left\lfloor\frac{N+D(L-1)-L}{L}\right\rfloor,\quad B_{\rm cd}=D \tag{13}$$

while the noncanonic transfer function that requires $\max(B_{\rm ncn}, B_{\rm ncd})$ ADB's can be expressed as in (14), shown at the bottom of the page, where

$$p_j=\left\lfloor\frac{jL}{2(L-1)}\right\rfloor$$
$$B_{\rm ncn}=\left\lfloor\frac{N+D(L-1)-1}{2(L-1)}\right\rfloor,\quad B_{\rm ncd}=\left\lfloor\frac{DL}{2(L-1)}\right\rfloor.$$

It is obvious that a noncanonic structure requires fewer, though relatively high-speed OTA's due to the reduced number of ADB's and single accumulator. On the contrary, the canonic structure needs more, though slower OTA's, as in the FIR counterparts.

B. Complete-DFII (C-DFII) Realization

For simplicity, let us directly consider an LP interpolator for a video decoder which converts the 3.6-MHz bandwidth composite analog video signal from sampling at 10–30 MHz. For standard CCIR 601 8-bit accuracy requirement, a fourth-order elliptic filter with <0.4-dB passband ripple and $\geq$ 40-dB attenuation is obtained, and its original and multirate modified transfer-function coefficients are listed in Table II(a).

The corresponding canonic and noncanonic R-ADB polyphase structures in C-DFII realization are, respectively, shown in Fig. 7(a) and (b) by formulating its multirate transfer function into (13) and (14). The SC implementation of canonic form is similar to that for FIR circuit [Fig. 5(b)], except for the addition of the recursive branches from each ADB output to the first ADB/adder [22]. Here, only the circuit in noncanonic form is presented in Fig. 8(a), where an SC summing circuit embedding one unit delay is required to add recursive signals at the beginning of the SC MF ADB delay line. Note that the recursive networks contribute not only to the common delay

$$\hat{H}(z)=\frac{A_0+z^{-1}\cdot\sum_{j=0}^{B_{\rm ncn}}\left(\sum_{i=0}^{2(L-1)-1}A_{i+j\cdot 2(L-1)+1}z^{-i}\right)\cdot(z^{-2(L-1)})^j}{1-z^{-1}\cdot\sum_{j=1}^{D}\left(B_{jL}z^{-(jL-2(L-1)\cdot(p_j-1)-1)}\right)\cdot(z^{-2(L-1)})^{p_j-1}} \tag{14}$$

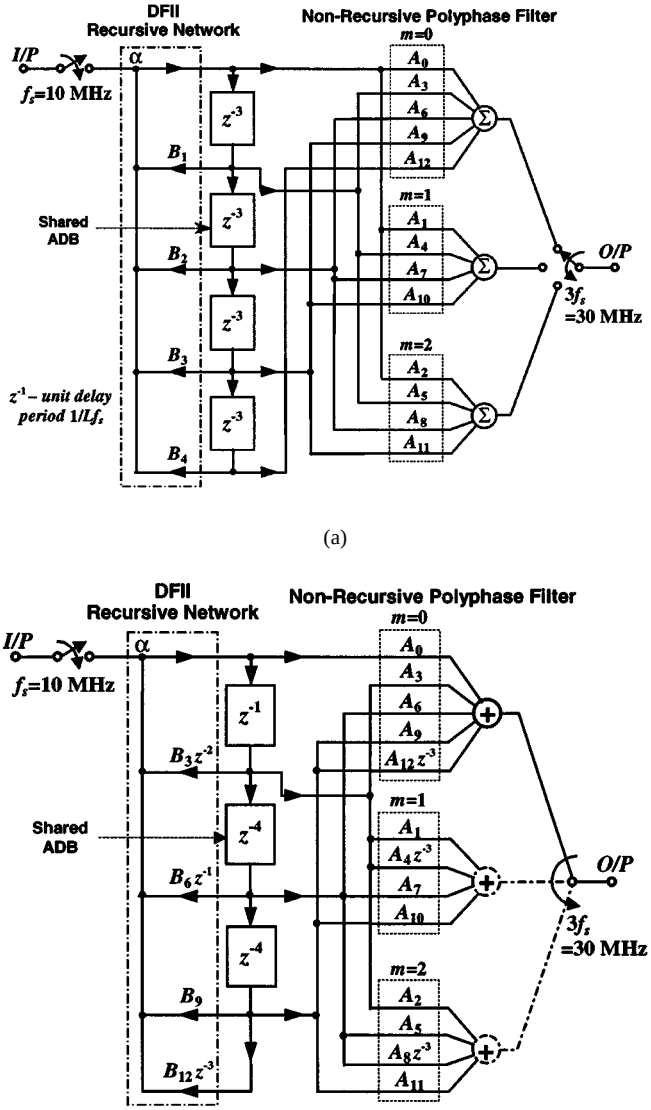
TABLE II
TRANSFER-FUNCTION COEFFICIENTS OF IMPROVED THREE-FOLD SC IIR LP VIDEO INTERPOLATORS. (a) ORIGINAL AND MULTIRATE MODIFIED COEFFICIENTS FOR ELLIPTIC AND ER IN C-DFII IN STRUCTURES. (b) MULTIRATE MODIFIED COEFFICIENTS FOR ELLIPTIC P-DFII AND MCP-DFII STRUCTURES

Original			Multirate Modified		
Eq. (12)	Elliptic (*D*=4)	ER (*N*=9, *D*=2)	*Eq.* (12)	Elliptic (*D*=4)	ER (*N*=9, *D*=2)
a_0	0.0958	0.1006	A_0	0.0958	0.1006
a_1	0.0808	0.2146	A_1	0.2927	0.3181
a_2	0.1554	0.3616	A_2	0.5807	0.6198
a_3	0.0808	0.4385	A_3	0.8945	0.9613
a_4	0.0958	0.4084	A_4	1.1316	1.1926
a_5		0.2868	A_5	1.1983	1.2257
a_6		0.1355	A_6	1.0592	1.0613
a_7		0.0415	A_7	0.8073	0.7813
a_8		-0.0249	A_8	0.5250	0.4620
			A_9	0.2741	0.2199
			A_{10}	0.1140	0.0836
			A_{11}	0.0351	0.0020
			A_{12}	0.0065	-0.0117
b_1	2.2112	1.0285	B_3	-0.9688	-1.0256
b_2	-2.3148	-0.6850	B_6	-0.3683	-0.3214
b_3	1.1918		B_9	-0.0082	
b_4	-0.2695		B_{12}	-0.0175	

(a)

Elliptic	P-DFII		MCP-DFII	
	Biquad 1	Biquad 2	Biquad 1	Biquad 2
A_0	0.0958	0	0.0958	0
A_1	-0.8309	1.1236	0.2927	0.8948
A_2	-0.4863	1.0670	0.5807	0.6083
A_3	0.1621	0.7406	0.9027	0.3340
A_4	-0.4429	0.3175	1.1568	0.0656
A_5	-0.0593	0.0900	1.2484	-0.0172
A_6	0.3027	-0.0149	1.1330	-0.0410
B_3	-1.0550	0.0862	-1.0550	0.0862
B_6	-0.4174	-0.0419	-0.4174	-0.0419

(b)



(a)

(b)

Fig. 7. (a) Canonic and (b) non-canonic R-ADB/C-DFII polyphase structures for improved threefold SC IIR LP video interpolator.

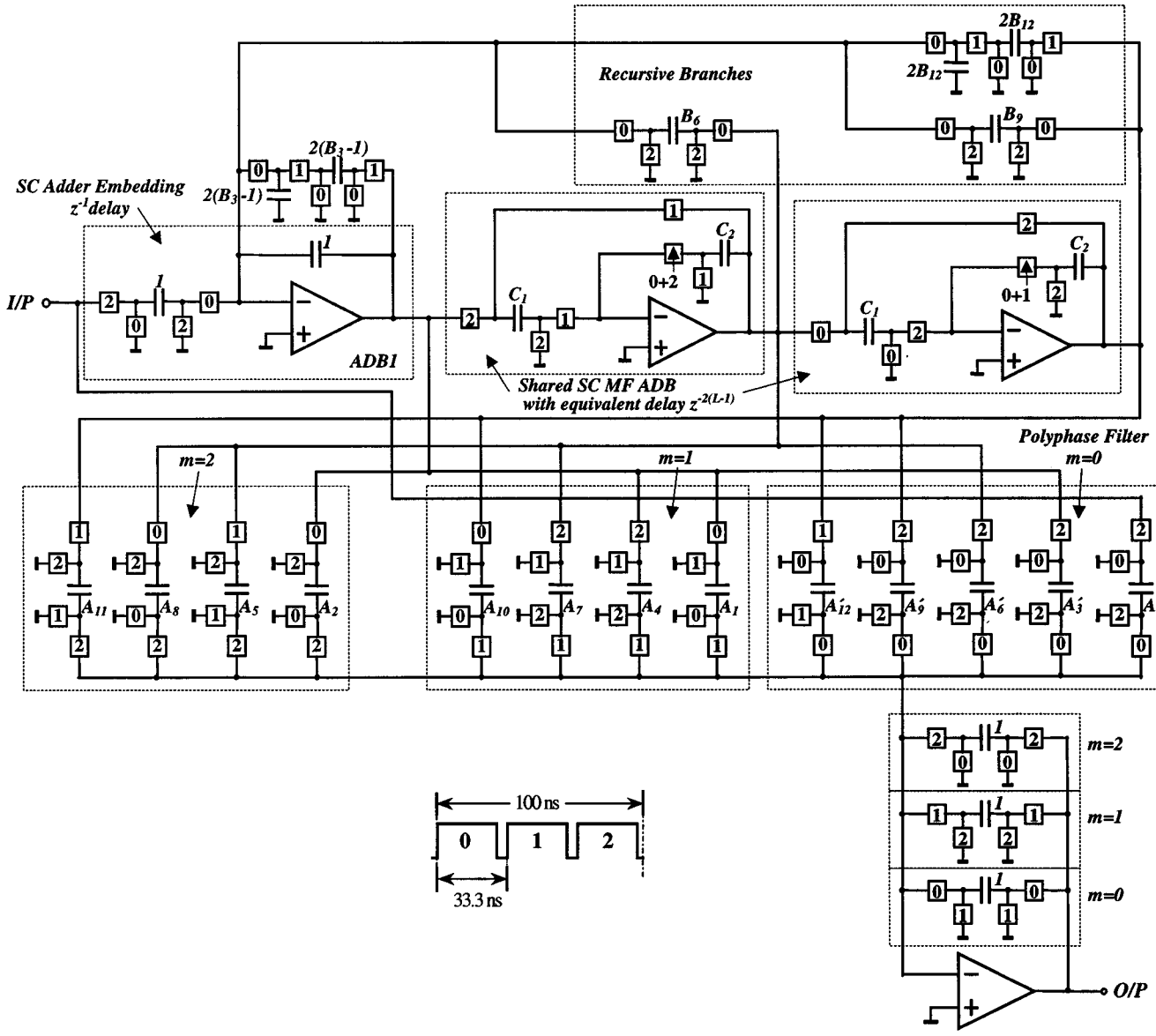
line but also to the nonrecursive SC branch A_0 (while for both A_0, A_1 and A_2 in canonic form) in the first polyphase filter at the same time, since input and recursive signals must originally be added together at node "α," as illustrated in Fig. 7(b). In order to save this adder (one extra OTA) and take advantage of both the existing output accumulator and of the OTA in the ADB, a coefficient-simplification procedure is proposed to the first polyphase filter based on two sets of the same recursive networks: one that feeds back to the input of ADB1, and another that feeds forward to the output accumulator, which can be efficiently combined together with existing nonrecursive branches. In other words, no extra SC branches are needed, e.g., A_3 is simplified to $A_3' = B_3 \times A_0 + A_3$ (similar for A_6, A_9 and A_{12}).

The simulated overall and passband amplitude responses are obtained in the solid line of Fig. 8(b). The passband satisfies the requirement (<0.4 dB), although there is 0.2-dB rolloff caused by the output sampling rate of 30 MHz, which is much better than the nearly 2-dB rolloff suffered from the input S/H distortion in the conventional SC interpolator.

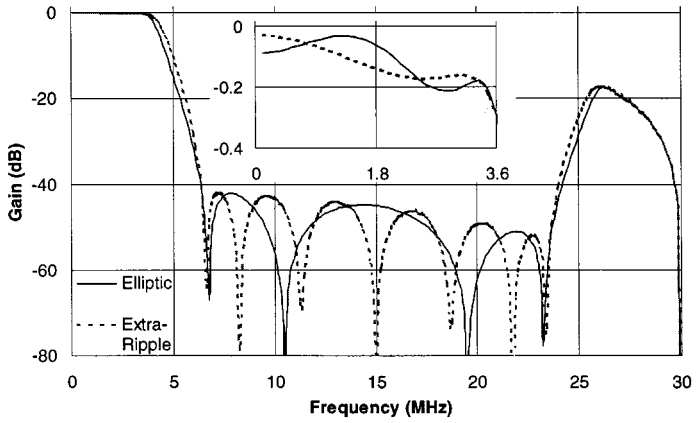
C. Parallel and Mixed-Cascade/Parallel DFII (MCP-DFII) Realizations

Although high-order IIR interpolators can be implemented directly in a single stage by employing the above R-ADB/C-DFII polyphase structures, cascade- or parallel-form structures are usually preferable for their lower sensitivity to coefficient deviation. Therefore, for interpolation with relatively smaller or prime L factors but higher IIR filter order, parallel form (P-DFII) structures can be simply achieved by expressing the rational transfer function in a partial fraction expansion and implementing it by the first- and second-order building blocks in parallel. Thus, the corresponding modified multirate transfer function can be expressed as

$$\hat{H}(z) = \sum_{i=1}^{S} \frac{\hat{N}_{p\_i}(z)}{\hat{D}_i(z)} \tag{15}$$



(a)

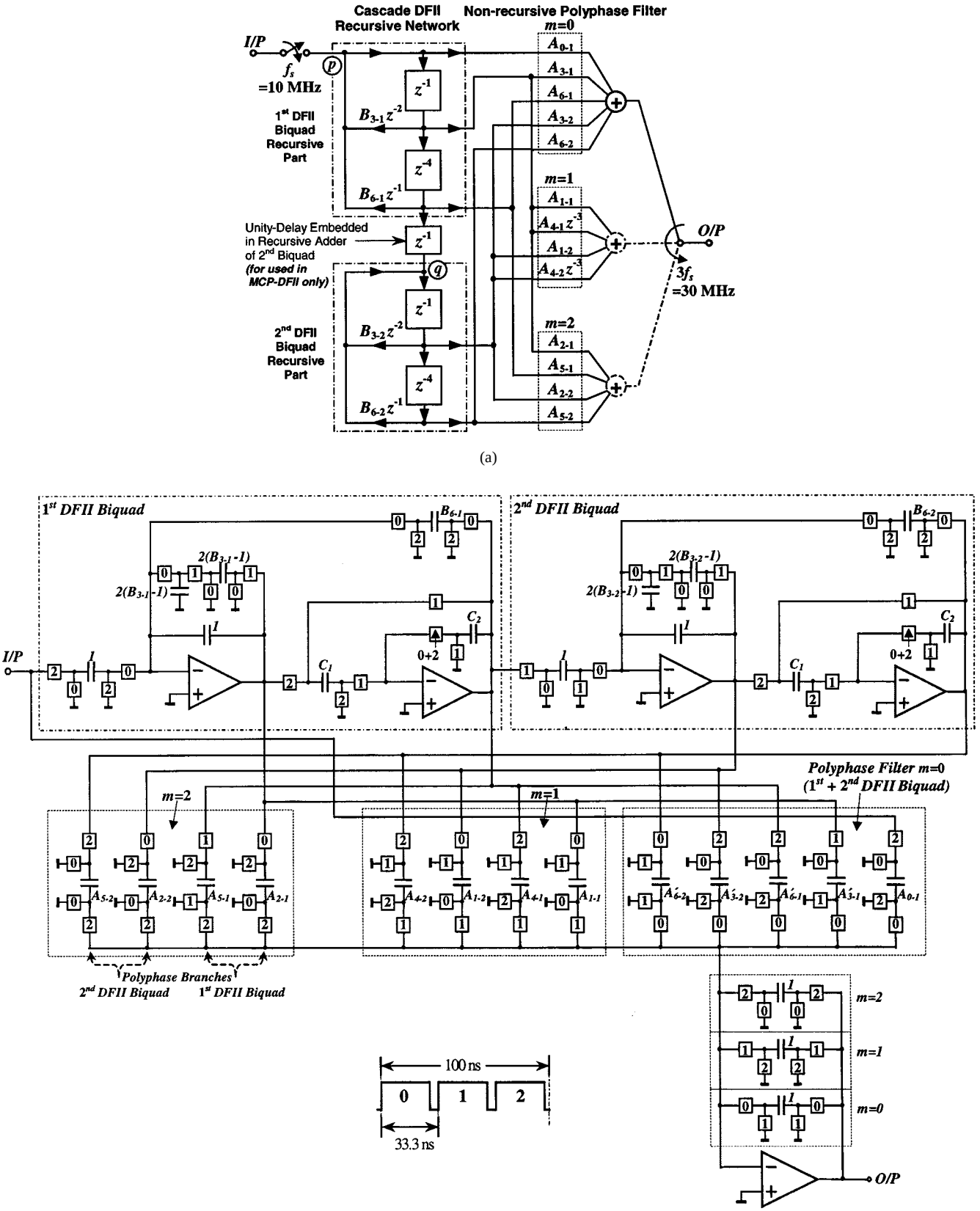


(b)

Fig. 8. Improved threefold SC IIR LP video interpolator with R-ADB/C-DFII polyphase structure. (a) Non-canonic SC implementation. (b) Simulated amplitude responses with elliptic and ER transfer function.

where S is the number of the stages, and each stage can be realized by the above DFII R-ADB polyphase structures.

Nevertheless, the cascade form normally has better sensitivity performance than the parallel form due to the indepen-



(a)

(b)

Fig. 9. Improved threefold SC IIR LP video interpolator with R-ADB/MCP-DFII polyphase structure. (a) Non-canonic R-ADB/MCP-DFII polyphase structure (for P-DFII: join the nodes p and q and take out the z^{-1} delay term). (b) SC circuit implementation.

dence of the errors in each section caused by both their poles and zeros deviation, while the sensitivity performance of parallel form highly depends on the output adder. However, the pure cascade form is actually a multistage implementation of

TABLE III
POWER ANALYSIS OF IMPROVED (a) FOURFOLD SC FIR BP INTERPOLATOR AND (b) THREEFOLD SC IIR LP VIDEO INTERPOLATOR WITH ER TRANSFER FUNCTION

	FIR Canonic			FIR Non-Canonic	
OTA	***MF ADB*** ×2	***Accu.*** ×4	***O/P Mul*** .×1	***S/H & MF ADB***	***Accu.*** ×1
t_{sett}	40 ns	40 ns	10 ns	10 ns	10 ns
SR (V_{ostep}= 1V)	125 V/μs	125 V/μs	500 V/μs	500 V/μs	500 V/μs
g_m	2.18 mS	1.55 mS	3.6 mS	7.02 mS	9.6 mS
I_{SS}	0.62 mA	0.31 mA	1.02 mA	1.74 mA	1.92 mA
No. of Use		×5	×2	×2	×1
Total Power	11.8 mW (3.3 V Supply)			17.8 mW (3.3 V Supply)	

(a)

	IIR Canonic				IIR Non-Canonic		
OTA	***R. Adder*** ×1	***MF ADB*** ×3	***Accu.*** ×3	***O/P Mul.*** ×1	***R. Adder*** ×1	***MF ADB*** ×2	***Accu.*** ×1
t_{sett}	100 ns	100 ns	100 ns	33.33 ns	33.33 ns	33.33 ns	33.33 ns
V_{ostep}	1 V	1 V	1 V	0.6 V	1 V	1 V	0.6 V
SR	50 V/μs	50 V/μs	50 V/μs	90 V/μs	150 V/μs	150 V/μs	150 V/μs
g_m	2.92 mS	0.65 mS	0.6 mS	0.65 mS	4.94 mS	2.7 mS	3.38 mS
I_{SS}	0.58 mA	0.22 mA	0.13 mA	0.13 mA	0.99 mA	0.73 mA	0.68 mA
No. of Use	×2			×6	×2		×2
Total Power	6.4 mW (3.3 V Supply)				11 mW (3.3 V Supply)		

Note: The highest g_m and I_{SS} are presented for the OTA's in ADB's and accumulators.

(b)

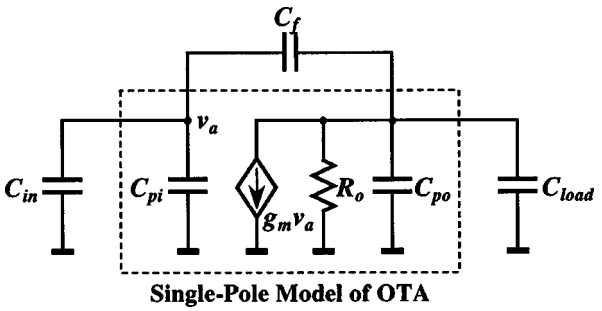


Fig. 10. Equivalent continuous-time model of the SC circuit during charge-transfer phase.

interpolation that is only suitable for large or nonprime alteration factor L due to its inherent nonidentity of input and output sampling rate. Therefore, here we propose another alternative: the MCP-DFII structure, which is a combination of a cascade of low-order recursive DFII parts and a multifeedout parallel nonrecursive polyphase filters (so called "internally-cascaded" [23]), and is especially suitable for sampling-rate conversion. The cascade of recursive parts leads to a considerably large reduction in the dependency between coefficient sensitivity and output adder, thus improving significantly the overall circuit sensitivity performance. In this case, the modified transfer function can be mathematically decomposed into the form as

$$\hat{H}(z) = \sum_{i=1}^{S} \left(T_i(z) \cdot \frac{\hat{N}_{\mathrm{MCP}\_i}(z)}{\prod_{j=1}^{i} \hat{D}_j(z)} \right) \tag{16}$$

where the $T_i(z)$ is the accumulated delay factor introduced by the cascade of recursive parts and $T_1(z) = 1$. An optimized choice of this delay factor will render a better performance, and the idea is actually to lower the peak of gain of each cascaded stage.

We further explain them by illustrating the same fourth-order video interpolator. The coefficients of modified multirate transfer function for P-DFII and MCP-DFII ($T_2(z) = z^{-6}$) realizations are all tabulated in Table II(b), and their corresponding R-ADB polyphase structures are shown in Fig. 9(a) (for P-DFII, join the nodes p and q and take out the middle unity delay). As will be illustrated in the next section, MCP-DFII structure offers a much better performance than C-DFII and P-DFII, especially for high-order function. Hence, we only present in Fig. 9(b) the SC implementation of MCP-DFII structure in noncanonic form for easy comparison with the previous circuits, although canonic form is also equivalently applicable, and the P-DFII one can also be derived similarly. Note that the output accumulators of polyphase filters in these two second-order sections are efficiently shared. Moreover, both PF- and MCP-DFII always offer an extra superiority of reduced capacitor spread, e.g., maximum coefficient spread for C- , PF-, and MCP-DFII are 209, 67, and 58, respectively, in this example. The simulated result is the same as for C-DFII shown in the solid line of Fig. 8(b).

D. Extra-Ripple (ER) IIR Transfer Function Realizations

Another alternative technique for IIR interpolation uses the ER-type IIR transfer function obtained by the improved Martinez/Parks algorithm [24] for achieving better sensitivity in passband due to its advantage of smaller denominator order, by optimum positioning poles and zeros [24]–[26]. For

the same specifications of the above video interpolator, the original ER IIR transfer function is obtained in Table II(a) with a lower second-order denominator, but with the price of a higher eighth-order numerator $(N = 9, D = 2)$. However, its multirate modified transfer function has a lower denominator order of six, but, more importantly, exactly the same order of 12 in numerator when compared with that of the fourth-order IIR elliptic, as shown in Table II(a), meaning no penalty for an increasing number of zeros, which shows its additional superiority for the use in multirate circuits. It has an identical implementation in R-ADB/C-DFII structure with either canonic or noncanonic form as in Fig. 7 but with two fewer recursive branches. If higher denominator order is required, both P-DFII and MCP-DFII realizations can also be preferably employed. The simulated results for their corresponding SC circuits in both canonic and noncanonic forms are the same, and are illustrated in the dashed line of Fig. 8(b).

V. Practical Implementation Issues

A. Power Analysis of Canonic and Non-Canonic Realizations

In order to estimate and compare the approximate analog power dissipated in the proposed SC interpolators in canonic and noncanonic forms, we employ the single-stage telescopic OTA architecture, which is often used for high-speed applications and can be well approximated by the single-pole OTA model shown in Fig. 10, as its nondominant pole can be very far from the dominant one, and thus its phase margin is normally greater than 60°. Consider the equivalent continuous-time model of an SC circuit during the charge transfer phase [e.g., in either phase 0, 1, 2, or 3 of Fig. 4(b)], as also shown in Fig. 10, where $C_{\rm in}$ and $C_{\rm load}$ are, respectively, the total capacitance of input and output SC branches connected to the OTA in this phase. Assuming 1/5 of the phase (or overall settling time $t_{\rm sett}$ to be allocated for slewing, while the remaining 4/5 for linear settling $(t_{\rm sett} = t_{\rm slew} + t_{\rm lin})$, for the worst-case estimation, the OTA must be capable to drive the equivalent total capacitive loading $C_{\rm Leq}$ to a certain output voltage step $V_{\rm ostep}$ during the slewing time interval $t_{\rm slew}$, and also be exponentially settled within 0.1% accuracy during the slewing interval $t_{\rm lin}$ (the closed-loop time constant is approximately $t_{\rm lin}/7$). Thus, the required tail bias current $I_{\rm SS}$ of the OTA can be simply estimated as

$$I_{\rm SS} = \max(I_{\rm SS\_SR}, I_{\rm SS\_lin}) \tag{17}$$

where $I_{\rm SS\_SR}$ and $I_{\rm SS\_lin}$ are the tail current required in slewing and linear settling time intervals, respectively, and can be given by

$$I_{\rm SS\_SR} = SR \cdot C_{\rm Leq} = \frac{|V_{\rm ostep}|}{t_{\rm slew}} \cdot C_{\rm Leq} \tag{18a}$$

$$I_{\rm SS\_lin} = g_m \cdot V_{\rm eff}, \text{ with } g_m = \frac{C_{\rm Leq}}{\beta \cdot (t_{\rm lin}/7)} \tag{18b}$$

in which SR and g_m are the required slew rate and transconductance, $V_{\rm eff}$ is the effective voltage $(V_{\rm GS} - V_{\rm th})$ for differential-pair MOS transistors, and the equivalent total capacitive loading

$$C_{\rm Leq} = C_{\rm load} + C_{\rm po} + \beta \cdot (C_{\rm in} + C_{\rm pi}) \tag{18c}$$

and feedback factor

$$\beta = \frac{C_F}{C_{\rm in} + C_{\rm pi} + C_F}. \tag{18d}$$

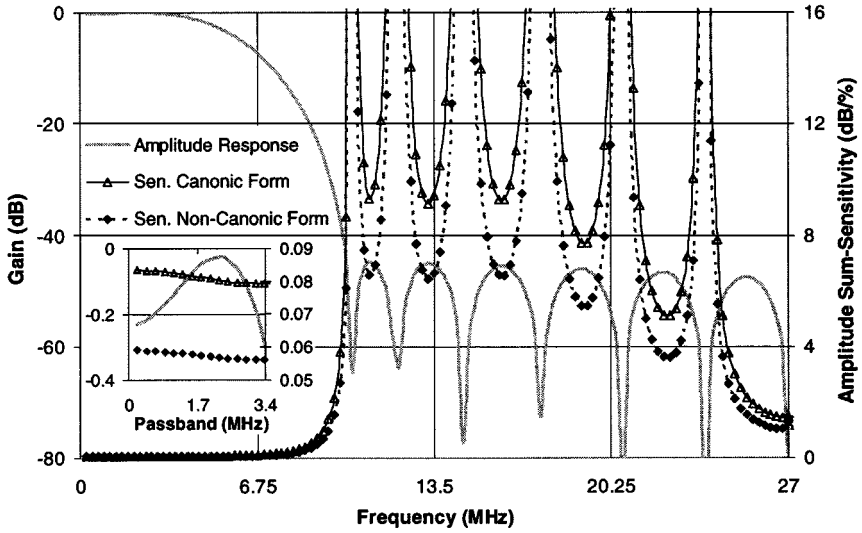
Therefore, the expected static power of the OTA is given by the product of the supply voltage $V_{\rm DD}$ and the $I_{\rm SS}$, i.e., $P_{\rm OTA} = V_{\rm DD} I_{\rm SS}$. It is worth pointing out that a final optimum solution of the tail current normally needs to be investigated according to the required specifications in terms of gain, speed, power, dynamic range, and noise, as well as with a necessary safety margin for counting the process parasitics and variations. However, the above estimation is still very useful for an initial stage of the design.

According to the above expressions, the approximate analog powers of the FIR BP interpolator in canonic and non-canonic forms introduced in Section III-B are presented in Table III(a) ($V_{\rm eff}$ is assumed as a typical 200 mV). For a more realistic approach, each circuit here uses only one fast and one slow OTA instead of several different speed OTA's. Although canonic form has more than the double of the OTA number when compared with non-canonic form, the power is still about only 66% of the latter due to the very low-speed operation of these OTA's. Thus, the canonic form is very attractive for high-frequency applications, not only from the perspective of power efficiency, but mainly from a much more relaxed design in low-speed high-performance OTA. Besides, in this example, a better power performance and design efficiency for a 25-MHz DDFS/DAC instead of the traditional 100 MHz is also achieved. This derivation is also valid for the IIR counterpart which has been illustrated in Table III(b), by the example of the video interpolator with ER transfer function in Section IV-D. As mentioned before, the faster OTA in the output multiplexer in canonic structure consumes not much power, and even less when compared to those OTA's with L times enlarged $t_{\rm sett}$ in ADB's and accumulators as in IIR LP case (it does not happen in the circuit of Section III-B due to the specifically identical voltage step of input and output signals in this frequency-translated BP operation, thus no relaxation is exhibited in SR but usually in the low-pass interpolation). And, it is obvious that OTA in multiplexer always needs less power and also smaller g_m than those in ADB's and accumulators with the same $t_{\rm sett}$ in non-canonic form.

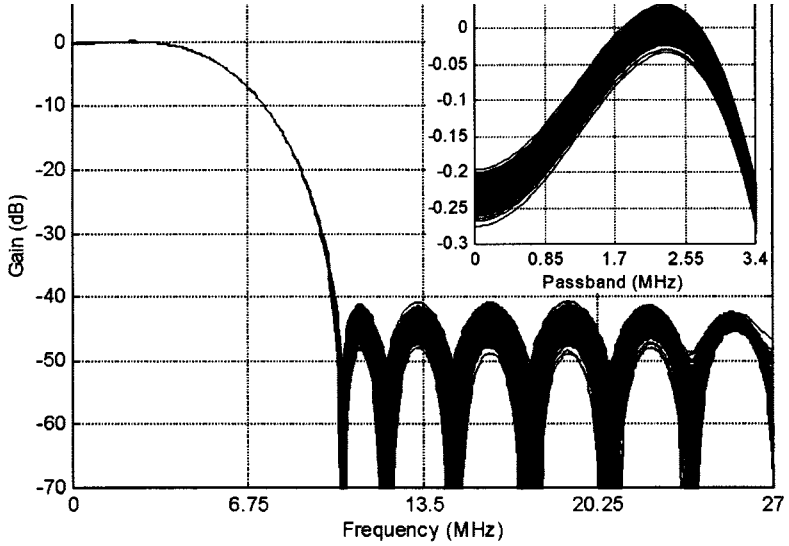
B. Sensitivity Analysis of Capacitor Ratio Mismatches

The sum-sensitivity [27] of the response with respect to all capacitors is performed to compare different designs with deviations of multiple circuit parameters.

1) FIR Structure: For a more general case, instead of the above specific multinotch narrow BP interpolator, we consider an example of an 18-tap LP fourfold interpolator, whose amplitude sum-sensitivity for the ADB polyphase structures in both canonic and noncanonic forms are performed as shown in Fig. 11(a). Canonic realization has relatively worse overall sensitivity when compared with noncanonic mainly due to the



(a)



(b)

Fig. 11. (a) Amplitude sum-sensitivity. (b) Monte Carlo simulations with respect to all capacitors of 18-tap improved SC FIR LP interpolator.

double-sampling nature. For its having only-zero property, FIR structure presents a good sensitivity in passband, but relatively poor sensitivity in stopband. For a 0.3% capacitor ratio error, which can be achieved in current technologies, maximum passband and stopband deviations are roughly 0.025 and 2.7 dB and 0.018 and 2 dB for canonic and noncanonic form, respectively, which still have a satisfactory more than −40-dB attenuation in the stopband. Since the coefficients are implemented with a direct capacitor ratio, the stopband is also predictable to have the mean about −43 dB from the estimation by the sum of original stopband ripple and the mean value of the expected magnitude deviation $\overline{h}_k\sigma_e \cdot (\sqrt{\pi N}/2)$ ($\overline{h}_k$—arithmetic mean value of all coefficients: σ_e—standard deviation of ratio error) for an N-tap FIR filter obtained by the Rayleigh distribution [25]. In addition, we derive here a further estimation of the worst-case stopband, i.e., about −41 dB, by using $h_{k\max}$ (passband normalized to 1) instead of $\overline{h}_k$ to approximate the worst-case magnitude variation. This has been verified with a good agreement by comparing to the Monte Carlo simulation shown in Fig. 11(b) with respect to all coefficients which are independent zero-mean Gaussian random variables with $\sigma_e = 0.3\%$. Thus, from the above prediction expressions and also the Monte-Carlo simulation, an SC 50-tap fourfold FIR interpolator with theoretical −45.5-dB stopband (for regular LP L-fold interpolation, $h_{k\max} \approx 1/L$) can achieve the worst-case stopband about −40 dB with capacitor ratio standard deviation $\sigma_e = 0.3\%$ (without counting other nonideal effects in SC realization). It is also expected that it will be quite difficult to achieve higher than 8-bit accuracy for high-order and high-speed SC FIR filters without a specific improvement technique.

One attractive advantage of FIR implementation is its linear phase property; therefore, the sum-sensitivity of group delay with respect to all capacitors is performed, as shown in Fig. 12. From the results, the group delay is incredibly insensitive to the capacitor ratio errors, thus SC FIR filtering is an efficient solution in terms of low costs in power and silicon consumption for video applications, which normally require linear phase with 8-bit accuracy.

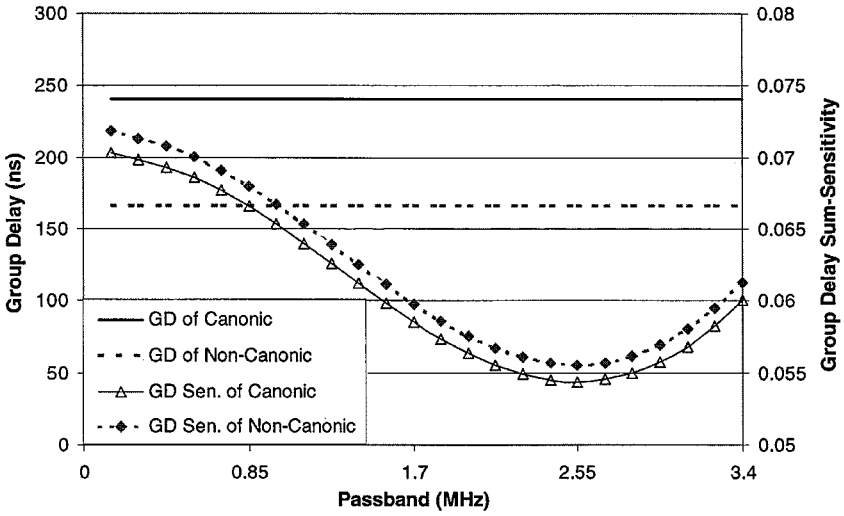
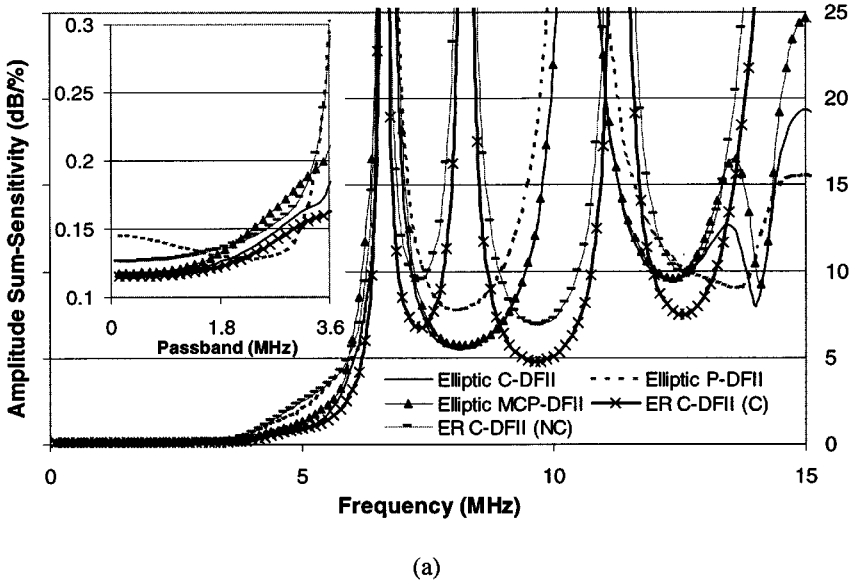
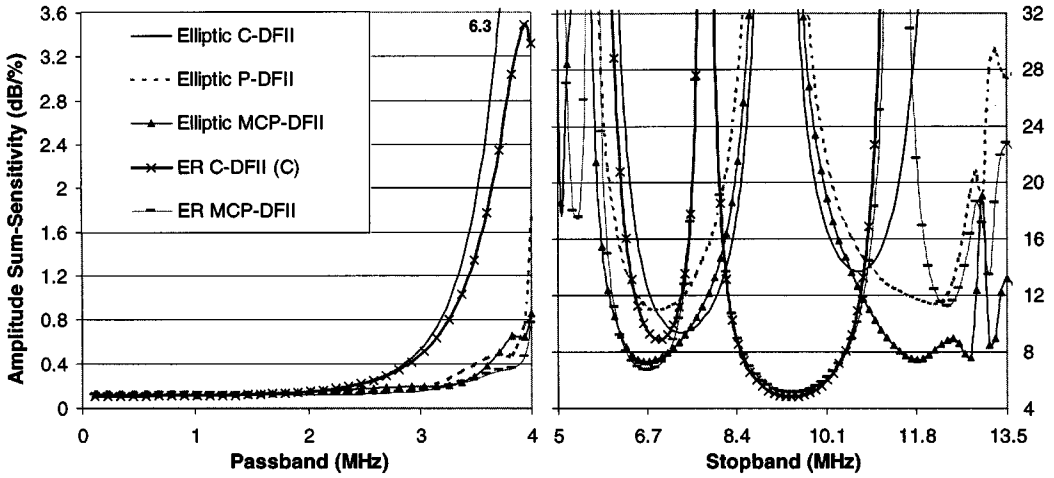


Fig. 12. Group-delay sum-sensitivity with respect to all capacitors of 18-tap improved SC FIR LP interpolator.



(a)



(b)

Fig. 13. Amplitude sum-sensitivity with respect to all capacitors for improved threefold SC IIR LP video interpolators with different architectures and with (a) fourth-order elliptic and ER ($N = 9, D = 2$) and (b) sixth-order elliptic and ER ($N = 9, D = 4$) transfer functions.

2) IIR Structure: The simulated sum-sensitivity of a fourth-order IIR video interpolator presented before with non-canonic in C-DFII, P-DFII, and MCP-DFII, as well as C-DFII with ER transfer function [C-DFII/ER; $(N = 9, D = 2)$], respectively, are presented in Fig. 13(a). As we expected, the C-DFII/ER obtains the best sensitivity in passband due to its fewer pole characteristics, and its stopband has a similar level when compared to all other realizations because of no extra zeros in the multirate form. The MCP-DFII, which remains superior to the cascade structure, is more advanced in the overall response than the P-DFII, whose performance depends on the output adder. However, these two are both worse than C-DFII in the passband, since the poles are not tightly clustered due to the relatively lower order and larger transition band; thus, the low-sensitivity advantage of cascade or parallel structures is not explicit. This can be shown in a higher sixth-order IIR interpolation filter whose simulated sensitivities are shown in Fig. 13(b). Both P-DFII and MCP-DFII are much less sensitive than C-DFII in passband, stopband, and also pole-zero cancellation, and the MCP-DFII achieves the best performance, as expected. Besides, an ER IIR interpolator $(N = 9, D = 4)$ for the same specifications is again much less sensitive when compared with the sixth-order filter both in C-DFII realization, while its MCP-DFII structure possesses a performance similar to the sixth-order one implemented also in MCP-DFII structure. This results from the fact that it still requires four poles to maintain the flatness in this relatively wide passband. However, comparing that with the general IIR transfer function $(N - 1 = D)$, ER form is still a good alternative, especially for multirate filtering, due to its reduced passband sensitivity (fewer poles) without increasing sensitivity in the stopband in most cases (similar number of zeros in multirate form), and its superiority will be very apparent for narrow passbands, i.e., $D = 2$. The small sensitivity overshoots in nearly half of the higher output sampling rates are caused by the incomplete multirate pole-zero cancellation. In addition, for the same reason as in its FIR counterpart, canonic structures are more sensitive than noncanonic. Besides, the delay factor $T_i(z)$ in MCP-DFII is important aforementioned, e.g. the sensitivity has an 18% increase if $T_2(z) = z^{-3}$ (use first-delay block output for second DFII biquad input) in this example.

For either FIR or IIR responses, very narrowband signal conversion is normally associated with a large alteration ratio, and a pure cascade or multistage realization is thus always an efficient and practical solution [28], while for the system with a small or prime alteration ratio but stringent specifications, a combination of integer and the fractional sampling-rate converters [29] is another alternative for achieving better analog circuitry performance.

C. Analysis of OTA Finite Gain and Bandwidth and dc Offset Effects

For simplicity, here we consider the threefold interpolator with ER IIR transfer function as it also contains an FIR-like multinotch stopband. The simulated results using the OTA model in Fig. 10 with a gain of 3000 and a nominal g_m (gm_nm) in Table III(b) are presented in Fig. 14(a) and (b) for, respectively, passband and stopband either keeping the nominal g_m (same speed) but reducing the gain to 500, or keeping a low gain of 500 but with extra 40% reduction in nominal g_m. Results show that passband deviation imposed by finite gain of OTA's is less important than that caused by unity-gain bandwidth of OTA's, as the former leads mainly to a net gain shift, while the latter to a relatively larger rolloff in the passband. Although these errors lead to the movement of zeros from the unit circle, affecting the stopband and also the cancellation of poles and zeros shown in Fig. 14(b), nearly half of the output sampling rate, −40-dB attenuation is still achieved. The situation of a canonic structure is also worse than noncanonic, but the low-speed and low-power requirements of the former allow to have a free headroom in design and also a decreased sensitivity to process variation.

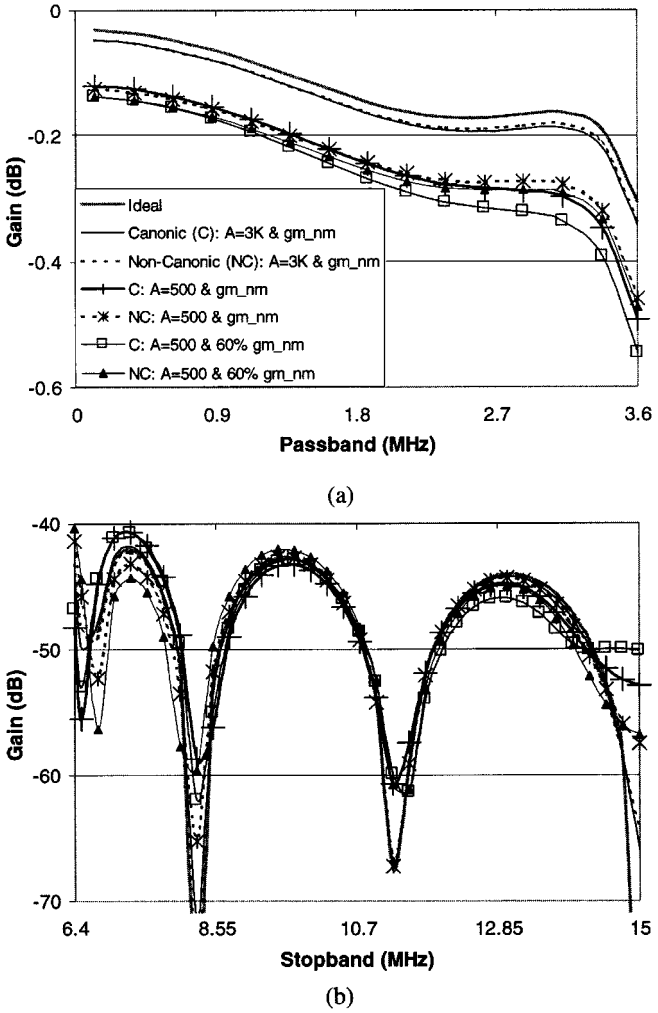


Fig. 14. OTA finite gain and bandwidth effects for improved threefold SC IIR LP interpolator with ER $(N = 9, D = 2)$ transfer function.

TABLE IV
SIMULATIONS OF FIXED-PATTERN NOISE IMPOSED BY INPUT-REFERRED DC OFFSET OF OTA'S IN IMPROVED SC FIR AND IIR INTERPOLATORS

	FIR LP Interpolator (N=18, L=4)		IIR ER LP Interpolator (N=9, D=2, L=3)	
	DC Offset	Max P. Noise	DC Offset	Max P. Noise
Non-Canonic	-26 dB	-59 dB	-22 dB	-62 dB
Canonic	-26 dB	-61 dB	-24 dB	-45 dB
IIR Canonic without Adder Sharing			-22 dB	-51 dB

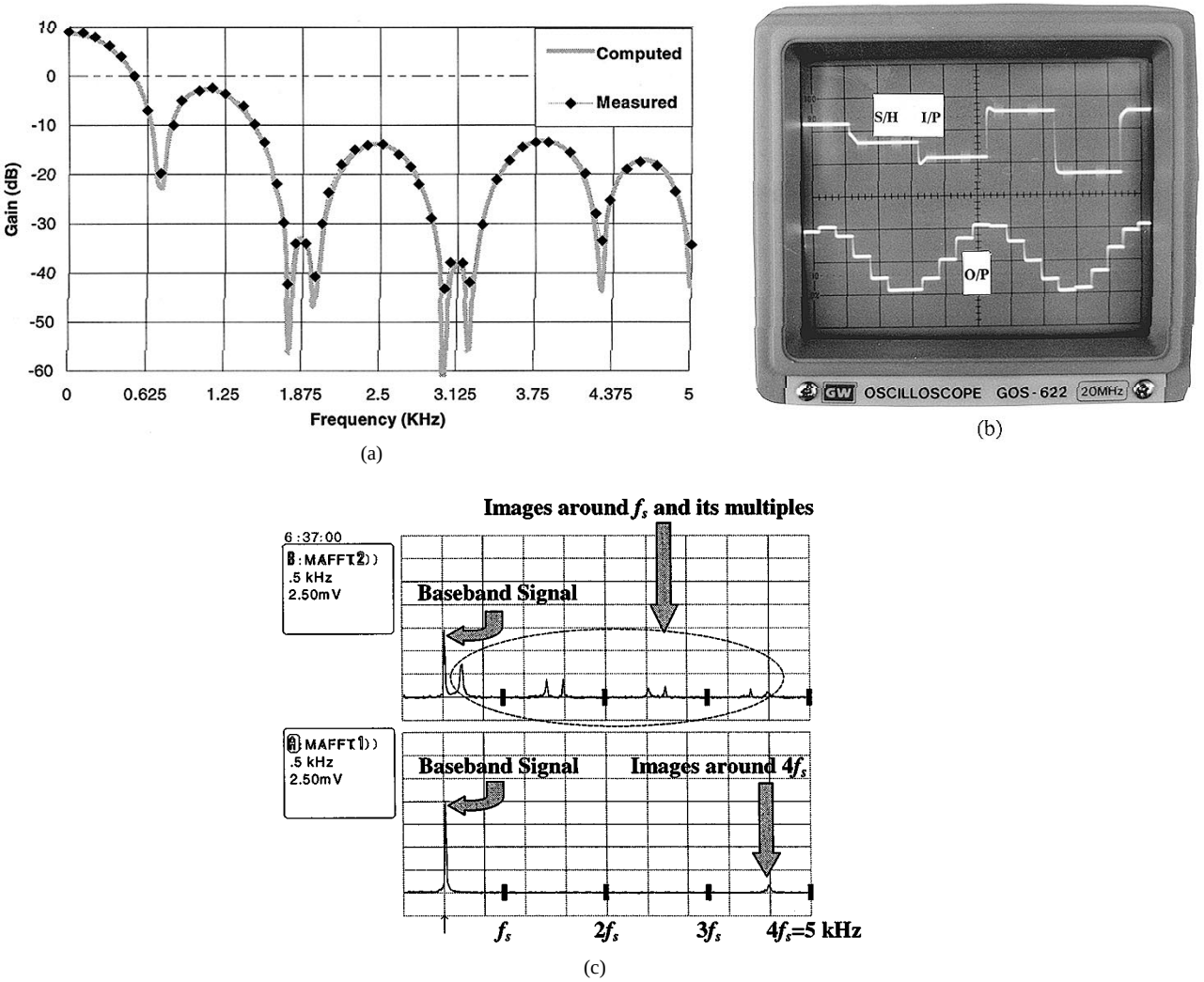
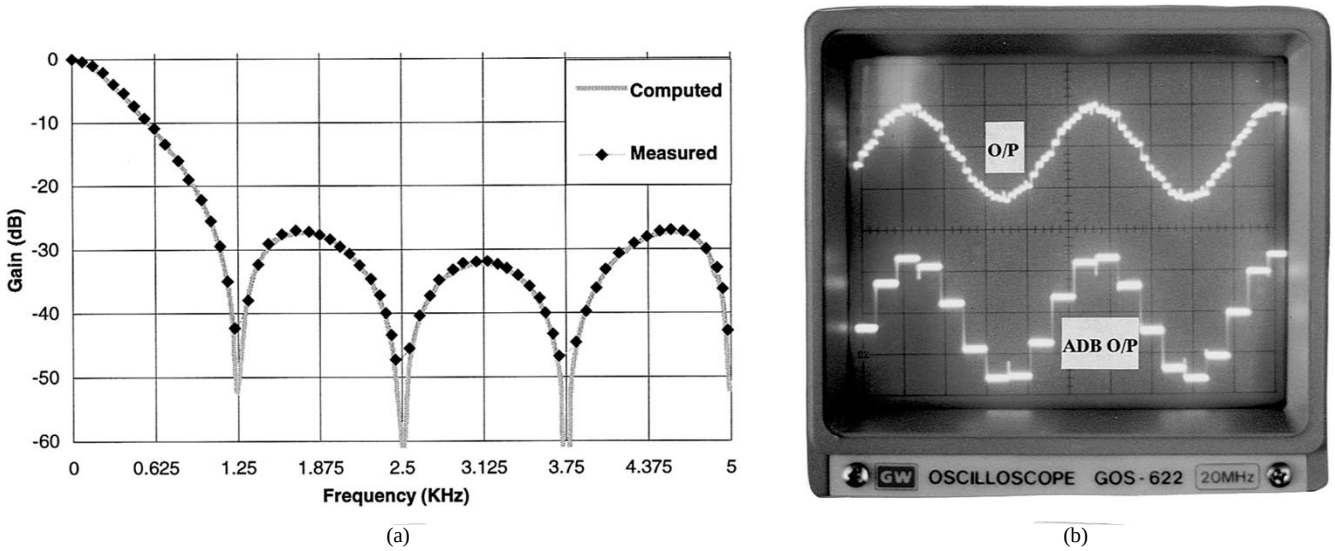


Fig. 15. Experimental results of an improved fourfold SC FIR LP interpolator. (a) Computed and measured amplitude responses. (b) Mid-frequency S/H input and measured output interpolated signals. (c) Spectrum of mid-frequency input and output signals.

Another limitation of the analog delay line is the OTA dc offset propagation and accumulation which results in a reduced signal-to-noise-ratio (SNR) by the undesired fixed-pattern noise placed at lower input sampling rate and its multiples in the interpolation. The pattern noises obtained by the FFT of the output interpolated signal with 5-mV OTA offset, which can be controlled with a proper layout in current technologies, has been summarized in Table IV for both FIR and IIR realizations. Canonic IIR realization has the poorest situation, not only because it contains more OTA's, but more importantly, a worse unbalanced offset propagation in both nonrecursive and recursive branches caused mainly by the input adder (embedding delay z^{-3}) and its sharing in the coefficient simplification procedure aforementioned. Simulation shows that a 6-dB improvement can be achieved by employing an SC adder for summing input and recursive signals before the delay line, although one extra OTA is required. In noncanonic IIR, the adder (z^{-1}) affects only coefficients related to A0, thus mainly rendering a relatively larger dc offset to output signal and having similar performance as in the FIR case. For a further reduction in such undesired noise, offset- and gain-compensation by correlated-double sampling techniques can be employed [30].

VI. Experimental Results

The proposed DF and ADB polyphase, as well as the R-ADB polyphase structures for FIR and IIR improved SC interpolation, have been verified by the realization of discrete-component models employing CMOS 4066 analog switches, BiCMOS 3140 OA's and a unit capacitance value of 1 nF. First, we implemented fourfold SC FIR LP interpolator [2] for a narrow SC BP system, which operates with an output sampling rate of 5 kHz due to constraints of the available discrete components. The measured amplitude response shown in Fig. 15(a) matches well with the computed response. The measured time-domain input and output signals at mid-frequency, together with their associated spectral characteristics are shown respectively in Fig. 15(b) and (c). Although there is about a 3-dB loss for the input baseband signal due to the S/H effect at the lower input rate, the improved interpolator provides a perfectly interpolated sinusoidal output sampled at the higher rate by rejecting the unwanted images around f_s and its multiples. More importantly, the baseband signal has been recovered with only little loss imposed by the sole S/H shaping at higher output sampling rate.



(a) (b)

Fig. 16. Experimental results of an improved threefold SC IIR LP interpolator. (a) Computed and measured amplitude responses. (b) First ADB output and interpolated output signals ($f_{\text{in}} = 150$ Hz).

To verify the effectiveness of R-ADB polyphase structure, a first-order fourfold IIR LP interpolator is implemented also with a 5-kHz output sampling rate. Its simulated and measured responses are illustrated in Fig. 16(a). Fig. 16(b) shows the output of the first ADB, which processes the input and recursive signals efficiently at lower input sampling rate, and the final interpolated output. The slightly imperfect output sinusoidal waveform is caused by the insufficient suppression (about 30 dB) of the frequency-translated image components due to the first-order IIR function nature.

VII. Conclusion

A novel sampling technique based on multirate polyphase structures has been proposed for precise sampled-data analog interpolation whereby the input S/H shaping distortion is eliminated, and thus achieving an operation similar to digital interpolation. Several low sensitive SC architectures, with both FIR and IIR filtering responses, have been proposed for such improved analog interpolation. Canonic-ADB-based structures specialized for high-speed applications demand OTA's with a very relaxed settling time compatible with the full larger input sampling period, while noncanonic-ADB-based structures consume fewer analog component count with a reduced sensitivity at the expense of requiring a relatively shrunken OTA settling time compatible with a full-output sampling period. Practical implementation issues have also been addressed in terms of the analysis of power dissipation, sensitivity to the effects of realistic capacitance ratio mismatches, and OTA finite gain and bandwidth, as well as offset voltage. Both computer simulated and experimental results have been presented for demonstrating the correctness of operation of the proposed improved SC interpolators.

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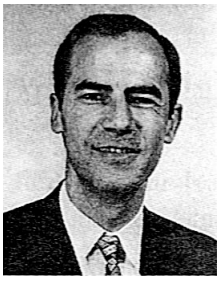

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