IIR Switched-Capacitor Decimator Building Blocks with Optimum Implementation

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Abstract —The concepts of multirate sampled-data signal processing play an important role in the area of multirate switched-capacitor (SC) systems, i.e. systems that operate with more than one sampling rate. In such systems, the purpose of SC decimator building blocks is to reduce the sampling rate of a sampled-data signal from a high value MF_s to a lower value F_s. This paper is concerned with the design of SC decimators whose transfer functions have infinite impulse response (IIR). New optimum architectures are developed such that the speed requirements of the amplifiers are determined by the lower sampling rate F_s, thus rendering the circuits particularly attractive for high-frequency applications. Appropriate Z-transfer functions are derived for first- and second-order IIR SC decimator building blocks. Design examples of optimum IIR SC decimators with different types of frequency response, as well as different factors M of sampling rate reduction, are presented to demonstrate their practical feasibility.

I. INTRODUCTION

SWITCHED-CAPACITOR (SC) signal processing has been traditionally looked at from the point of view of continuous-time models, i.e., models that approximate the behavior of continuous-time circuits, and has used with success the vast amount of theoretical background available for classical continuous-time processing, especially filtering. This, together with the rapid developments of MOS technology, explains the progress of SC signal processing over the past 8 years [1]–[3]. However, we see today that some of the disadvantages attributed to SC circuits, namely, the phenomena of aliasing and imaging, result from their own sampled-data nature and are associated with the inherent spectral properties of discrete-time signals.

In recent work, we have started developing an alternative philosophy for SC signal processing based on the framework of multirate sampled-data signal processing [4] and where, unlike in traditional continuous-time models, we take full advantage of the discrete-time spectra resulting from the operation of SC circuits. Multirate SC systems have been successfully employed for the realization of different signal processing applications, namely filtering with very narrow relative bandwidth and also for the
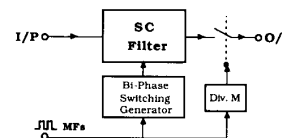
Fig. 1. Non-optimum implementation of IIR SC decimators.

generation and detection of single sideband signals [5]–[8]. Multirate SC systems are particularly important for the implementation of interface systems between continuous-time and sampled-data signals, both analog and digital [9]–[11].

In multirate SC systems, the reduction of the sampling rate of a sampled-data signal from a high value MF_s to a lower value F_s is accomplished by means of an SC decimator which should provide an appropriate amplitude response for filtering the aliasing spectrum associated with the signal sampled at the lower rate F_s. To implement such filtering function we can employ either finite impulse response (FIR) or infinite impulse response (IIR) transfer functions, depending on the particular application and the required anti-aliasing specifications [12]. FIR SC decimators are suitable for multinotch stopband and linear phase response characteristics, and are most efficiently implemented using non-recursive polyphase structures [13]. This paper is concerned with the design of IIR SC decimators, which are more adequate for applications with high selectivity and wide stopband approximations.

IIR SC decimators are currently implemented based on *non-optimum* and *sub-optimum* classes of circuits, according to the resulting speed requirements of the operational amplifiers (OA's). The non-optimum class of IIR SC decimator circuits, schematically illustrated in Fig. 1, consists of an SC filter operating at MF_s and whose output signal is sampled at the lower rate F_s. Although this offers a straightforward solution for the realisation of high selectivity amplitude responses using simple bi-phase SC filters designed by classical methods, it does not take advantage of the sampling rate reduction inherent to the decimation process. Hence, the resulting speed of the OA's and capacitance spread are both determined by the higher input sampling rate MF_s. Furthermore, classical IIR SC filter designs are not sufficiently flexible to realise Z-transfer functions having a numerator polynomial function with higher order than the corresponding denominator polyno-
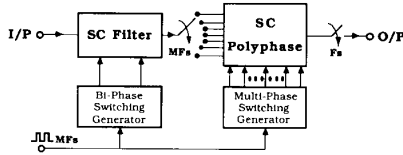
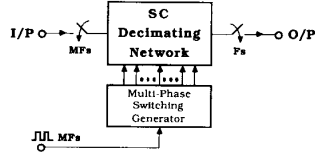Fig. 2.   Sub-optimum implementation of IIR SC decimators.

Fig. 3.   Optimum implementation of IIR SC decimators.

(a)

(b)

Fig. 4.   Example of an optimum first-order SC decimator with $M = 4$.
(a) Circuit. (b) Time frames.

mial function, as required for high selectivity multinotch amplitude responses [12]. Fig. 2 represents the sub-optimum class of IIR SC decimator circuits consisting of the cascading of an SC filter operating at MF_s and a non-recursive polyphase structure with a decimating factor of M [14]. This architecture gives greater design flexibility than the above non-optimum class of IIR SC decimators, and also allows slower OA's in the polyphase structure with output sampling rate F_s. However, faster OA's are still needed in the SC filter operating at the higher sampling rate MF_s.

To overcome the speed limitations of the above architectures a new optimum class has been introduced for the implementation of IIR SC decimators where the speed of the OA's is determined by the lower output sampling rate F_s [15]. This paper proposes a systematic methodology for the design of optimum first- and second-order IIR SC decimator building blocks, respectively, in Sections II and III, with arbitrary numerator polynomial functions and integer decimating factors up to $M = 10$. Practical design examples and experimental results are illustrated in Section IV. In Section V we briefly discuss some sensitivity aspects related to the amplitude response of the optimum class of IIR SC decimator circuits.
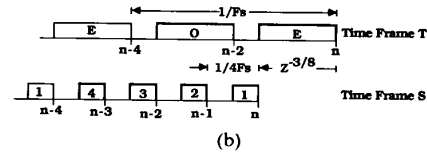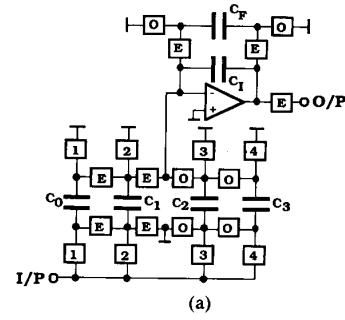
II. First-Order SC Decimator Building Block

A. General Z-Transfer Function

An optimum IIR SC decimator with a sampling rate reduction factor of M, schematically illustrated in Fig. 3, consists of a single network whose input sampling rate is MF_s and whose output sampling rate is F_s. The amplitude response of such network is designed to meet the desired passband specifications, and, at the same time, achieve the required rejection of the unwanted alias signal components associated with the signal sampled at F_s. The original Z-transfer function of a first-order decimator

$$H(Z) = \frac{\sum_{j=0}^{N} a_j \cdot Z^{-j}}{b_0 - Z^{-1}} \qquad (1)$$

can have an arbitrary order N of the numerator polyno-

mial function. The unit delay period is relative to $1/MF_s$ corresponding to the sampling period at the input of the decimator. By using the equivalence [4]:

$$b_0 - Z^{-1} = \frac{b_0^M - Z^{-M}}{\sum_{I=0}^{M-1} b_0^{M-I} \cdot Z^{-I}} \qquad (2)$$

the above Z-transfer function can also be expressed as

$$\overline{H}(Z) = \frac{\sum_{m=0}^{N+M-1} \bar{a}_m \cdot Z^{-m}}{b_0^M - Z^{-M}} \qquad (3)$$

with the following numerator coefficients:

$$\sum_{m=0}^{N+M-1} \bar{a}_m \cdot Z^{-m} = \sum_{j=0}^{N} a_j \cdot Z^{-j} \sum_{I=0}^{M-1} b_0^{M-I} \cdot Z^{-I}. \qquad (4)$$

For consistency, we still represent the delay terms in (3) referring to a unit delay period of $1/MF_s$. Hence, the denominator terms proportional to Z^{-iM} can now be implemented by a recursive structure operating at the lower sampling rate F_s. This is illustrated next for a simple example of a first-order SC low-pass decimator with a decimating factor of $M = 4$.

B. SC Implementation

The optimum implementation of a first-order SC decimator described by the Z-transfer function

$$H(Z) = \frac{\bar{a}_0 + \bar{a}_1 \cdot Z^{-1} + \bar{a}_2 \cdot Z^{-2} + \bar{a}_3 \cdot Z^{-3}}{\bar{b}_0 - Z^{-4}} \qquad (5)$$

is illustrated in Fig. 4(a). The OA with integrating capacitor C_I and feedback SC branch C_F is viewed as a first-order charge-to-voltage converter, while the input SC branches C_i ($i = 0$ to 3) are viewed as voltage-to-charge converters and are organized as in a polyphase structure [13]. The
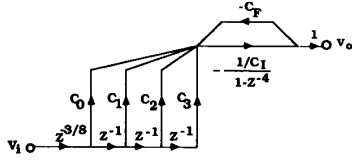
Fig. 5. Signal flow graph representing the operation of the SC decimator in Fig. 4.

operation of this SC decimator refers to the time frames given in Fig. 4(b). In the figure, time frame T, for charge transfer, has 2 wide time slots like in a conventional SC integrator operating at F_S, which determines the operation of the switches controlling the flow of charge through the virtual ground of the amplifier. On the other hand, the 4 time slots in time frame S, for signal sampling, control the switching operation of the switches which are responsible for the sampling of the input signal. The width of such time slots is simply limited by the equivalent RC time constants associated with the charging of each one of the input SC's, and thus can be substantially narrower than the time slots in time frame T. Time slot 1, in frame S, occurs immediately before time slot E in time frame T. Hence, by referring to the time reference given in Fig. 4(b), we have an unimportant flat delay factor of $Z^{-3/8}$ between the output sampling instant (at the end of time slot E) and the most recent sampling instant of the input signal (at the end of time slot 1).

The operation of the SC decimator in Fig. 4 can be conveniently represented by the signal flow graph (SFG) diagram of Fig. 5. The transmission factor $Z^{-3/8}$ represents, as mentioned above, the flat delay between time frame S and time frame T, whereas the transmission factors $C_i \cdot Z^{-i}$ result from the operation of the input toggle switched-inverter (TSI) branches acting as voltage-to-charge converters. The coefficients C_i correspond to the capacitance value of each SC branch, while the delay terms Z^{-i} represent the *instant of signal sampling at the end of the time slot controlling the respective input switch*. Following the input branches, we have a branch with transmission factor $(1/C_I)/(1 - Z^{-4})$ representing the periodic charge-to-voltage conversion between two consecutive output sampling instants at the end of time frame E, and which is carried-out by the OA with integrating capacitor C_I. Finally, the feedback branch with transmission factor $- C_F$ describes the voltage-to-charge conversion of the feedback SC branch in Fig. 4(a). From this SFG diagram, and using the feedback equation [16], we arrive at the Z-transfer function:

$$T(Z) = Z^{-3/8} \cdot \frac{C_0 + C_1 \cdot Z^{-1} + C_2 \cdot Z^{-2} + C_3 \cdot Z^{-3}}{(C_I + C_F) - C_I \cdot Z^{-4}} \quad (6)$$

for the first-order SC decimator of Fig. 4.

In the above SC decimator building block, the proposed switching of the SC branches is devised such that the sampling of the input signal is performed during a short time interval, whereas the transfer of charge is performed
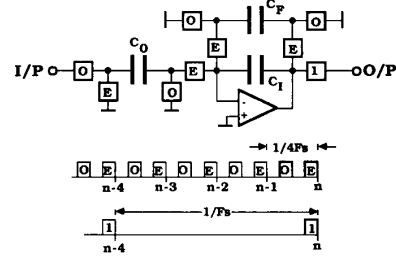

Fig. 6. Non-optimum implementation of a first-order SC decimator with $M = 4$.

during a much wider time interval to maximize the time allowed for amplifier settling. In comparison with the non-optimum implementation of this SC decimator, shown in Fig. 6 for clarity, the SC decimator building block of Fig. 4 employs a larger number of SC branches and switching waveforms. However, we can now obtain a significant M-fold increase ($M = 4$ in this example) of the time allowed for amplifier settling. In other words, for the same settling time of the OA, the proposed circuit is capable of achieving an M-fold increase of the input sampling rate compared with the traditional non-optimum implementation. Next, we shall extend this technique to the design of second-order SC decimator building blocks.

III. SECOND-ORDER SC DECIMATOR BUILDING BLOCK

A. General Z-Transfer Function

The original Z-transfer function of a second-order decimator, with arbitrary numerator polynomial function, is described by

$$H(Z) = \frac{\sum\limits_{j=0}^{N} a_j \cdot Z^{-j}}{1 - 2r_p \cdot \cos(\theta_p) \cdot Z^{-1} + r_p^2 \cdot Z^{-2}}. \quad (7)$$

The type of equivalence given in (2) can also be applied to the above Z-transfer function [4]. After some simple algebraic manipulations, this leads to

$$\overline{H}(Z) = \frac{\sum\limits_{j=0}^{N} a_j \cdot Z^{-j} \sum\limits_{l=0}^{2(M-1)} \alpha_l \cdot r_p^l \cdot Z^{-l}}{1 - 2r_p^M \cdot \cos(M\theta_p) \cdot Z^{-M} + r_p^{2M} \cdot Z^{-2M}} \quad (8)$$

where the coefficients α_l in the numerator function are given in Table I for practical decimating factors up to $M = 10$.

B. SC Implementation

The SC decimator building block implementing the Z-transfer function (8) is described in Fig. 7. The SC network of Fig. 7(a) employs a basic two integrator loop (TIL) structure which is responsible for the realization of the denominator function. Capacitor E (capacitive damping), and switched capacitor F (resistive damping), represent two alternative forms of damping that can be used in the
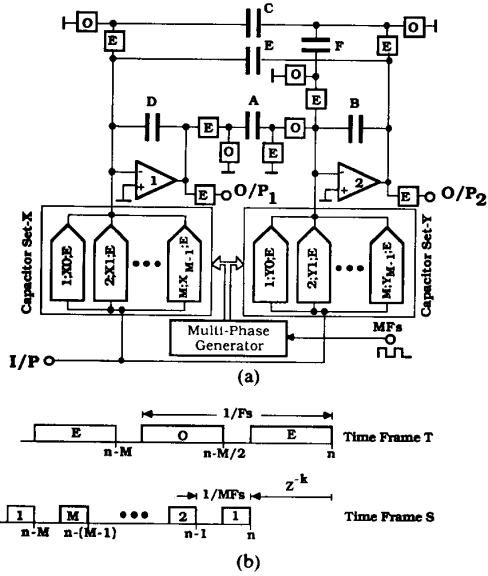
Fig. 7. Optimum implementation of second-order SC decimator. (a) General structure. (b) Time frames.

loop [12], [17]. In a similar fashion as before, this TIL structure is viewed as a second-order charge-to-voltage converter whose input packets of charge are produced by the two sets of SC branches, set X and set Y, respectively, connected to the virtual ground of OA1 and OA2. These SC branches, organized in the form of polyphase structures, are represented by polygonal symbols where we indicate the time slot for input signal sampling, the time slot for output signal sampling, and the capacitive value of the branch as well as the polarity of charge transfer. For greater design flexibility we shall always use different input and output time slots. Parasitic-compensated toggle
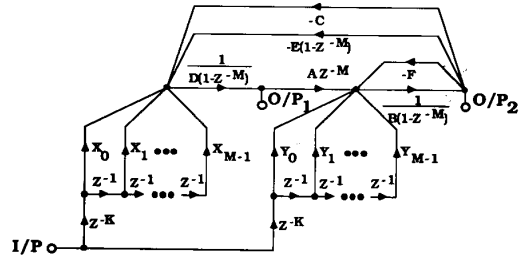

Fig. 8. Signal flow graph representing the operation of the SC decimator in Fig. 7.

instants at the end of the respective input time slot *relative to the sampling instant at the output of the amplifier to which they are connected*. The term Z^{-k} represents a flat delay between the first instant of input signal sampling at the end of time slot 1, in time frame S, relative to the output sampling instant at the end of time slot E, in time frame T.

The SFG diagram of Fig. 8 represents the operation of the SC decimator building block in Fig. 7. The interpretation of this SFG closely follows the interpretation given before for the first-order SC decimator with optimum implementation. However, we should notice here that the transmission factor $[-E(1-Z^{-M})]$ emulates the memory-type behavior of the unswitched-capacitor E, i.e., corresponding to the packet of charge produced by the variation of the output voltage of OA2 between two consecutive sampling instants at the output of OA1. The output signals of the SC decimator in Fig. 7(a), sampled in time slot E, can be available either from terminal 1, corresponding to the output of OA1, or from terminal 2, corresponding to the output of OA2. By applying the feedback equation to the corresponding SFG diagram of Fig. 8, the resulting overall Z-transfer functions are then given by

$$T_1(Z) = \frac{[(B+F)\cdot X(Z)-(C+E)\cdot Y(Z)]+[E\cdot Y(Z)-B\cdot X(Z)]\cdot Z^{-M}}{(B\cdot D+D\cdot F)+(A\cdot C+A\cdot E-D\cdot F-2B\cdot D)\cdot Z^{-M}+(B\cdot D-A\cdot E)\cdot Z^{-2M}}\cdot Z^{-k} \qquad (9\text{-}a)$$

for terminal 1, and by

$$T_2(Z) = \frac{D\cdot Y(Z)+[A\cdot X(Z)-D\cdot Y(Z)]\cdot Z^{-M}}{(B\cdot D+D\cdot F)+(A\cdot C+A\cdot E-D\cdot F-2B\cdot D)\cdot Z^{-M}+(B\cdot D-A\cdot E)\cdot Z^{-2M}}\cdot Z^{-k} \qquad (9\text{-}b)$$

switched capacitor (PCTSC) branches are utilized for negative charge transfers, whereas TSI branches are employed for positive charge transfers. The time frames controlling the operation of the SC network, in Fig. 7(b), are designed to maximize the time allowed for amplifier settling. Two wide time slots, in the charge transfer time frame T, control the flow of charge through the virtual ground of the amplifiers. The sampling of the input signal is controlled by the sampling time frame S with M much narrower time slots that do not affect the speed requirements of the amplifiers. The delay terms associated with each input SC branch are determined by the sampling

for terminal 2. For conciseness, we have represented by

$$X(Z) = \sum_{u=0}^{M-1} X_u\cdot Z^{-u} \qquad (10\text{-}a)$$

the voltage-to-charge conversion function associated with set X of input SC branches, and by

$$Y(Z) = \sum_{v=0}^{M-1} Y_v\cdot Z^{-v} \qquad (10\text{-}b)$$

the corresponding function associated with set Y of input SC branches.

TABLE I
EXPRESSIONS GIVING THE COEFFICIENTS α_1 IN THE TRANSFORMATION FUNCTION FOR OPTIMUM
SECOND-ORDER DECIMATORS

M	2	3	4	5	6	7	8	9	10
$\alpha 1$	$2x$	$2x$	$2x$	$2x$	$2x$	$2x$	$2x$	$2x$	$2x$
$\alpha 2$		$4x^2-1$	$4x^2-1$	$4x^2-1$	$4x^2-1$	$4x^2-1$	$4x^2-1$	$4x^2-1$	$4x^2-1$
$\alpha 3$			$8x^3-4x$	$8x^3-4x$	$8x^3-4x$	$8x^3-4x$	$8x^3-4x$	$8x^3-4x$	$8x^3-4x$
$\alpha 4$				$16x^4-12x^2+1$	$16x^4-12x^2+1$	$16x^4-12x^2+1$	$16x^4-12x^2+1$	$16x^4-12x^2+1$	$16x^4-12x^2+1$
$\alpha 5$					$32x^5-32x^3+6x$				
$\alpha 6$	$F(z)=\sum\limits_{i=0}^{2(M-1)}\alpha_i(r_p)^i z^{-1}$						$64x^6-80x^4+24x^2-1$		
$\alpha 7$							$128x^7-192x^5+80x^3-8x$		
$\alpha 8$	$\alpha_0=1, \quad \alpha_{[2(M-1)-1]}=\alpha_1, \quad x=\cos(\theta_p)$							$256x^8-448x^6+240x^4-40x^2+1$	
$\alpha 9$									$512x^9-1024x^7+448x^5-192x^3+10x$

For each one of the above Z-transfer functions (9) of the SC decimator building block, the coefficients of Z-transfer function (8) are determined as functions of the input SC's X_u and Y_v, respectively, in capacitor set X and capacitor set Y, as well as the capacitors in the loop of the decimator. The adoption of a particular topology, including the selection of the output terminal and type of damping, as well as the design of capacitor sets X and Y, is carried out on a case-by-case basis to minimize the capacitance spread and total overall capacitor area and also to obtain reduced sensitivity of the amplitude response with respect to capacitance ratio errors. Designing for maximum dynamic range is achieved by using the conventional technique of scaling the voltages at the output of the OA's [17].

In the above SC decimator structure we have considered each capacitor set with M input SC branches such that the maximum delay between the first and the last input sampling instants is always less than one period $1/F_s$. However, there are practical applications of optimum SC decimators where it might be necessary for the input SC branches to realize longer delay terms, as is the case where the order of the numerator polynomial function is higher than the corresponding denominator polynomial function. As we shall see next for a practical design example such applications require more than M input SC branches in each capacitor set, although we still use the same number of M input time slots determining the decimating factor.

IV. DESIGN EXAMPLES AND EXPERIMENTAL RESULTS

A. SC Bandpass-Notch Decimator with M = 2

The purpose of the first design example given here is twofold. Firstly, it illustrates the detailed step-by-step design procedure of the proposed SC decimator building blocks, and, secondly, shows its flexibility for realizing arbitrary numerator functions. This SC decimator is part of a high selectivity multistage SC bandpass decimator for a voiceband analog interface system [11], where it reduces the sampling rate from $2F_s = 19.2$ kHz to $F_s = 9.6$ kHz. By using a computer-aided filter synthesis procedure [18] we obtained the following original Z-transfer function:

$$H(Z) = \frac{(1-Z^{-1})\cdot(1-0.344887Z^{-1}+Z^{-2})}{1-1.213774Z^{-1}+0.624551Z^{-2}} \quad (11)$$

corresponding to a bandpass-notch amplitude response with notch frequency at 4.277 kHz, and a complex-conjugate pole-pair at 2.241 kHz with Q-factor of 1.525. The modified Z-transfer function for optimum implementation is given by

$$\bar{H}(Z) = \frac{\bar{N}(Z)}{\bar{D}(Z)}$$

$$= \frac{\bar{a}_0 + \bar{a}_1\cdot Z^{-1} + \bar{a}_2\cdot Z^{-2} + \bar{a}_3\cdot Z^{-3} + \bar{a}_4\cdot Z^{-4} + \bar{a}_5\cdot Z^{-5}}{1 + \bar{b}_1\cdot Z^{-2} + \bar{b}_2\cdot Z^{-4}}$$

$$(12)$$

where the modified denominator coefficients:

$$\bar{b}_1 = -0.224145 \qquad \bar{b}_2 = 0.390064$$

and the modified numerator coefficients:

$$\bar{a}_0 = 1 \qquad \bar{a}_1 = -0.131113 \qquad \bar{a}_2 = 0.337049$$
$$\bar{a}_3 = -0.207562 \qquad \bar{a}_4 = -0.373823 \qquad \bar{a}_5 = -0.624551$$

are obtained following the procedure outlined in the previous section.

The design solution we have developed for this second-order IIR SC decimator employs the Z-transfer function $T_1(Z)$ with capacitive-damping ($F = 0$). The resulting circuit is shown in Fig. 9(a) and operates with the time frames given in Fig. 9(b). The design equations for the capacitors A, B, C, D, and E in the loop of the decimator are derived from the denominator functions in (12) and (9-a) (with $M = 2$). Initially, by considering $B = D = 1$, the equations

$$\bar{b}_1 = A\cdot C + A\cdot E - 2$$
$$\bar{b}_2 = 1 - A\cdot E \quad (13\text{-a})$$

lead to

$$A = C = \sqrt{\bar{b}_1 + \bar{b}_2 + 1}$$

$$E = \frac{1 - \bar{b}_2}{\sqrt{\bar{b}_1 + \bar{b}_2 + 1}}. \quad (13\text{-b})$$

In the final design stage, the capacitance values of A, B, C, D, and E are adjusted for maximum dynamic range.

In the above SC decimator circuit, the input SC branches corresponding to capacitors X_2, Y_2, and X_3, Y_3, realize the
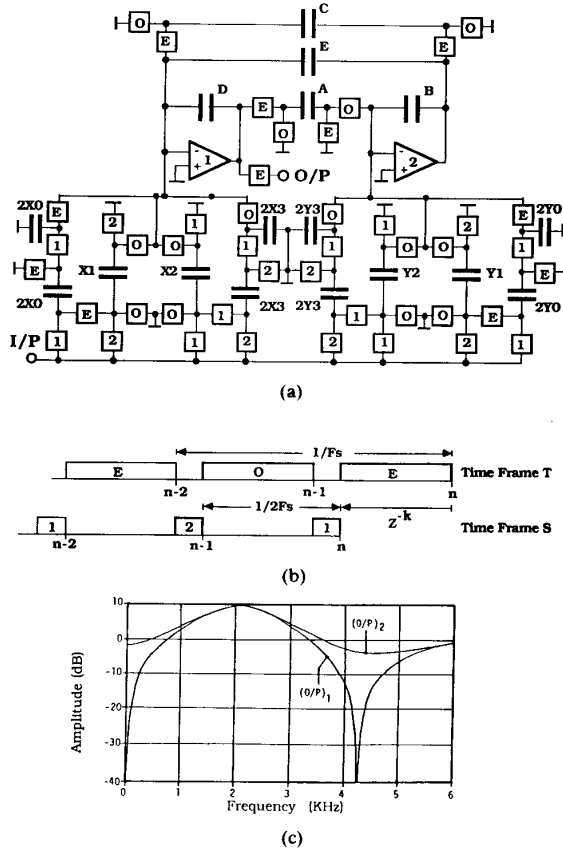
(a)

(b)

(c)

Fig. 9.   SC bandpass-notch decimator with $M = 2$. (a) Circuit. (b) Time frames. (c) Response.

terms corresponding, respectively, to delays Z^{-2} and Z^{-3}. For capacitors X_2 and Y_2 we employ simple TSI branches, whereas for capacitors X_3 and Y_3 we have to utilize their parasitic-compensated version [19]. PCTSC branches are employed for capacitors X_0 and Y_0 to implement negative transmission factors. The voltage-to-charge conversion functions associated with the input SC branches can then be expressed as

$$X(Z) = -X_0 + X_1 \cdot Z^{-1} + X_2 \cdot Z^{-2} + X_3 \cdot Z^{-3} \quad \text{(14-a)}$$

for capacitor set X, while for capacitor set Y we have

$$Y(Z) = -Y_0 + Y_1 \cdot Z^{-1} + Y_2 \cdot Z^{-2} + Y_3 \cdot Z^{-3}. \quad \text{(14-b)}$$

To derive the design equations for these capacitors we first consider for the modified numerator function in (12) the following alternative expression:

$$\bar{N}(Z) = \bar{a}_0 + \bar{a}_1 \cdot Z^{-1} + \bar{a}_{21} \cdot Z^{-2} + \bar{a}_{31} \cdot Z^{-3}$$

$$+ \left(\bar{a}_{22} + \bar{a}_{32} \cdot Z^{-1} + \bar{a}_4 \cdot Z^{-2} + \bar{a}_5 \cdot Z^{-3} \right) \cdot Z^{-2}. \quad \text{(15)}$$

Then, after replacing (14) into (9-a) (with $M = 2$), equating the resulting expression to (15) and performing some simple algebraic manipulations, we arrive at the following set

of design equations:

$$Y_0 = \left[\left(\bar{a}_0 + \bar{a}_{22} \right) / C \right] \qquad X_0 = E \cdot Y_0 + a_{22}$$

$$Y_1 = -\left[\left(\bar{a}_1 + \bar{a}_{32} \right) / C \right] \qquad X_1 = E \cdot Y_1 - \bar{a}_{32}$$

$$Y_2 = -\left[\left(\bar{a}_{21} + \bar{a}_4 \right) / C \right] \qquad X_2 = E \cdot Y_2 - \bar{a}_4$$

$$Y_3 = -\left[\left(\bar{a}_{31} + \bar{a}_5 \right) / C \right] \qquad X_3 = E \cdot Y_3 - \bar{a}_5 \quad \text{(16)}$$

where coefficients a_{21}, a_{22}, a_{31}, and a_{32} can be adequately chosen to control the resulting capacitance spread in the circuit. In this design, a satisfactory solution is obtained for $a_{21} = a_{22} = a_2/2$, $a_{31} = 0$, and $a_{32} = a_3$. After scaling for maximum dynamic range, we obtain the normalized capacitance values given below:

$$X_0 = 2.0269 \qquad Y_0 = 5.692$$
$$X_1 = 1 \qquad Y_1 = 1.6497$$
$$X_2 = 1.2508 \qquad Y_2 = 1$$
$$X_3 = 2.47255 \qquad Y_3 = 3.04215$$
$$C = 3.2422 \qquad A = 6.0368$$
$$D = 2.7629 \qquad B = 6.0760$$
$$E = 1.6962$$

showing a maximum capacitance spread of 11.38 and a total area of 77.65 capacitor units for the complete circuit (notice the capacitor area required for the parasitic-compensated type of SC branches). Fig. 9(c) illustrates the computer simulated amplitude response of this SC band-pass-notch decimator.

B. SC Low-Pass Decimator with $M = 4$

The second design example corresponds to the optimum implementation of a second order low-pass decimator, with Chebyshev approximation and maximum ripple of 0.05 dB in the passband with cutoff frequency of 6 kHz. The SC decimator reduces the sampling rate from $4F_s = 1$ MHz at the input to $F_s = 250$ kHz at the output, giving a minimum rejection of 50 dB of the alias signal components associated with the lower sampling rate F_s, i.e., in the frequency band from F_s ranging from -6 to $+6$ kHz, and their corresponding repetitions around $2F_s$ and $3F_s$. To meet these specifications we investigated four alternative design solutions for the SC decimator circuit shown in Fig. 10(a) and which operates with time frames of Fig. 10(b). Such solutions correspond to the implementation of Z-transfer functions (9-a), for output terminal from OA1, and (9-b), for output terminal from OA2, both of which can have either resistive-damping ($E = 0$) or capacitive-damping ($F = 0$). After scaling for maximum dynamic range these solutions led to the normalized capacitance values indicated in Table II. Solution 1 is clearly the most economical one both in terms of capacitance spread (19.7) and total capacitor area (68.3). Hence, for further practical evaluation, we built the corresponding discrete component model using CMOS 4016 analog switches, CA 3140 OA's, and HCMOS logic circuits for the switching circuitry.

The nominal passband and overall computer-simulated impulse sampled baseband amplitude responses are shown, respectively, in Fig. 11(a) and (b). Overall, the measured frequency-translated amplitude response of the SC deci-
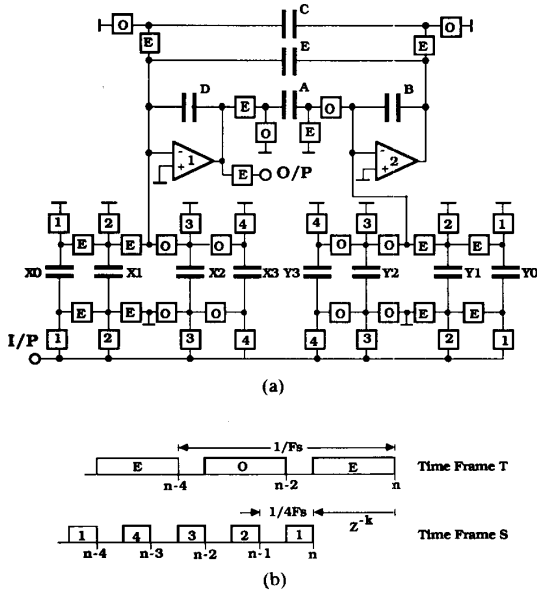
Fig. 10. SC low-pass decimator with $M = 4$. (a) Circuit. (b) Time frames.

Fig. 11. Nominal computer simulated amplitude responses of the SC decimator in Fig. 10. (a) Passband. (b) Overall.

TABLE II
SC LOW-PASS DECIMATOR WITH $M = 4$ CAPACITANCE VALUES

Solution	1	2	3	4
Output Terminal	1		2	
Damping	E	F	E	F
Amplifier Capacitor Set-1 YO	1.00957	1.38411	1	1
Y1	1.01232	1.24985	1.89417	1.89417
Y2	1.00892	1.12178	2.68790	2.68789
Y3	1	1	3.38663	3.38663
A	4.07695	4.07695	31.4045	55.6255
B	19.6998	9.2309	174.292	114.338
F	0	4.84026	0	59.9537
Amplifier Capacitor Set-2 XO	1.17406	3.31861	1.00956	1.00956
X1	1.11664	2.10469	1.01232	1.01232
X2	1.05849	1	1.00891	1.00891
X3	1	0	1	1
C	4.53678	42.8870	4.07694	4.07693
D	11.8521	156.858	9.27309	16.4250
E	19.6998	0	17.7031	0
C_{spread}	19.6998	156.858	174.292	114.338
ΣC	68.246	229.072	249.749	263.419

mator is in agreement with the response of Fig. 11, except for some local deviations around $F_s = 250$ kHz, and its multiples $2F_s$ and $3F_s$. Expanded measurements of such frequency-translated responses are presented in Fig. 12, showing the detection of the output signal components from dc to 15 kHz, when the input signal components are in the frequency bands from 235 to 265 kHz, in Fig. 12(a), from 485 to 515 kHz, in Fig. 12(b), and from 735 to 765 kHz, in Fig. 12(c). A minimum 48 dB rejection (close to the designed 50 dB) of the unwanted alias frequency signal components above 244 kHz was obtained in practice, thus suggesting the practical feasibility of the circuit. In the laboratory, we have also been able to increase by a factor of 10 the operating frequency of this discrete component prototype model. The input and output sampling rates
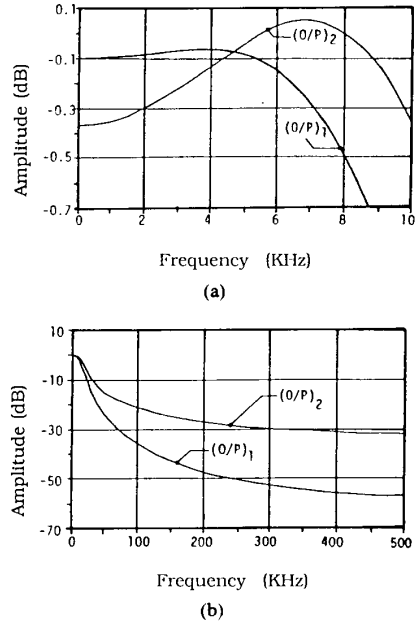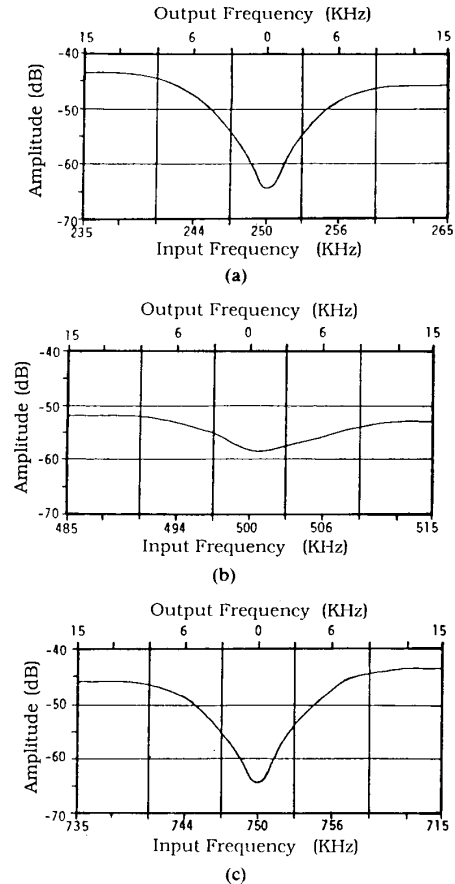

Fig. 12. Measured anti-aliasing performance for input signals in critical frequency bands. (a) 235–265 kHz. (b) 485–515 kHz. (c) 735–765 kHz.

become, respectively, 10 and 1 MHz, and the resulting cutoff frequency is extended up to 60 kHz. The measured performance in this situation gives similar results to those described above, with the appropriate frequency scaling. This showed the capability of the proposed SC decimator building blocks to operate at high frequency.

Experiments carried out in the discrete component prototype model suggested that clock feedthrough is responsible, in part, by the local deviations observed in the frequency-translated alias responses shown in Fig. 12. Other contributions to such deviations result from errors both in the capacitance ratios, and switch timing, both of which affect more the response of the circuit to input signals in those frequency bands than in the passband. This aspect, which was clearly put in evidence by a detailed investigation (by computer simulation) of the behavior of this SC decimator circuit, is discussed in more detail in the following section.

V. SENSITIVITY ASPECTS OF OPTIMUM IIR SC DECIMATORS

To understand the sensitivity performance of an IIR SC decimator with optimum implementation, it is convenient to interpret the relationship between the corresponding original and modified Z-transfer functions obtained following the systematic procedure described before. For this purpose we shall consider the example of the previous low-pass SC decimator, with $M = 4$, originally described by

$$H(Z) = \frac{K}{1 + b_1 \cdot Z^{-1} + b_2 \cdot Z^{-2}}. \quad (17\text{-a})$$

The corresponding complex-conjugate pole-pair location in the Z-plane with angular frequency $\theta = \omega/4F_s$ is represented as in Fig. 13(a). The appropriate equivalence for optimum implementation leads to the modified Z-transfer function

Fig. 13. Pole–zero pattern representation in the Z-plane. (a) Original transfer function. (b) Modified transfer function.

$F_s/2$, and in the frequency-translated alias bands corresponding to the pairing of poles and zeroes around F_s, $2F_s$, and $3F_s$. This is demonstrated in Figs. 14 and 15 showing some of the computer simulated amplitude responses of the SC low-pass decimator in Fig. 10 for ± 1-percent variations of the nominal capacitance values and ± 5 ns variations of the nominal time slots determining the sampling instants of the input signal. The passband amplitude response, in Fig. 14, is more affected by variations of the loop capacitors (e.g., Fig. 14(a)) than by variations of the input capacitors (e.g., Fig. 14(b)), and are not affected at all by variations of the input time slots (e.g., Fig. 14(c)). On the contrary, the frequency-translated amplitude alias

$$\overline{H}(Z) = K \frac{\bar{a}_0 + \bar{a}_1 \cdot Z^{-1} + \bar{a}_2 \cdot Z^{-2} + \bar{a}_3 \cdot Z^{-3} + \bar{a}_4 \cdot Z^{-4} + \bar{a}_5 \cdot Z^{-5} + \bar{a}_6 \cdot Z^{-6}}{1 + \bar{b}_1 \cdot Z^{-4} + \bar{b}_2 \cdot Z^{-8}} \quad (17\text{-b})$$

giving the pole–zero pattern configuration shown in Fig. 13(b). Although this is still ideally equivalent to a Z-transfer function with a single complex-conjugate pole-pair, such an equivalence is achieved by means of a pole–zero cancellation at frequencies around F_s, $2F_s$, and $3F_s$. The variability of the pole frequency and Q-factor is essentially determined by the capacitors A, B, C, D, and E in the loop of the decimator circuit, and is similar to the corresponding variability observed in a typical biquadratic section [17]. On the contrary, the variability of the zero frequencies and Q-factors is basically determined by the input capacitors of capacitor set X and capacitor set Y, as well as the timing accuracy of the time slots determining the corresponding delay factors. Therefore, under non-ideal circuit conditions, we should expect a rather different behavior of the amplitude response in the passband, corresponding to the single complex-conjugate pole-pair below
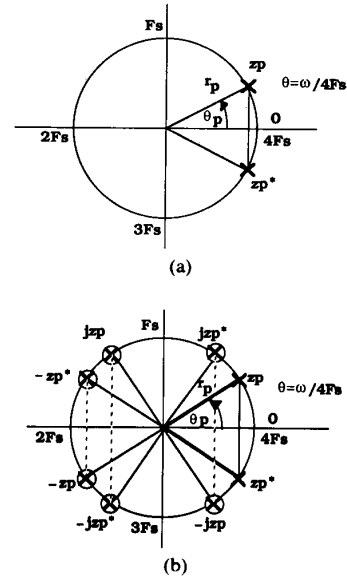
responses around F_s, in Fig. 15, as well as around $2F_s$ and $3F_s$ are not significantly affected by variations of the loop capacitors (e.g., Fig. 15(a)), but are critically dependent on the accuracy both of the input capacitors (e.g., Fig. 15(b)) and input time slots (e.g., Fig. 15(c)).

VI. CONCLUSIONS

This paper proposed new IIR SC decimator building blocks for sampling rate reduction from a high input value MF_s to a lower output value F_s. The optimum implementation of such SC decimator building blocks enables us, in the first place, to utilize operational amplifiers whose speed requirements are determined by the lower output sampling rate, rather than the higher input sampling rate that typically constraints the amplifiers in traditional non-optimum implementations. This also yields further advan-
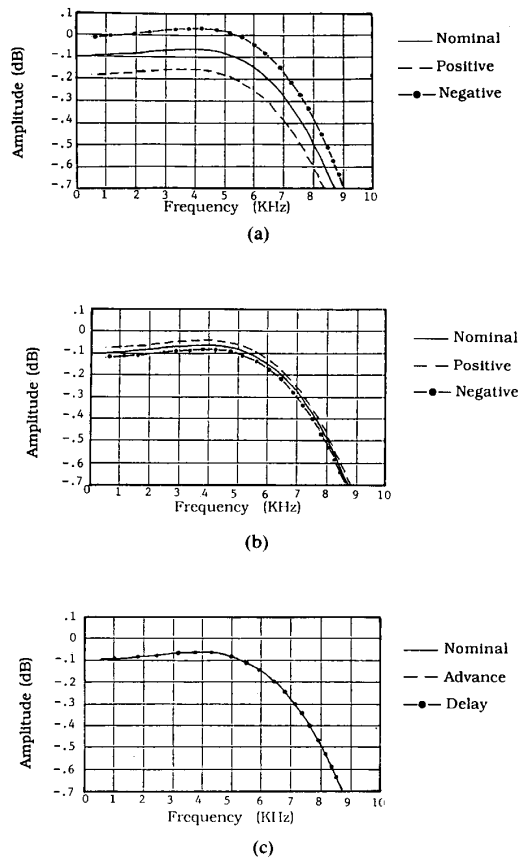
Fig. 14. Computer simulated variability of the amplitude response in the passband due to: (a) variation in Capacitor A. Passband response with ± 1 percent variation in Capacitor A; (b) variation in capacitor $Y0$. Passband response with 1 percent variation in Capacitor $Y0$; (c) variation in time slot 3; ± 5 ns variation of time slot 3 in both sampling blocks X and Y.
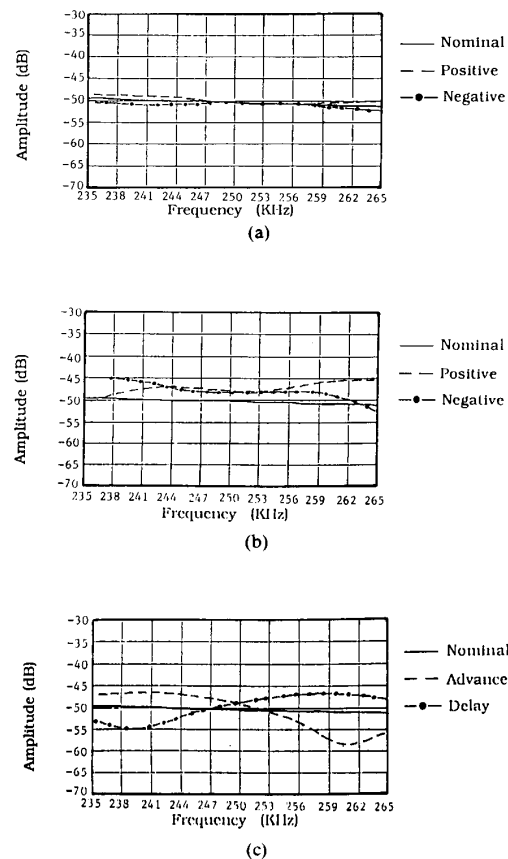
Fig. 15. Computer simulated variability of the amplitude response in the first aliasing band due to: (a) variation in capacitor C; (b) variation in capacitor $Y0$; (c) variation in time slot 3.

tages with respect to the reduction of the capacitance spread and total capacitor area, and thus largely offsets the increased number of switching waveforms required for the realization of such optimum SC decimator building blocks. In the second place, our design approach makes it possible to implement decimator Z-transfer functions where the numerator polynomial function can have an arbitrary order regardless of the order of the denominator polynomial function, and thus can be optimally tailored to meet specific anti-aliasing filtering requirements. We presented the general design procedure of SC decimator building blocks for first- and second-order IIR Z-transfer functions, and gave practical design examples for illustration purposes. The experimental evaluation of a discrete component prototype model demonstrated the feasibility of the proposed SC decimator building blocks, and also showed the capability for high-frequency operation.
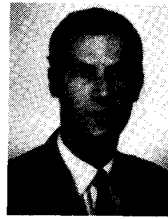
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