OPTIMUM IMPLEMENTATION OF A MULTISTAGE IIR SC BANDPASS DECIMATOR FOR A VOICEBAND ANALOGUE INTERFACE SYSTEM

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Abstract

A novel methodology has been developed for the design of multistage IIR Switched-Capacitor (SC) decimators with optimum implementation. The approach employs a cascade of only IIR SC decimator building blocks as a means of obtaining minimum order structures for high selectivity filtering requirements with very large factors of sampling rate reduction. The strategy for reducing the sampling rate is determined in conjunction with the pole-zero pairing to achieve relaxed speed requirements for the operational amplifiers together with reduced capacitance spread and total capacitor area. This is demonstrated for an SC bandpass decimator which virtually eliminates the need for costly on-chip continuous-time filters in a voiceband analogue interface system, thus making it extremely attractive for integrated circuit implementation.

1. INTRODUCTION.

An Analogue Interface System (AIS) is a specialised signal processing system which provides all the filtering and signal conversion functions that are required for interfacing continuous-time analogue and sampled-data digital environments. One of the main functions to be performed in the receive path of an AIS is the anti-aliasing filtering of the incoming analogue signals. Traditionally, an Anti-Aliasing Filter (AAF) has been implemented by a combination of a low selectivity active-RC prefilter followed by an SC decimator. For high selectivity filtering requirements FIR SC decimators [1] need high order transfer functions that render the resulting SC circuits rather complex for Integrated Circuit (IC) implementation. IIR SC decimators [2], on the other hand, have been implemented in an non-optimum fashion that imposes high speed requirements for the Operational Amplifiers (OA's) together with a large capacitance spread and total capacitor area. Such limitations have compelled the utilisation of moderate to large factors of sampling rate reduction (typically less than 70 for voiceband AIS applications) and which, in turn, have determined the design of minimum second order active-RC prefilters that still occupy a considerable amount of silicon area. However, recent advances in the design of IIR SC decimator building blocks [3,4] have indicated the potential for considerably increasing the factors of sampling rate reduction in AIS applications, at no expense of the speed requirements of the OA's, and thus further simplifying or even eliminating costly on-chip active RC prefilters. Multistage architectures of such IIR SC decimator building blocks are particularly suitable for high selectivity filtering applications with factors of sampling rate reduction larger than 100.

Within the framework of multirate digital signal processing an efficient methodology has been proposed for the design of optimal multistage IIR decimators employing a cascade of FIR decimators, for sampling rate reduction from MF_S to F_S, followed by an IIR filter operating at the lower output sampling rate F_S [5]. In this approach the FIR decimating stages basically determine the anti-aliasing filtering characteristic above $F_S/2$, whereas the IIR filter is responsible for the baseband filtering characteristic from DC to $F_S/2$. Although quite attractive for digital implementations, such design methodology is not amenable for the counterpart SC implementation mainly for reasons of circuit efficiency. A rather complex multistage FIR SC decimator would be needed to shape solely the specified anti-aliasing band and an additional high order IIR SC filter would still be needed for defining the desired baseband response.

In this paper we present a novel design methodology that is more adequate for the implementation of multistage IIR SC decimators. This approach leads to minimum order structures employing only IIR SC decimator building blocks designed to meet both of the anti-aliasing and baseband filtering specifications. The strategy for reducing the sampling rate is determined in conjunction with the pole-zero pairing to achieve relaxed speed requirements for the OA's together with reduced capacitance spread and total capacitor area. A design example is given of an SC bandpass decimator that is appropriate for a voiceband AIS and which virtually eliminates the need for costly on-chip active-RC prefilters.

2. IIR SC DECIMATOR BUILDING BLOCKS

The basic building block for the implementation of multistage IIR SC decimators is illustrated in Fig.1 [3,4]. This consists of a single SC network with input sampling rate MF_S and whose output sampling rate F_S determines the speed requirements of the OA's. The corresponding z-transfer functions are given by

$$T_1(z) = \frac{[(B+F)X(z)-(C+E)Y(z)]+[EY(z)-BX(z)]z^{-M}}{(BD+DF)+(AC+AE-DF-2BD)z^{-M}+(BD-AE)z^{-2M}} \qquad (1\text{-a})$$

for the output terminal-1, and by

$$T_2(z) = \frac{DY(z)+[AX(z)-DY(z)]z^{-M}}{(BD+DF)+(AC+AE-DF-2BD)z^{-M}+(BD-AE)z^{-2M}} \qquad (1\text{-b})$$

for the output terminal-2. The terms X(z) and Y(z) represent the equivalent transfer functions of the input SC branches organised as polyphase structures [1]. The procedure for designing this SC decimator building block is carried-out by equating either (1-a) or (1-b) to the appropriate modified z-transfer function of the decimator

prototype filter. This is a very flexible design procedure allowing a significant reduction of the capacitance spread and total capacitor area in the circuit, together with the maximisation of signal handling capability. Next, we shall look at ways of designing a multistage IIR SC decimator using this type of building block.

3. MULTISTAGE IIR SC DECIMATORS

General Design Methodology: The first step in the design of a multistage IIR SC decimator consists of obtaining the overall z-transfer function of the corresponding decimator prototype filter that meets the specified baseband and anti-aliasing filtering characteristics. For implementation using a cascade of N second order building blocks this is initially expressed as

$$H(z) = \prod_{i=1}^{N} k_i \frac{(1-2r_{0_i}\cos(\theta_{0_i})z^{-1}+r_{0_i}^2 z^{-2})}{(1-2r_{p_i}\cos(\theta_{p_i})z^{-1}+r_{p_i}^2 z^{-2})} \qquad (2)$$

where the unit delay period is referred to the input sampling rate MF_S of the decimator. The above z-transfer function can not be directly implemented since this would lead to traditional SC filter building blocks operating at the high sampling rate MF_S. Instead, the purpose of our design methodology consists of assigning appropriate factors of sampling rate reduction to optimum IIR SC decimator building blocks in order to gradually decrease the sampling rate and thus achieving the corresponding benefits of more relaxed speed requirements for the OA's and lower capacitance spreads. Such z-transfer function with non-uniform sampling rate is obtained by a suitable modification of (2) and can be written in the following general form

$$\bar{H}(z) = \prod_{i=1}^{N} k_i \frac{(1-2\bar{r}_{0_i}\cos(\bar{\theta}_{0_i})z^{-T_i}+\bar{r}_{0_i}^2 z^{-2T_i})}{(1-2\bar{r}_{p_i}\cos(\bar{\theta}_{p_i})z^{-T_i}+\bar{r}_{p_i}^2 z^{-2T_i})} \qquad (3)$$

where i gives the sequence of the decimator stages from the input, i=1, to the output, i=N. If we designate the input sampling frequency of each SC decimator stage as F_i, then the normalised delay periods T_i appearing in the corresponding z-transfer functions are determined by

$$T_i = \prod_{j=1}^{i} M_j \qquad (4)$$

where M_j represent the factors of sampling rate reduction of the decimator stages from j=1 to j=i, and M is the desired overall decimation factor of the multistage structure. The modified poles and zeroes in (3) are obtained using well known properties of discrete-time transfer functions [6].

Strategy for Decimation and Pole-Zero Pairing: The selection of a particular sequence for decimation is determined in conjunction with the assignment of poles and zeroes to each SC decimator building block and by taking into account the corresponding frequency-translated aliasing responses. This makes it possible not only to obtain the desired baseband specifications, as in traditional cascade filter design methods, but also the specified anti-aliasing filtering response. The optimum sequence of decimation and corresponding pole-zero pairing are obtained by the computer assisted trial-and-error design procedure schematically illustrated in Fig.2, and where we make use of the following design criteria:

i) Decompose M in prime factors by descending order, in order to minimise the speed requirements of the OA's.

ii) Associate the larger values of the pole and zero frequencies to the lower values of T_i, i.e. minimise F_{si}/F_{pi} and F_{si}/F_{oi}, in order to minimise capacitance spread and total capacitor area.

iii) Implement first lowpass decimator stages with low selectivity poles, i.e. low Q_p, and wide transition bands in order to reject the alias frequency components at higher frequency, and also to increase the attenuation of the input high frequency noise.

iv) Implement high selectivity lowpass decimator stages, as well as bandpass decimator stages, at the heart of the cascade structure in order to increase the attenuation of those aliasing frequency components closer to the passband, and also to maximise the dynamic range of the overall decimator.

v) Implement all highpass decimator stages at the end of the cascade structure, since they only contribute to the definition of the lower stopband of the baseband response.

The automated design procedure is carried-out for all decimator stages until the resulting amplitude response meets the target specifications, both in the baseband and in the aliasing band. Once the optimum sequence of decimation and pole-zero pairing have been determined we can carry-out further single stage optimisations in order to improve signal handling capability and minimise capacitance spread.

4. IIR SC BANDPASS DECIMATOR FOR A VOICEBAND AIS

Decimator Requirements and Architecture: In order to demonstrate the above methodology we shall consider now the design of an IIR SC bandpass decimator with the specifications given in Table-1, and which is appropriate for a voiceband AIS. For an input sampling rate above 1MHz only a mere first order prefilter is required and this can be realised by a simple off-chip RC section. Despite this high input sampling rate, the decimator will be designed to allow comfortable settling times for the OA's determined by switching frequencies well below 1MHz.

The complete architecture of the SC bandpass decimator is illustrated in Fig.3. A high selectivity 12th. order SC bandpass decimator with a factor M=40 of sampling rate reduction is designed to meet the baseband specifications together with a minimum 55dB rejection of the aliasing frequency components up to $40F_S/2$ and the corresponding repetition above $40F_S/2$. In front of this bandpass decimator we place a simple 2nd. order lowpass decimator to increase the input sampling rate up to $120F_S$ and, at the same time, guarantee the required 65dB rejection of the aliasing frequency components over the entire frequency range from baseband to $120F_S/2$ and the corresponding repetition above $120F_S/2$.

Results: Based on a computer aided filter synthesis procedure [7] we obtained the bilinear discrete-time coefficients for the lowpass 2nd. order and for the bandpass 12th. order decimator prototype filters, respectively given in Table-2 and in Table-3. The SC lowpass decimator with a factor M=3 of sampling rate reduction is easily implemented following the procedure outlined in [3,4]. The implementation of the multistage SC bandpass decimator following the methodology

described before leads to the structure of Fig.4, where the intermediate parameters of the decimator stages are indicated in Table-4. Then, the design of each one of the SC decimator building blocks proceedes in a similar way as for the SC lowpass decimator. The overall SC bandpass decimator is presented in Fig.5-a where we obtain a maximum capacitance spread of 48 and total capacitor area of 528.75. The corresponding switching waveforms for operation are illustrated in Fig.5-b. For non--overlapping switching waveforms with zero guard intervals the resulting minimum time for the settling of the OA's is 889ns, occuring in the input SC lowpass decimator stage. For the remaining decimator stages we obtain, respectively, 5.2μs, 9.4μs, 18.8μs and 37.6μs. For comparison, the traditional implementation of an SC bandpass decimator meeting similar specifications would lead to a maximum capacitance spread of the order of 800 with a total capacitor area above 5000. In addition, significantly faster OA's would be required to settle within a time interval of only 434ns.

The correct designs of the SC lowpass and bandpass decimators and of the complete decimator structure have been verified by computer simulations. Fig.6 and Fig.7 illustrate the ideal amplitude baseband responses, respectively of the SC lowpass and bandpass decimators, i.e. from DC to $120F_S/2$ for the former and from DC to F_S for the latter. The complete response of the overall SC bandpass decimator in the frequency band from DC to $120F_S/2$, is shown in Fig.8 giving the required 65 dB minimum rejection of the unwanted aliasing frequency components,as specified in Table-1.

5. CONCLUSIONS

This paper described a novel methodology for the design of multistage IIR Switched-Capacitor (SC) decimators with optimum implementation. This is based on the cascade of only IIR SC decimator building blocks as a means of obtaining minimum order structures for high selectivity filtering requirements with large factors of sampling rate reduction. In such structures, the strategy for decimation is determined in conjunction with the pole-zero pairing to achieve relaxed speed requirements for the operational amplifiers together with reduced capacitance spread and total capacitor area. An automated trial-and-error procedure assists in this process. The proposed approach has been employed for designing an SC bandpass decimator which virtually eliminates the need for costly on-chip continuous-time filters in a voiceband analogue interface system, thus making it extremely attractive for integrated circuit implementation.

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Table-2: Bilinear discrete-time coefficients of the 2nd. order lowpass prototype filter.

F_s (MHz)	1.152
k	1.6833985E-3
$2r_o\cos(\theta_o)$	-2
r_o^2	1
$2r_p\cos(\theta_p)$	1.8832212
r_p^2	0.88996253

	Frequency (KHz)		Attenuation (dB)
Low Stopband	0 - 0.15	min	60
Passband	0.3 - 3.4	max	0.5
Upper Stopband	4 - 4.8	min	40
Aliasing Band	4.8 - >1000	min	65

Table-1 : Specifications of the IIR SC Bandpass Decimator.

Stage (Sel.)	1 (BP)	2 (LPN)	3 (LPN)	4 (LPN)	5 (HPNF)	6 (HPNF)
$2r_o\cos(\theta_o)$	0	1.982303	1.993029	1.995108	1.999999	1.999995
r_o^2	-1	1	1	1	1	1
$2r_p\cos(\theta_p)$	1.981607	1.984651	1.993228	1.974924	1.999110	1.995752
r_p^2	0.981843	0.987177	0.996371	0.976252	0.999133	0.995794
F_s (kHz)	384	LPN-Lowpass Notch	BP-Bandpass	HPNF-Highpass Notch Filter		

Table-3 : Bilinear discrete-time coefficients of the 12 th. order bandpass decimator prototype filter.

Stage (Sel.)	1 (LP)	2 (LPN)	3 (LPN)	4 (BPN)	5 (HPNF)	6 (HPNF)
$2\bar{r}_o\cos(\bar{\theta}_o)$	-2	1.571346	1.340384	0.344887	1.999840	1.991538
$\bar{r}_o^2$	1	1	1	1	1	1
$2\bar{r}_p\cos(\bar{\theta}_p)$	1.981607	1.877846	1.664613	1.213774	1.930394	1.786013
$\bar{r}_p^2$	0.981843	0.938905	0.965309	0.624551	0.966196	0.846884
F_{s_1} (kHz)	384	76.8	38.4	19.2	9.6	9.6

LP- Lowpass LPN- Lowpass Notch BPN-Bandpass Notch HPNF-Highpass Notch Filter

Table-4 : Bilinear discrete-time coefficients of the 12 th. order bandpass decimator.

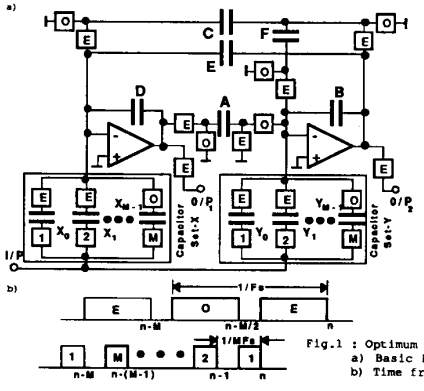

Fig.1 : Optimum IIR SC decimator .
a) Basic building block.
b) Time frames.

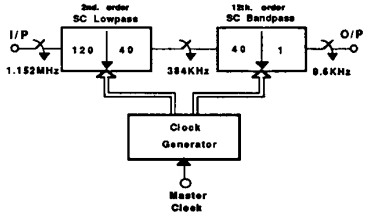

Fig.3 : Overall Architecture of the SC Bandpass Decimator.

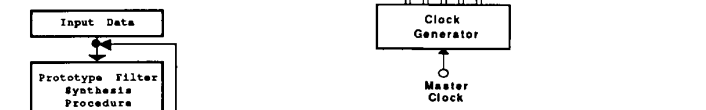

Fig.4 : Multistage SC Bandpass Decimator System (M=40).

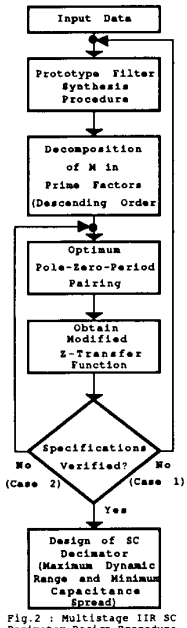

Fig.2 : Multistage IIR SC Decimator Design Procedure

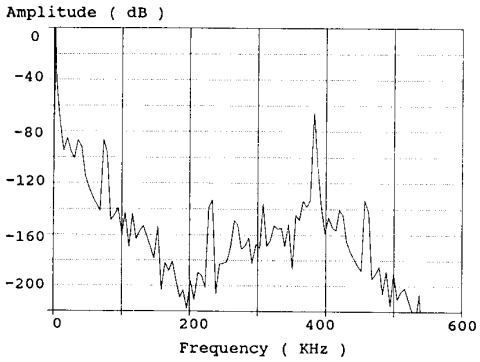

Fig. 8 : IIR SC Bandpass Decimator (Lowpass + Bandpass).

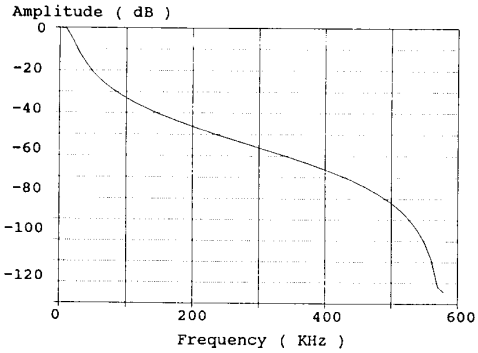

Fig. 6 : IIR SC Lowpass Decimator.

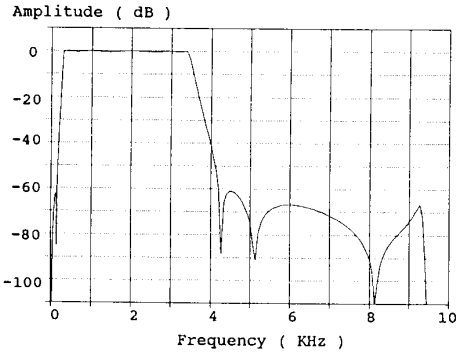

Fig. 7 : IIR SC Bandpass Decimator.

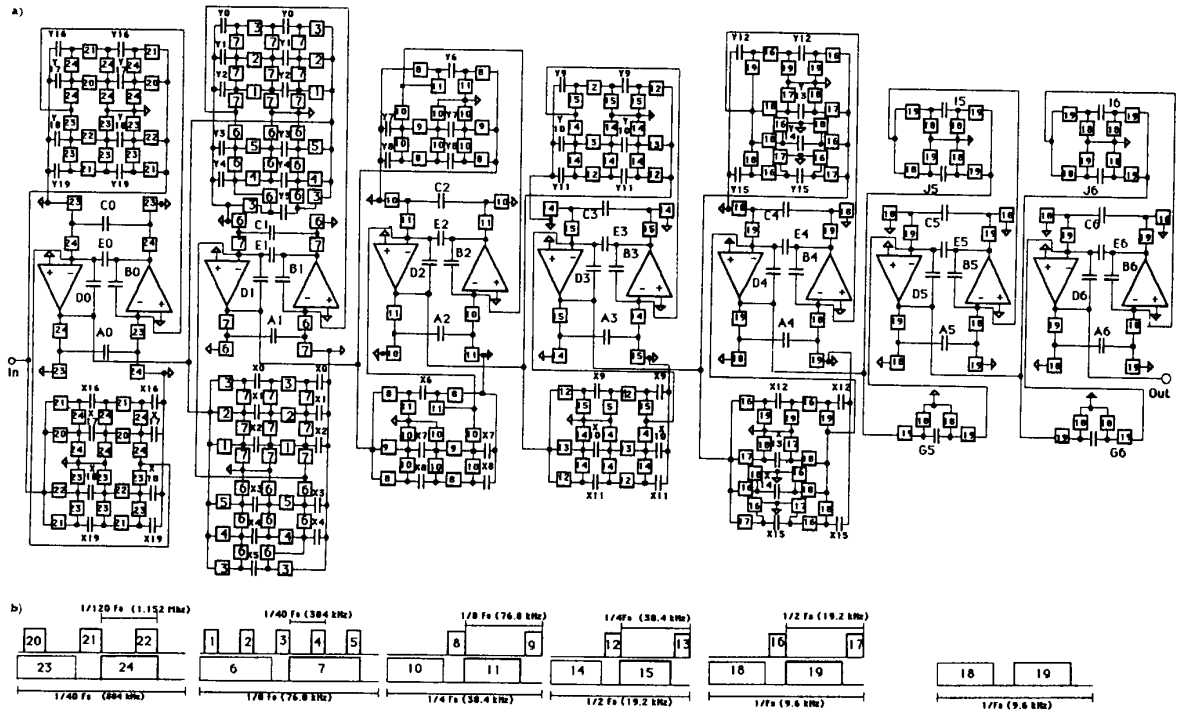

Fig 5 IIR SC Bandpass Decimator. a) Complete Structure b) Switching Waveforms